Avant!

Chapter 29

Running Demos

This chapter contains examples of basic file construction techniques, advanced features, and simulation tricks. Several Star-Hspice input files are listed and described.

The following topics are covered in this chapter:

Using the Demo Directory Tree

The last section of this chapter is a listing of demonstration files, which are designed as good training examples.These examples are included with most Star-Hspice distributions in the *demo* directory tree, where *$installdir* is the installation directory environment variable:

$installdir/demo/hspice	*/alge*	algebraic output
	/apps	general applications
	/behave	analog behavioral components
	/bench	standard benchmarks
	/bjt	bipolar components
	/cchar	cell characterization prototypes
	/ciropt	circuit level optimization
	/ddl	Discrete Device Library
	/devopt	device level optimization
	/fft	Fourier analysis
	/filters	filters
	/mag	transformers, magnetic core components
	/mos	MOS components
	/pci	Intel Peripheral Component Interconnect
	/rad	radiation effects (photocurrent)
	/sources	dependent and independent sources
	/tline	filters and transmission lines

Running the Two-Bit Adder Demo

This two-bit adder demonstrates many techniques to improve circuit simulation efficiency, accuracy, and productivity. The adder in demonstration file *demo/hspice/apps/mos2bit.sp* is composed of two-input NAND gates defined by the subcircuit NAND. CMOS devices are parameterized with length, width, and output loading. Descriptive names enhance the readability of this circuit.

The subcircuit ONEBIT defines the two half adders with carry in and carry out. The two-bit adder is created by two calls to ONEBIT. Independent piecewise linear voltage sources provide input stimuli. Complex waveforms are created by the "R" repeat function.

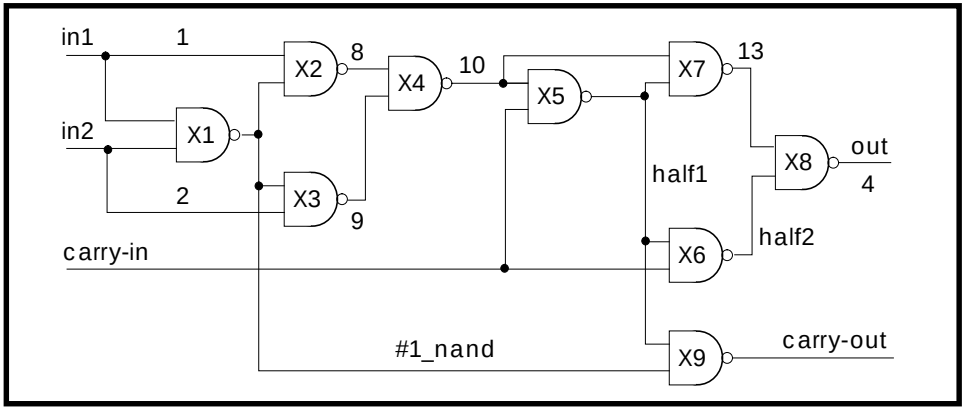

Figure 29-1: – One-bit Adder Subcircuit

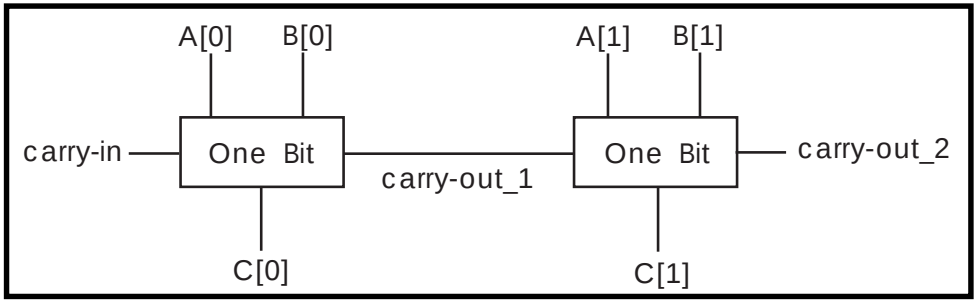

Figure 29-2: – Two-bit Adder Circuit

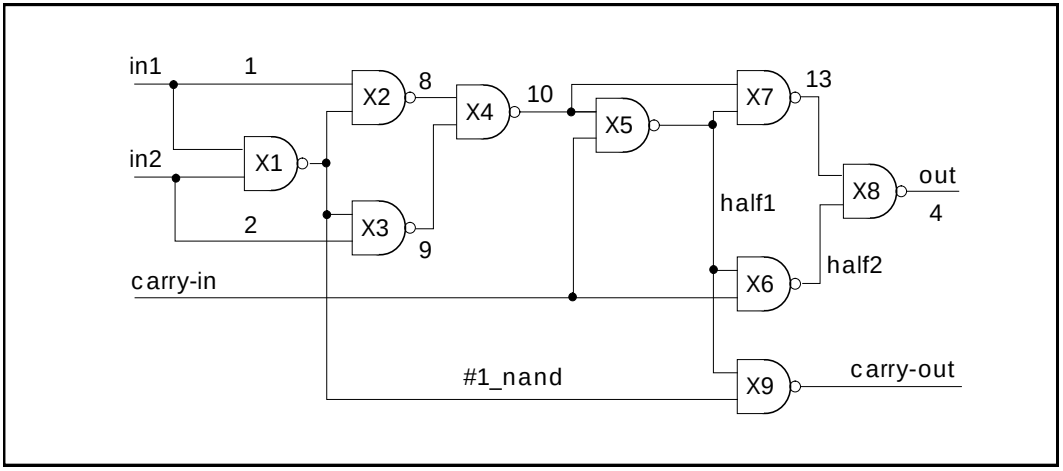

Figure 29-3: – 1-bit NAND Gate Binary Adder

MOS Two-Bit Adder Input File

```
*FILE: MOS2BIT.SP - ADDER - 2 BIT ALL-NAND-GATE BINARY ADDER
.OPTIONS ACCT NOMOD FAST autostop scale=1u gmindc=100n
.param lmin=1.25  hi=2.8v lo=.4v vdd=4.5
.global vdd
.TRAN .5NS 60NS
.graph TRAN V(c[0]) V(carry-out_1) V(c[1]) V(carry-out_2)
+ par('V(carry-in)/6 + 1.5')
+ par('V(a[0])/6     + 2.0')
+ par('V(b[0])/6     + 2.5') (0,5)
.MEAS PROP-DELAY TRIG V(carry-in) TD=10NS VAL='vdd*.5' RISE=1
+                TARG V(c[1])     TD=10NS VAL='vdd*.5' RISE=3
*
.MEAS PULSE-WIDTH  TRIG V(carry-out_1) VAL='vdd*.5' RISE=1
+                  TARG V(carry-out_1) VAL='vdd*.5' FALL=1
*
.MEAS FALL-TIME    TRIG V(c[1]) TD=32NS VAL='vdd*.9' FALL=1
+                  TARG V(c[1]) TD=32NS VAL='vdd*.1' FALL=1
VDD  vdd gnd DC vdd
X1    A[0]  B[0]  carry-in     C[0]  carry-out_1  ONEBIT
X2    A[1]  B[1]  carry-out_1  C[1]  carry-out_2  ONEBIT
```

Subcircuit Definitions

```
.subckt NAND  in1  in2  out   wp=10 wn=5
   M1  out  in1 vdd vdd P W=wp  L=lmin    ad=0
   M2  out  in2 vdd vdd P W=wp  L=lmin    ad=0
   M3  out  in1 mid gnd N W=wn  L=lmin    as=0
   M4  mid  in2 gnd gnd N W=wn  L=lmin    ad=0
   CLOAD out gnd 'wp*5.7f'
.ends

* switch model equivalent of the NAND. Gives a 10 times
* speedup over the MOS version.

.subckt NANDx  in1  in2  out   wp=10 wn=5
   G1 out vdd vdd in1  LEVEL=1 MIN=1200 MAX=1MEG 1.MEG -.5MEG
   G2 out vdd vdd in2  LEVEL=1 MIN=1200 MAX=1MEG 1.MEG -.5MEG
   G3 out mid in1 gnd  LEVEL=1 MIN=1200 MAX=1MEG 1.MEG -.5MEG
   G4 mid gnd in2 gnd  LEVEL=1 MIN=1200 MAX=1MEG 1.MEG -.5MEG
   cout out gnd 300f
.ends

.subckt ONEBIT  in1  in2  carry-in  out  carry-out
         X1  in1      in2      #1_nand   NAND
         X2  in1      #1_nand  8         NAND
         X3  in2      #1_nand  9         NAND
         X4  8        9        10        NAND
         X5  carry-in 10       half1     NAND
         X6  carry-in half1    half2     NAND
         X7  10       half1    13        NAND
         X8  half2    13       out       NAND
         X9  half1    #1_nand  carry-out NAND
.ENDS ONEBIT
```

Stimuli

```
V1 carry-in gnd PWL(0NS,lo 1NS,hi 7.5NS,hi 8.5NS,lo 15NS lo R
V2 A[0] gnd PWL  (0NS,hi 1NS,lo 15.0NS,lo 16.0NS,hi 30NS hi R
V3 A[1] gnd PWL  (0NS,hi 1NS,lo 15.0NS,lo 16.0NS,hi 30NS hi R
V4 B[0] gnd PWL  (0NS,hi 1NS,lo 30.0NS,lo 31.0NS,hi 60NS hi
V5 B[1] gnd PWL  (0NS,hi 1NS,lo 30.0NS,lo 31.0NS,hi 60NS hi
```

Models

```
.MODEL N  NMOS LEVEL=3  VTO=0.7  UO=500    KAPPA=.25 KP=30U
+ ETA=.01    THETA=.04 VMAX=2E5 NSUB=9E16 TOX=400 GAMMA=1.5
+ PB=0.6     JS=.1M    XJ=0.5U  LD=0.1U   NFS=1E11 NSS=2E10
+ RSH=80     CJ=.3M    MJ=0.5   CJSW=.1N  MJSW=0.3
+ acm=2  capop=4
.MODEL P  PMOS LEVEL=3  VTO=-0.8 UO=150    KAPPA=.25 KP=15U
+ ETA=.015 THETA=.04 VMAX=5E4 NSUB=1.8E16 TOX=400 GAMMA=.672
+ PB=0.6    JS=.1M    XJ=0.5U  LD=0.15U    NFS=1E11  NSS=2E10
+ RSH=80    CJ=.3M    MJ=0.5   CJSW=.1N   MJSW=0.3
+ acm=2  capop=4
.END
```

Running the MOS I-V and C-V Plotting Demo

It is often necessary to review the basic transistor characteristics to diagnose a simulation or modeling problem. This demonstration file, *demo/hspice/mos/mosivcv.sp*, is a template file that can be used with any MOS model. The example shows the easy input file creation and the complete graphical results display. The following features aid model evaluations:

SCALE=1u	sets the element units to microns from meters since users generally think in microns rather than meters
DCCAP	forces the voltage variable capacitors to be evaluated during a DC sweep
node names	makes the circuit easy to understand. Up to 16 characters can be used in the symbolic name
.GRAPH	.GRAPH statements create high resolution plots. A graph model can be added to set additional characteristics

This template provides the ability to get plots of internal variables such as:

i(mn1)	i1, i2, i3, or i4 can specify the true branch currents for each transistor node
LV18(mn6)	total gate capacitance (C-V plot)
LX7(mn1)	gate transconductance GM. (LX8 specifies GDS, and LX9 specifies GMB)

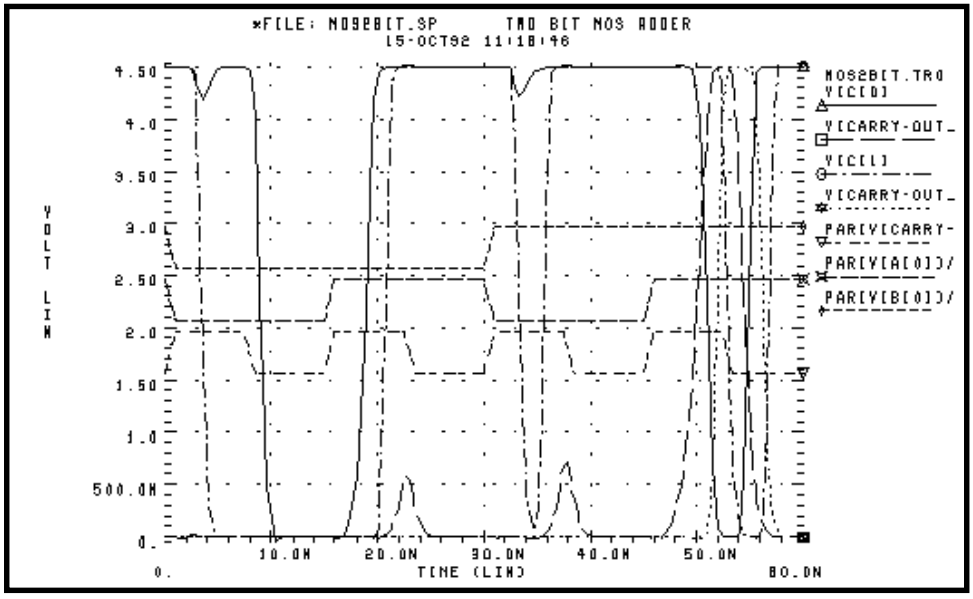

Figure 29-4: – MOS IDS Plot

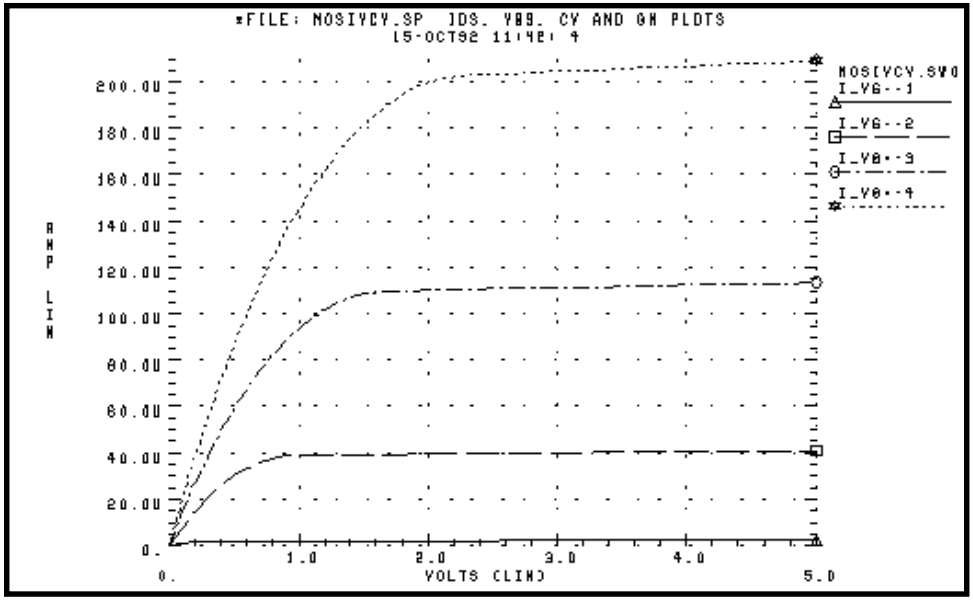

Figure 29-5: – MOS VGS Plot

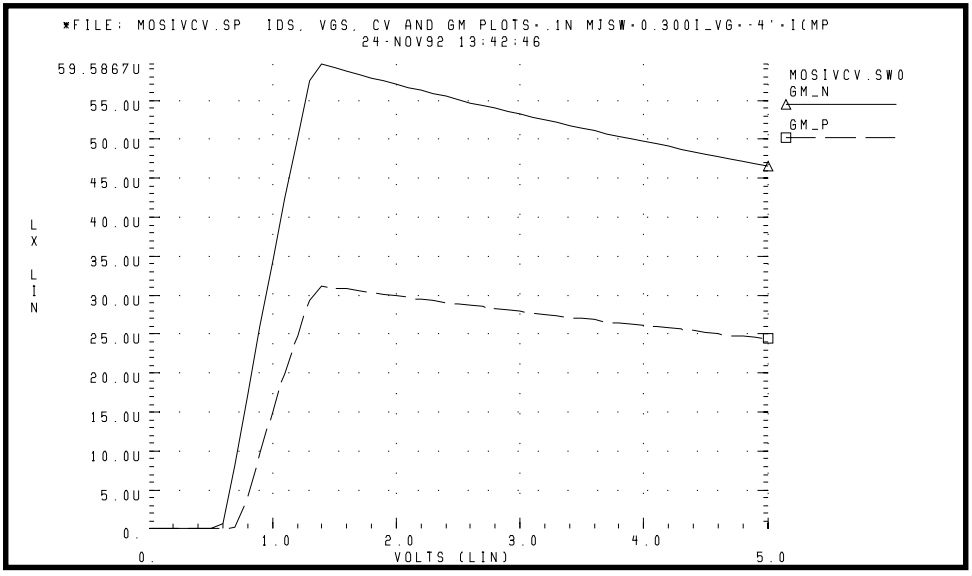

Figure 29-6: MOS GM Plot

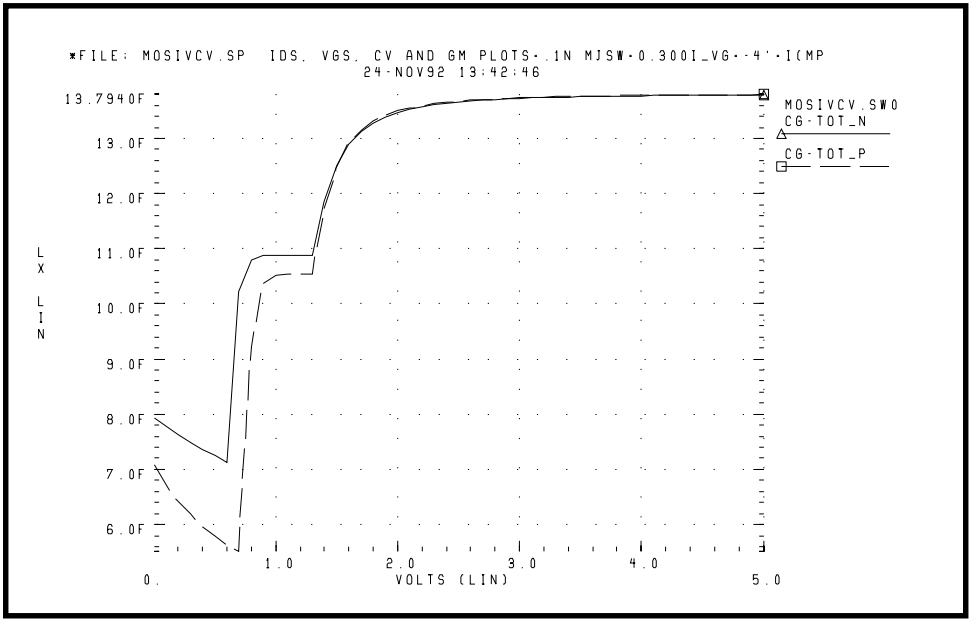

Figure 29-7: MOS C-V Plot

MOS I-V and C-V Plot Example Input File

```
*FILE: MOSIVCV.SP IDS, VGS, CV AND GM PLOTS

.OPTIONS SCALE=1U DCCAP
.DC VDDN 0 5.0 .1 $VBBN 0 -3 -3      sweep supplies
.PARAM ww=8 LL=2

$ ids-vds curves
.GRAPH 'I_VG=1' =I(MN1) 'I_VG=2' =I(MN2) 'I_VG=3' =I(MN3)
+ 'I_VG=4' =I(MN4)
.GRAPH 'I_VG=-1'=I(MP1) 'I_VG=-2'=I(MP2) 'I_VG=-3'=I(MP3)
+ 'I_VG=-4'=I(MP4)
$ ids-VGs curves
.GRAPH 'I_VD=.5'=I(MN6) 'I_VD=-.5'=I(MP6)
$ gate caps (cgs+cgd+cgb)
.GRAPH 'CG-TOT_N'=LX18(MN6) 'CG-TOT_P'= LX18(MP6)
$ gm
.GRAPH 'GM_N'=LX7(MN6) 'GM_P'=LX7(MP6)

VDDN vdd_n gnd 5.0
VBBN vbb_n gnd 0.0
EPD  vdd_p gnd vdd_n gnd -1   $ reflect vdd for P devices
EPB  vbb_p gnd vbb_n gnd -1   $ reflect vbb for P devices

V1  vg1  gnd 1
V2  vg2  gnd 2
V3  vg3  gnd 3
V4  vg4  gnd 4
V5  vddlow_n  gnd .5
V-1 vg-1 gnd -1
V-2 vg-2 gnd -2
V-3 vg-3 gnd -3
V-4 vg-4 gnd -4
V-5 vddlow_p gnd -.5

MN1  vdd_n  vg1  gnd vbb_n N  W=ww L=LL
MN2  vdd_n  vg2  gnd vbb_n N  W=ww L=LL
MN3  vdd_n  vg3  gnd vbb_n N  W=ww L=LL
MN4  vdd_n  vg4  gnd vbb_n N  W=ww L=LL

MP1  gnd vg-1 vdd_p vbb_p P  W=ww L=LL
```

```
MP2  gnd vg-2 vdd_p vbb_p P  W=ww L=LL
MP3  gnd vg-3 vdd_p vbb_p P  W=ww L=LL
MP4  gnd vg-4 vdd_p vbb_p P  W=ww L=LL

MN6  vddlow_n vdd_n  gnd vbb_n N  W=ww L=LL
MP6  gnd vdd_p vddlow_p vbb_p P  W=ww L=LL

.MODEL      N  NMOS LEVEL=3   VTO=0.7  UO=500    KAPPA=.25
+ KP=30U    ETA=.01 THETA=.04 VMAX=2E5 NSUB=9E16 TOX=400
+ GAMMA=1.5 PB=0.6  JS=.1M    XJ=0.5U  LD=0.1U   NFS=1E11
+ NSS=2E10  RSH=80  CJ=.3M    MJ=0.5   CJSW=.1N  MJSW=0.3
+ acm=2     capop=4
*
.MODEL      P   PMOS LEVEL=3   VTO=-0.8 UO=150   KAPPA=.25
+ KP=15U    ETA=.015 THETA=.04 VMAX=5E4 NSUB=1.8E16 TOX=400
+ GAMMA=.67 PB=0.6   JS=.1M    XJ=0.5U  LD=0.15U NFS=1E11
+ NSS=2E10  RSH=80   CJ=.3M    MJ=0.5   CJSW=.1N MJSW=0.3
+ acm=2     capop=4

.END
```

Running the CMOS Output Driver Demo

ASIC designers face the problem of integrating high performance IC parts onto a printed circuit board (PCB). The output driver circuit is most critical to the overall system performance. The demonstration file *demo/hspice/apps/asic1.sp* shows the models for an output driver, the bond wire and leadframe, and a six inch length of copper transmission line.

This simulation demonstrates how to:

- Define parameters and measure test outputs
- Use the “LUMP5” macro to input geometric units and convert them to electrical units
- Use .MEASURE statements to calculate the peak local supply current, voltage drop, and power
- Measure RMS power, delay, rise times and fall times
- Simulate and measure an output driver under load. The load consists of
- Bondwire and leadframe inductance
- Bondwire and leadframe resistance
- Leadframe capacitance
- Six inches of 6 mil copper on a FR-4 printed circuit board
- Capacitive load at end of copper wire

The Star-Hspice strategy is to:

- Create a five-lump transmission line model for the copper wire
- Create single lumped models for leadframe loads

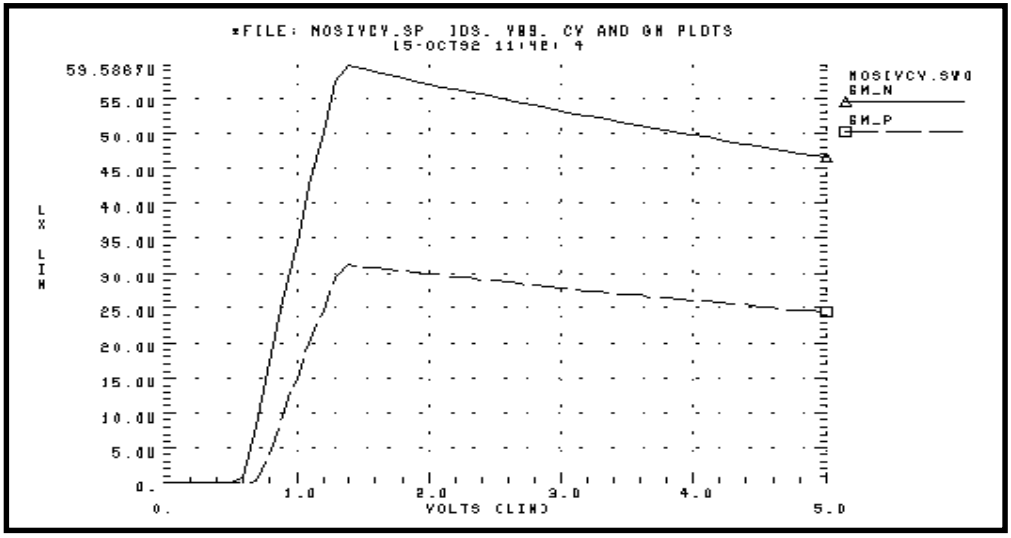

Figure 29-8: – Noise Bounce

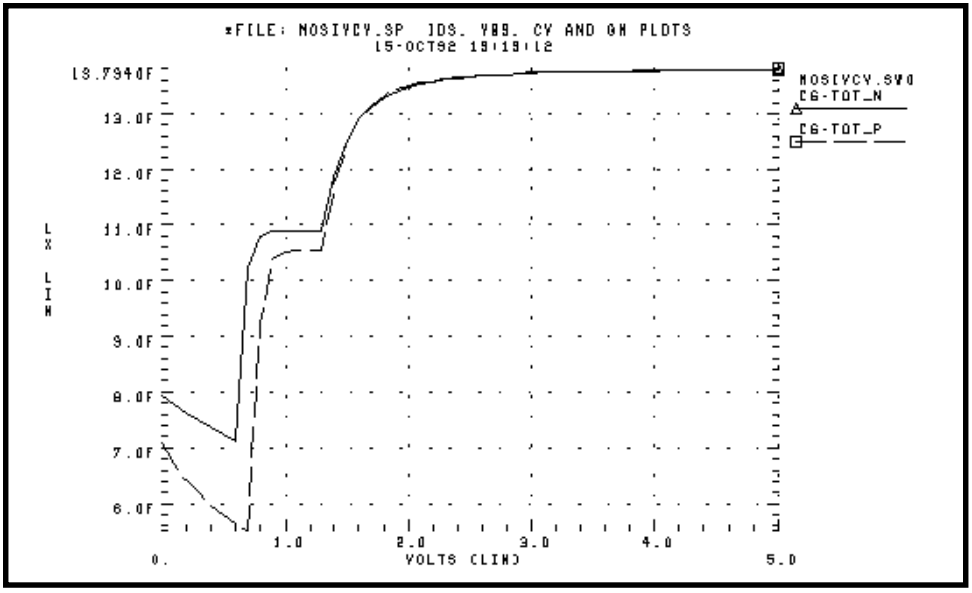

Figure 29-9: Asic1.sp Demo Local Supply Voltage

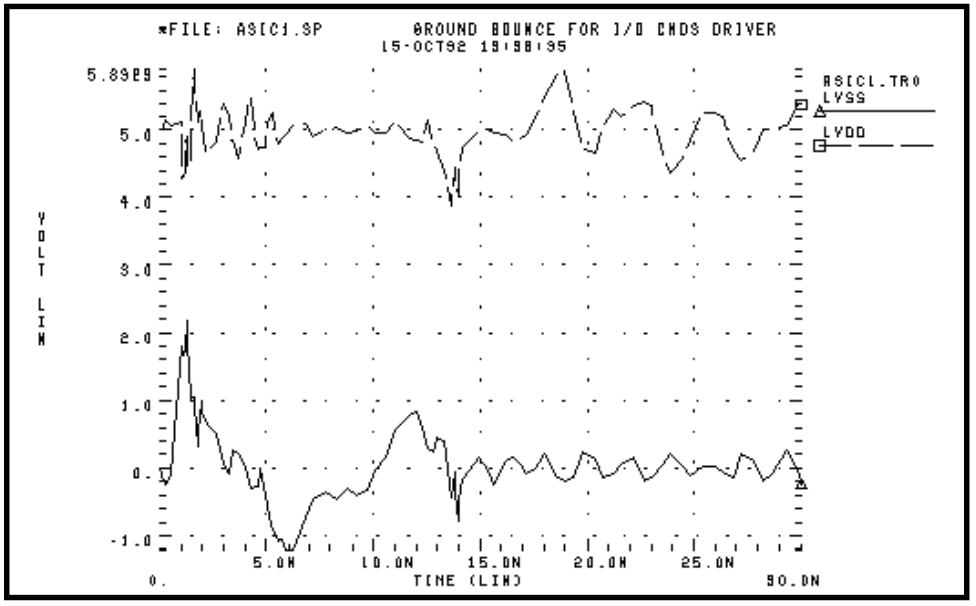

Figure 29-10: Asic1.sp Demo Local Supply Current

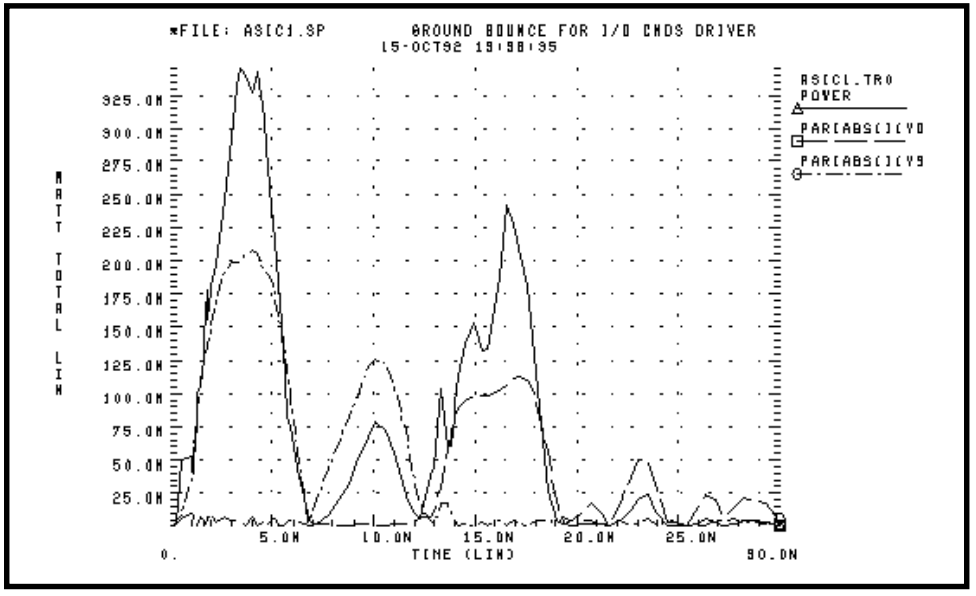

Figure 29-11: Asic1.sp Demo Input and Output Signals

CMOS Output Driver Example Input File

```
* FILE: ASIC1.SP
* SIMULATE AN OUTPUT DRIVER DRIVING 6 INCHES OF 6MIL PRINTED
*    CIRCUIT BOARD COPPER WITH 25PF OF LOAD CAPACITANCE
* MEASURE PEAK TO PEAK GROUND VOLTAGE
* MEASURE MAXIMUM GROUND CURRENT
* MEASURE MAXIMUM SUPPLY CURRENT

GROUND BOUNCE FOR I/O CMOS DRIVER 1200/1.2 & 800/1.2 MICRONS

.OPTIONS POST=2  RELVAR=.05

.TRAN .25N 30N
.MEASURE  IVDD_MAX  MAX PAR('ABS(I(VD))')
.MEASURE  IVSS_MAX  MAX PAR('ABS(I(VS))')
.MEASURE  PEAK_GNDV PP V(LVSS)

.MEASURE  PEAK_IVD   PP PAR(' ABS(I(VD)*V(VDD,OUT)) ')
.MEASURE  PEAK_IVS   PP PAR(' ABS(I(VS)*V(VSS,OUT)) ')
.MEASURE  RMS_POWER RMS POWER

.MEASURE  FALL_TIME TRIG V(IN) RISE=1 VAL=2.5V
+                   TARG V(OUT) FALL=1 VAL=2.5V
.MEASURE  RISE_TIME TRIG V(IN) FALL=1 VAL=2.5V
+                   TARG V(OUT) RISE=1 VAL=2.5V
.MEASURE  TLINE_DLY TRIG V(OUT) RISE=1 VAL=2.5V
+                   TARG V(OUT2) RISE=1 VAL=2.5V
```

Input Signals

```
VIN IN LGND PWL(0N 0V, 2N 5V, 12N 5, 14N 0)

* OUTPUT DRIVER
MP1 LOUT IN LVDD LVDD P W=1400U L=1.2U
MN1 LOUT IN LVSS LVSS N W=800U L=1.2U
xout LOUT OUT LEADFRAME

*POWER AND GROUND LINE PARASITICS
Vd VDD GND 5V
xdd vdd lvdd leadframe
Vs VSS gnd 0v
xss vss lvss leadframe

*OUTPUT LOADING – 3 INCH FR-4 PC BOARD + 5PF LOAD +
*3 INCH FR-4 + 5PF LOAD
```

```
XLOAD1 OUT OUT1  GND LUMP5 LEN=3 WID=.006
CLOAD1 OUT1 GND  5PF
XLOAD2 OUT1 OUT2 GND LUMP5 LEN=3 WID=.006
CLOAD2 OUT2 GND  5PF

.macro leadframe in out
rframe in mid .01
lframe   mid out 10n
cframe   mid gnd .5p
.ends

*Tranmission Line Parameter Definitions
.param rho=.6mho/sq cap=.55nf/in**2 ind=60ph/sq

*The 5-lump macro defines a parameterized transmission line
.macro lump5 in out ref len_lump5=1 wid_lump5=.1
.prot
.param reseff='len_lump5*rho/wid_lump5*5'
+       capeff='len_lump5*wid_lump5*cap/5'
+       indeff='len_lump5*ind/wid_lump5*5'
r1  in  1   reseff
c1   1  ref capeff
l1   1  2   indeff

r2   2  3   reseff
c2   3  ref capeff
l2   3  4   indeff

r3   4  5   reseff
c3   5  ref capeff
l3   5  6   indeff

r4   6  7   reseff
c4   7  ref capeff
l4   7  8   indeff

r5   8  9   reseff
c5   9  ref capeff
l5   9 out  indeff

.unprot
.ends
```

Model Section

```
.MODEL N NMOS LEVEL=3 VTO=0.7 UO=500 KAPPA=.25 ETA=.03
+ THETA=.04 VMAX=2E5 NSUB=9E16 TOX=200E-10 GAMMA=1.5 PB=0.6 +
JS=.1M XJ=0.5U LD=0.0 NFS=1E11 NSS=2E10 capop=4
.MODEL P PMOS LEVEL=3 VTO=-0.8 UO=150 KAPPA=.25 ETA=.03
+ THETA=.04 VMAX=5E4 NSUB=1.8E16 TOX=200E-10 GAMMA=.672
+ PB=0.6 JS=.1M XJ=0.5U LD=0.0 NFS=1E11 NSS=2E10 capop=4
.end
IVDD_MAX        =  0.1141        AT=  1.7226E-08
            FROM=  0.0000E+00    TO=  3.0000E-08
IVSS_MAX        =  0.2086        AT=  3.7743E-09
            FROM=  0.0000E+00    TO=  3.0000E-08
PEAK_GNDV  =  3.221     FROM=  0.0000E+00  TO=  3.0000E-08
PEAK_IVD   =  0.2929    FROM=  0.0000E+00  TO=  3.0000E-08
PEAK_IVS   =  0.3968    FROM=  0.0000E+00  TO=  3.0000E-08
RMS_POWER  =  0.1233    FROM=  0.0000E+00  TO=  3.0000E-08
FALL_TIME  = 1.2366E-09 TARG= 1.9478E-09  TRIG=  7.1121E-10
RISE_TIME  = 9.4211E-10 TARG= 1.4116E-08  TRIG=  1.3173E-08
TLINE_DLY  = 1.6718E-09 TARG= 1.5787E-08  TRIG=  1.4116E-08
```

Running theTemperature Coefficients Demo

SPICE-type simulators do not always automatically compensate for variations in temperature. The simulators make many assumptions that are not valid for all technologies. Star-Hspice has first-order and second-order temperature coefficients in many of the critical model parameters to assure accurate simulations. There are two methods to optimize these temperature coefficients.

The first method uses the DC sweep variable TEMP. All of the Star-Hspice analysis sweeps allow two sweep variables; one of these must be the optimize variable to do an optimization. Sweeping TEMP limits the component to a linear element such as resistor, inductor, or capacitor. The second method uses multiple components at different temperatures.

In the following example, demo file *$installdir/demo/hspice/ciropt/opttemp.sp*, three circuits of a voltage source and a resistor are simulated at -25, 0, and +25 °C from nominal using the DTEMP parameter for element delta temperatures. The resistors share a common model. Three temperatures are necessary to solve a second order equation. This simulation template can be easily extended to a transient simulation of nonlinear components, such as bipolar transistors, diodes, and FETs.

Some simulation shortcuts are used in this example. In the internal output templates for resistors, LV1 (resistor) is the conductance (reciprocal resistance) at the desired temperature, allowing the optimization to be done in the resistance domain. To optimize more complex elements, use the current or voltage domain with measured sweep data. Also, the error function is expecting a sweep on at least two points, requiring the data statement to have two duplicate points.

Optimized Temperature Coefficients Example Input File

```
*FILE OPTTEMP.SP   OPTIMIZE RESISTOR TC1 AND TC2

v-25 1 0 1v
v0   2 0 1v
v+25 3 0 1v

r-25 1 0 rmod dtemp=-25
r0   2 0 rmod dtemp=0
r+25 3 0 rmod dtemp=25
.model rmod R res=1k tc1r=tc1r_opt tc2r=tc2r_opt
```

Optimization Section

```
.model optmod opt
.dc data=RES_TEMP optimize=opt1
+           results=r@temp1,r@temp2,r@temp3
+           model=optmod
.param tc1r_opt=opt1(.001,-.1,.1)
.param tc2r_opt=opt1(1u,-1m,1m)

.meas r@temp1 err2 par(R_meas_t1) par('1.0 / lv1(r-25)')
.meas r@temp2 err2 par(R_meas_t2) par('1.0 / lv1(r0) ')
.meas r@temp3 err2 par(R_meas_t3) par('1.0 / lv1(r+25) ')

* * Output section *
.dc data=RES_TEMP
.print 'r1_diff'=par('1.0/lv1(r-25)')
+      'r2_diff'=par('1.0/lv1(r0)  ')
+      'r3_diff'=par('1.0/lv1(r+25)')

.data RES_TEMP R_meas_t1 R_meas_t2 R_meas_t3
950 1000 1010
950 1000 1010
.enddata
.end
```

Simulating Electrical Measurements

In this example, Star-Hspice simulates the electrical measurements used to characterize devices for data sheet information. The demonstration file for this example is *$installdir/demo/hspice/ddl /t2n2222.sp*. The example automatically includes DDL models by reference using the DDLPATH environment variable, or through the .OPTION SEARCH='path'. It also combines an AC circuit and measurement with a transient circuit and measurement.

The AC circuit measures the maximum Hfe, the small signal common emitter gain. The WHEN option of the .MEASURE statement allows calculation of the unity gain frequency and the phase at the frequency specified with WHEN. In the "Transient Measurements" section of the input file, a segmented transient statement is used to speed up the simulation and compress the output graph. Measurements include:

TURN ON	from 90% of input rising to 90% of output falling
OUTPUT FALL	from 90% to 10% of output falling
TURN OFF	from 10% of input falling to 10% of output rising
OUTPUT RISE	from 10% to 90% of output rising

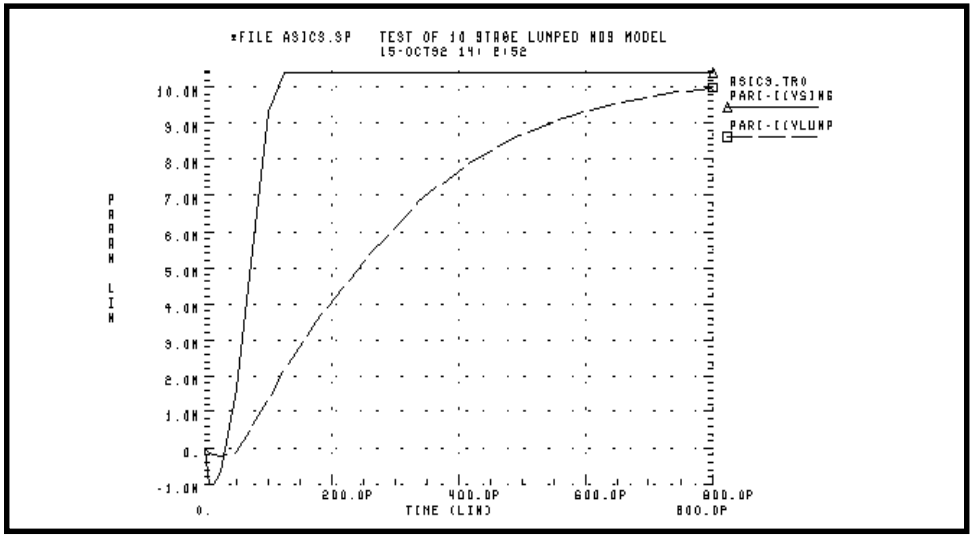

Figure 29-12: – T2N2222 Optimization

T2N2222 Optimization Example Input File

```
* FILE: T2N2222.SP
** assume beta=200 ft250meg at ic=20ma and vce=20v for 2n2222
.OPTION   nopage autostop search=' '
***  ft measurement
*  the net command is automatically reversing the sign of the
*  power supply current for the network calculations
.NET I(vce) IBASE ROUT=50 RIN=50
VCE  C 0 vce
IBASE 0 b   AC=1 DC=ibase
xqft c b 0 t2n2222
.ac dec 10 1 1000meg
.graph s21(m)  h21(m)
.measure 'phase @h21=0db' WHEN h21(db)=0
.measure 'h21_max'  max h21(m)
.measure 'phase @h21=0deg'  FIND h21(p) WHEN h21(db)=0
.param ibase=1e-4  vce=20 tauf=5.5e-10
```

Transient Measurements

```
**   vccf power supply for forward reverse step recovery time
**   vccr power supply for inverse reverse step recovery time
**   VPLUSF  positive voltage for forward pulse generator
**   VPLUSr  positive voltage for reverse pulse generator
**   Vminusf positive voltage for forward pulse generator
**   Vminusr positive voltage for reverse pulse generator
**   rloadf  load resistor for forward
**   rloadr  load resistor for reverse
.param  vccf=30v
.param  VPLUSF=9.9v
.param  VMINUSF=-0.5v
.param  rloadf=200
.TRAN 1N 75N 25N 200N 1N 300N 25N 1200N
.measure 'turn-on time 'trig par('v(inf)-0.9*vplusf') val=0
+  rise=1 targ par('v(outf)-0.9*vccf')  val=0 fall=1
.measure 'fall time 'trig par('v(outf)-0.9*vccf')  val=0
+ fall=1 targ par('v(outf)-0.1*vccf')  val=0 fall=1
.measure 'turn-off time' trig par('v(inf)-0.1*vplusf') val=0
+ fall=1 targ par('v(outf)-0.1*vccf')  val=0 rise=1
.measure 'rise time 'trig par('v(outf)-0.1*vccf')  val=0
+ rise=1 targ par('v(outf)-0.9*vccf')  val=0 rise=1
```

```
.graph V(INF)  V(OUTF)
VCCF    VCCF   0      vccf
RLOADF  VCCF   OUTF   RLOADF
RINF    INF    VBASEF 1000
RPARF   INF    0      58
XSCOPf  OUTF   0      SCOPE
VINF    INF    0      PL    VMINUSF 0S   VMINUSF 5NS
+ VPLUSF  7NS  VPLUSF 207NS  VMINUSF 209NS
* CCX0F    VBASEF  OUTF   CCX0F
* CEX0F    VBASEF  0      CEX0F
XQF      OUTF  VBASEF   0    t2n2222

.MACRO SCOPE  VLOAD VREF
RIN    VLOAD  VREF  100K
CIN    VLOAD  VREF   12P
.EOM
.END
```

Modeling Wide Channel MOS Transistors

Selecting an appropriate model for I/O cell transistors improves the accuracy of simulation. For wide channel devices, model the transistor as a group of transistors connected in parallel with appropriate RC delay networks, rather than as one transistor, because of the delay introduced by the polysilicon gate. When scaling to higher speed technologies, the area of the polysilicon gate decreases, reducing the gate capacitance. However, if you scale the gate oxide thickness, it increases the capacitance per unit area, increasing the RC product. The following example illustrates the effect on delay due to this scaling. For example, for a device with

channel width = 100 microns

channel length = 5 microns

gate oxide thickness = 800 Angstroms

the resulting RC product for the polysilicon gate is

$$Rpoly = \frac{W}{L} \cdot 40$$

$$poly = \frac{Esio \cdot nsi}{tox} \cdot L \cdot W$$

$$Rpoly = \frac{100}{5} \cdot 40 = 800, \quad Co = \frac{3.9 \cdot 8.86}{800} \cdot 100 \cdot 5 = 215\ fF$$

$$RC = 138\ ps$$

For a transistor with

channel width = 100 microns

channel length = 1.2 microns

gate oxide thickness = 250 Angstroms

$$Rpoly = \frac{channel\ \ width}{channel\ \ length} \cdot 40$$

$$Co = \frac{3.9 \cdot 8.86}{Tox} \cdot channel\ \ width \cdot channel\ \ length$$

RC = 546 ps

You can model the RC delay introduced in modern CMOS technologies by using a nine-stage ladder model.

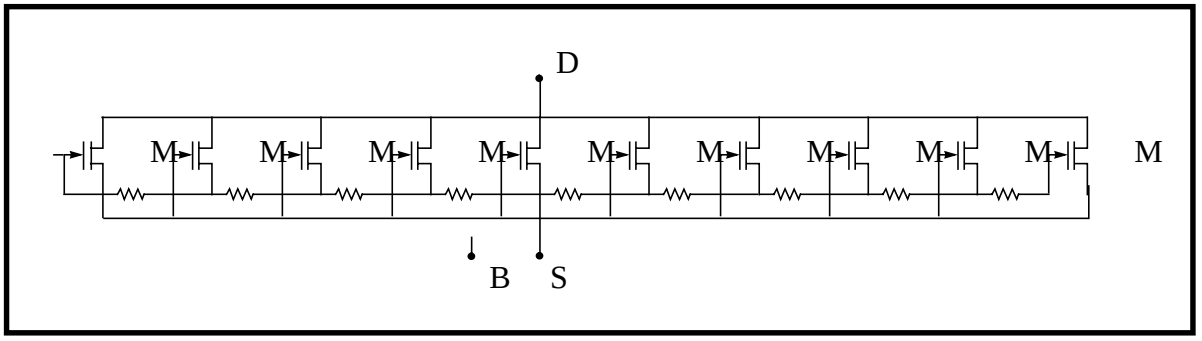

Figure 29-13: Nine-stage Ladder Model

In this example, the nine-stage ladder model was entered into an Star-Hspice data file, *$installdir/demo/hspice/apps /asic3.sp*, and then optimized by Star-Hspice (with actual measured data of a wide channel transistor as the target data). The optimization produced a nine-stage ladder model that matched the timing characteristics of the physical data. The simulation results for the nine-stage ladder model and the one-stage model were then compared using the nine-stage ladder model as the reference. The one-stage model produces results that are about 10% faster than the actual physical data indicates.

Example of 9-Stage Ladder Model

```
* FILE: ASIC3.SP Test of 9 Stage Ladder Model
.subckt lrgtp drain gate source bulk
m1 drain gate source bulk p w='wt/18' l=lt
m2 drain g1 source bulk p w='wt/9' l=lt
m3 drain g2 source bulk p w='wt/9' l=lt
m4 drain g3 source bulk p w='wt/9' l=lt
m5 drain g4 source bulk p w='wt/9' l=lt
m6 drain g5 source bulk p w='wt/9' l=lt
```

```
m7 drain g6 source bulk p w='wt/9' l=lt
m8 drain g7 source bulk p w='wt/9' l=lt
m9 drain g8 source bulk p w='wt/9' l=lt
m10 drain g9 source bulk p w='wt/18' l=lt
r1 gate g1 'wt/lt*rpoly/9'
r2 g1 g2 'wt/lt*rpoly/9'
r3 g2 g3 'wt/lt*rpoly/9'
r4 g3 g4 'wt/lt*rpoly/9'
r5 g4 g5 'wt/lt*rpoly/9'
r6 g5 g6 'wt/lt*rpoly/9'
r7 g6 g7 'wt/lt*rpoly/9'
r8 g7 g8 'wt/lt*rpoly/9'
r9 g8 g9 'wt/lt*rpoly/9'
.ends lrgtp
.end pro
.end
```

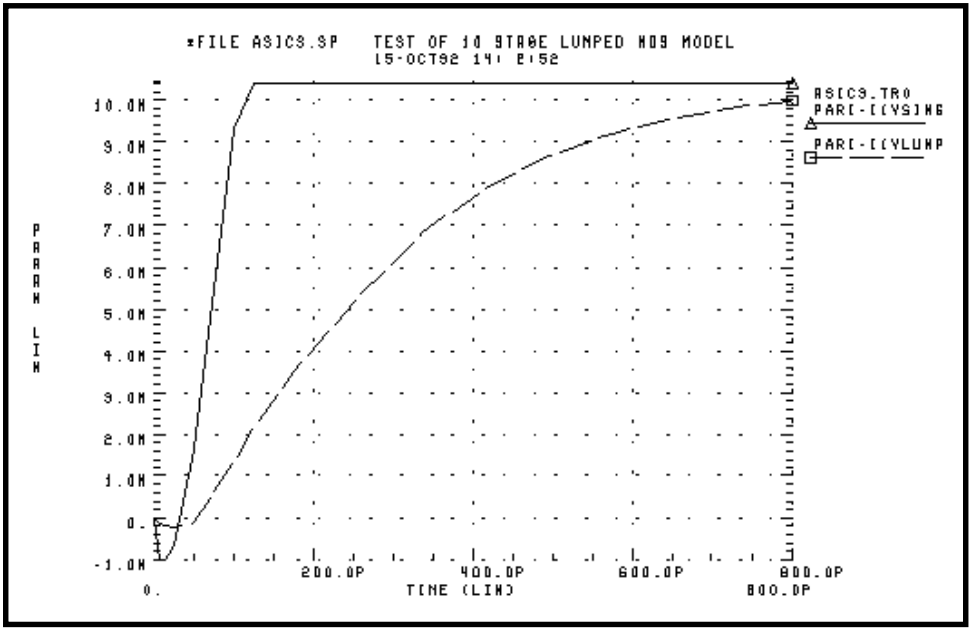

Figure 29-14: – Asic3 Single versus Lumped Model

Examining the Demonstration Input Files

File Name	Description
Algebraic Output Variable Examples *$installdir/demo/hspice/alge*	
alg.sp	demonstration of algebraic parameters
alg_fil.sp	magnitude response of behavioral filter model
alg_vco.sp	voltage controlled oscillator
alg_vf.sp	voltage-to-frequency converter behavioral model
xalg1.sp	QA of parameters
xalg2.sp	QA of parameters
Applications of General Interest *$installdir/demo/hspice/apps*	
alm124.sp	AC, noise, transient op-amp analysis
alter2.sp	.ALTER examples
ampg.sp	pole/zero analysis of a G source amplifier
asic1.sp	ground bounce for I/O CMOS driver
asic3.sp	ten-stage lumped MOS model
bjt2bit.sp	BJT two-bit adder
bjt4bit.sp	four-bit, all NAND gate binary adder
bjtdiff.sp	BJT diff amp with every analysis type
bjtschmt.sp	bipolar Schmidt trigger
bjtsense.sp	bipolar sense amplifier
cellchar.sp	ASIC inverter cell characterization
crystal.sp	crystal oscillator circuit
gaasamp.sp	simple GaAsFET amplifier
grouptim.sp	group time delay example
inv.sp	sweep MOSFET -3 sigma to +3 sigma, use .MEASURE output
mcdiff.sp	CMOS differential amplifier

File Name	Description
mondc_a.sp	Monte Carlo of MOS diffusion and photolithographic effects
mondc_b.sp	Monte Carlo DC analysis
mont1.sp	Monte Carlo Gaussian, uniform, and limit function
mos2bit.sp	two-bit MOS adder
pll.sp	phase locked loop
sclopass.sp	switched capacitor low-pass filter
worst.sp	worst case skew models using .ALTER
xbjt2bit.sp	BJT NAND gate two-bit binary adder
Behavioral Applications	*$installdir/demo/hspice/behave*
acl.sp	acl gate
amp_mod.sp	amplitude modulator with pulse waveform carrier
behave.sp	AND / NAND gates using G, E elements
calg2.sp	voltage variable capacitance
det_dff.sp	double edge triggered flip-flop
diff.sp	differentiator circuit
diode.sp	behavioral diode using a PWL VCCS
dlatch.sp	CMOS D-latch using behaviorals
galg1.sp	sampling a sine wave
idealop.sp	ninth-order low-pass filter
integ.sp	integrator circuit
invb_op.sp	optimization of CMOS macromodel inverter
ivx.sp	characterization of PMOS and NMOS as a switch
op_amp.sp	op-amp from Chua and Lin
pd.sp	phase detector modeled by switches
pdb.sp	phase detector using behavioral NAND gates
pwl10.sp	operational amplifier used as voltage follower

File Name	Description
pwl2.sp	PPW-VCCS with gain of 1 amp / volt
pwl4.sp	eight-input NAND gate
pwl7.sp	modeling inverter by a PWL VCVS
pwl8.sp	smoothing the triangle waveform by PWL CCCS
ring5bm.sp	five-stage ring oscillator – macromodel CMOS inverter
ringb.sp	ring oscillator using behavioral model
sampling.sp	sampling a sine wave
scr.sp	silicon controlled rectifier modelled with PWL CCVS
swcap5.sp	fifth-order elliptic switched capacitor filter
switch.sp	test for PWL switch element
swrc.sp	switched capacitor RC circuit
triode.sp	triode model family of curves using behavioral elements
triodex.sp	triode model family of curves using behavioral elements
tunnel.sp	modeling tunnel diode characteristic by PWL VCCS
vcob.sp	voltage controlled oscillator using PWL functions
Benchmarks	*$installdir/demo/hspice/bench*
bigmos1.sp	large MOS simulation
demo.sp	quick demo file to test installation
m2bit.sp	72-transistor two-bit adder – typical cell simulation
m2bitf.sp	fast simulation example
m2bitsw.sp	fast simulation example – same as m2bitf.sp but using behavioral elements
senseamp.sp	bipolar analog test case
Timing Analysis	*$installdir/demo/hspice/bisect*
fig3a.sp	DFF bisection search for setup time
fig3b.sp	DFF early, optimum, and late setup times
inv_a.sp	inverter bisection pass-fail

File Name	Description
BJT and Diode Devices	*$installdir/demo/hspice/bjt*
bjtbeta.sp	plot BJT beta
bjtft.sp	plot BJT FT using s-parameters
bjtgm.sp	plot BJT Gm, Gpi
dpntun.sp	junction tunnel diode
snaphsp.sp	convert SNAP to Star-Hspice
tun.sp	tunnel oxide diode
Cell Characterization	*$installdir/demo/hspice/cchar*
dff.sp	DFF bisection search for setup time
inv3.sp	inverter characterization
inva.sp	inverter characterization
invb.sp	inverter characterization
load1.sp	inverter sweep, delay versus fanout
setupbsc.sp	setup characterization
setupold.sp	setup characterization
setuppas.sp	setup characterization
sigma.sp	sweep MOSFET -3 sigma to +3 sigma, use measure output
tdgtl.a2d	Viewsim A2D Star-Hspice input file
tdgtl.d2a	Viewsim D2A Star-Hspice input file
tdgtl.sp	two-bit adder using D2A elements
Circuit Optimization	*$installdir/demo/hspice/ciropt*
ampgain.sp	set unity gain frequency of BJT diff pair
ampopt.sp	optimize area, power, speed of MOS amp
asic2.sp	optimize speed, power of CMOS output buffer
asic6.sp	find best width of CMOS input buffer
delayopt.sp	optimize group delay of LCR circuit

File Name	Description
lpopt.sp	match lossy filter to ideal filter
opttemp.sp	find first and second temperature coefficients of resistor
rcopt.sp	optimize speed, power for RC circuit
DDL	*$installdir/demo/hspice/ddl*
ad8bit.sp	eight-bit A / D flash converter
alf155.sp	National JFET op-amp characterization
alf156.sp	National JFET op-amp characterization
alf157.sp	National JFET op-amp characterization
alf255.sp	National JFET op-amp characterization
alf347.sp	National JFET op-amp characterization
alf351.sp	National wide bandwidth JFET input op-amp characterization
alf353.sp	National wide bandwidth dual JFET input op-amp char.
alf355.sp	Motorola JFET op-amp characterization
alf356.sp	Motorola JFET op-amp characterization
alf357.sp	Motorola JFET op-amp characterization
alf3741.sp	
alm101a.sp	
alm107.sp	National op-amp characterization
alm108.sp	National op-amp characterization
alm108a.sp	National op-amp characterization
alm118.sp	National op-amp characterization
alm124.sp	National low power quad op-amp characterization
alm124a.sp	National low power quad op-amp characterization
alm158.sp	National op-amp characterization
alm158a.sp	National op-amp characterization
alm201.sp	LM201 op-amp characterization

File Name	Description
alm201a.sp	LM201 op-amp characterization
alm207.sp	National op-amp characterization
alm208.sp	National op-amp characterization
alm208a.sp	National op-amp characterization
alm224.sp	National op-amp characterization
alm258.sp	National op-amp characterization
alm258a.sp	National op-amp characterization
alm301a.sp	National op-amp characterization
alm307.sp	National op-amp characterization
alm308.sp	National op-amp characterization
alm308a.sp	National op-amp characterization
alm318.sp	National op-amp characterization
alm324.sp	National op-amp characterization
alm358.sp	National op-amp characterization
alm358a.sp	National op-amp characterization
alm725.sp	National op-amp characterization
alm741.sp	National op-amp characterization
alm747.sp	National op-amp characterization
alm747c.sp	National op-amp characterization
alm1458.sp	National dual op-amp characterization
alm1558.sp	National dual op-amp characterization
alm2902.sp	National op-amp characterization
alm2904.sp	National op-amp characterization
amc1458.sp	Motorola internally compensated high performance op-amp characterization
amc1536.sp	Motorola internally compensated high voltage op-amp characterization
amc1741.sp	Motorola internally compensated high performance op-amp characterization

File Name	Description
amc1747.sp	Motorola internally compensated high performance op-amp characterization
ane5534.sp	TI low noise, high speed op-amp characterization
anjm4558.sp	TI dual op-amp characterization
anjm4559.sp	TI dual op-amp characterization
anjm4560.sp	TI dual op-amp characterization
aop04.sp	PMI op-amp characterization
aop07.sp	PMI ultra low offset voltage op-amp characterization
aop14.sp	PMI op-amp characterization
aop15b.sp	PMI precision JFET input op-amp characterization
aop16b.sp	PMI precision JFET input op-amp characterization
at094cns.sp	TI op-amp characterization
atl071c.sp	TI low noise op-amp characterization
atl072c.sp	TI low noise op-amp characterization
atl074c.sp	TI low noise op-amp characterization
atl081c.sp	TI JFET op-amp characterization
atl082c.sp	TI JFET op-amp characterization
atl084c.sp	TI JFET op-amp characterization
atl092cp.sp	TI op-amp characterization
atl094cn.sp	TI op-amp characterization
aupc358.sp	NEC general dual op-amp characterization
aupc1251.sp	NEC general dual op-amp characterization
j2n3330.sp	JFET 2n3330 I-V characteristics
mirf340.sp	IRF340 I-V characteristics
t2n2222.sp	BJT 2n2222 characterization
Device Optimization	*$installdir/demo/hspice/devopt*
beta.sp	Level=2 beta optimization

File Name	Description
bjtopt.sp	s-parameter optimization of 2n6604 BJT
bjtopt1.sp	2n2222 DC optimization
bjtopt2.sp	2n2222 Hfe optimization
d.sp	diode, multiple temperatures
dcopt1.sp	1n3019 diode I-V and C-V optimization
gaas.sp	JFET optimization
jopt.sp	300u / 1u GaAs FET DC optimization
jopt2.sp	JFET optimization
joptac.sp	300u / 1u GaAs FET 40 MHz–20 GHz s-parameter optimization
l3.sp	MOS Level 3 optimization
l3a.sp	MOS Level 3 optimization
l28.sp	Level=28 optimization
ml2opt.sp	MOS Level=2 I-V optimization
ml3opt.sp	MOS Level=3 I-V optimization
ml6opt.sp	MOS Level=6 I-V optimization
ml13opt.sp	MOS Level=13 I-V optimization
opt_bjt.sp	2n3947 forward and reverse Gummel optimization
Fourier Analysis	*$installdir/demo/hspice/fft*
am.sp	FFT analysis, AM source
bart.sp	FFT analysis, Bartlett window
black.sp	FFT analysis, Blackman window
dist.sp	FFT analysis, second harmonic distortion
exam1.sp	FFT analysis, AM source
exam3.sp	FFT analysis, high frequency signal detection test
exam4.sp	FFT analysis, small-signal harmonic distortion test
exp.sp	FFT analysis, exponential source

File Name	Description
fft.sp	FFT analysis, transient, sweeping a resistor
fft1.sp	FFT analysis, transient
fft2.sp	FFT analysis on the product of three waveforms
fft3.sp	FFT analysis, transient, sweeping frequency
fft4.sp	FFT analysis, transient, Monte Carlo Gaussian distribution
fft5.sp	FFT analysis, data-driven transient analysis
fft6.sp	FFT analysis, sinusoidal source
gauss.sp	FFT analysis, Gaussian window
hamm.sp	FFT analysis, Hamming window
hann.sp	FFT analysis, Hanning window
harris.sp	FFT analysis, Blackman-Harris window
intermod.sp	FFT analysis, intermodulation distortion
kaiser.sp	FFT analysis, Kaiser window
mod.sp	FFT analysis, modulated pulse
pulse.sp	FFT analysis, pulse source
pwl.sp	FFT analysis, piecewise linear source
rect.sp	FFT analysis, rectangular window
rectan.sp	FFT analysis, rectangular window
sffm.sp	FFT analysis, single-frequency FM source
sine.sp	FFT analysis, sinusoidal source
swcap5.sp	FFT analysis, fifth-order elliptic switched capacitor filter
tri.sp	FFT analysis, rectangular window
win.sp	FFT analysis, window test
window.sp	FFT analysis, window test
winreal.sp	FFT analysis, window test
Filters	*$installdir/demo/hspice/filters*

File Name	Description
fbp_1.sp	bandpass LCR filter measurement
fbp_2.sp	bandpass LCR filter pole / zero
fbpnet.sp	bandpass LCR filter s-parameters
fbprlc.sp	LCR AC analysis for resonance
fhp4th.sp	high-pass LCR fourth-order Butterworth filter
fkerwin.sp	pole / zero analysis of Kerwin's circuit
flp5th.sp	low-pass fifth-order filter
flp9th.sp	low-pass ninth-order FNDR with ideal op-amps
micro1.sp	test of microstrip
micro2.sp	test of microstrip
tcoax.sp	test of RG58 / AU coax
trans1m.sp	FR-4 printed circuit lumped transmission line
Magnetics	*$installdir/demo/hspice/mag*
aircore.sp	air core transformer circuit
bhloop.sp	b-h loop nonlinear magnetic core transformer
mag2.sp	three primary, two secondary magnetic core transformer
magcore.sp	magnetic core transformer circuit
royerosc.sp	Royer magnetic core oscillator
MOSFET Devices	*$installdir/demo/hspice/mos*
bsim3.sp	Level=47 BSIM3 model
cap13.sp	plot MOS capacitances Level=13 model
cap_b.sp	capacitances for Level=13 model
cap_m.sp	capacitance for Level=13 model
capop0.sp	plot MOS capacitances Level=2
capop1.sp	plot MOS capacitances Level=2
capop2.sp	plot MOS capacitances Level=2

File Name	Description
capop4.sp	plot MOS capacitances Level=6
chrgpump.sp	charge conservation test Level=3
iiplot.sp	impact ionization current plot
ml6fex.sp	plot temperature effects Level=6
ml13fex.sp	plot temperature effects Level=13
ml13ft.sp	s-parameters for Level=13
ml13iv.sp	plot I-V for Level=13
ml27iv.sp	plot I-V for Level=27 SOSFET
mosiv.sp	plot I-V for user include file
mosivcv.sp	plot I-V and C-V for Level=3
qpulse.sp	charge conservation test Level=6
qswitch.sp	charge conservation test Level=6
selector.sp	automatic width and length model selector
tgam2.sp	Level=6 gamma model
tmos34.sp	MOS Level=34 EPFL, test DC
Peripheral Component Interconnect	*$installdir/demo/hspice/pci*
pci_lab.sp	Intel Peripheral Component Interconnect demonstration
pci_mont.sp	PCI Monte Carlo example
pci_wc.sp	PCI worst-case modeling
Radiation Effects	*$installdir/demo/hspice/rad*
brad1.sp	bipolar radiation effects example
brad2.sp	bipolar radiation effects example
brad3.sp	bipolar radiation effects example
brad4.sp	bipolar radiation effects example
brad5.sp	bipolar radiation effects example
brad6.sp	bipolar radiation effects example

File Name	Description
drad1.sp	diode radiation effects example
drad2.sp	diode radiation effects example
drad4.sp	diode radiation effects example
drad5.sp	diode radiation effects example
drad6.sp	diode radiation effects example
dradarb2.sp	diode radiation effects example
jex1.sp	JFET radiation effects example
jex2.sp	JFET radiation effects example
jprad1.sp	JFET radiation effects example
jprad2.sp	JFET radiation effects example
jprad4.sp	JFET radiation effects example
jrad1.sp	JFET radiation effects example
jrad2.sp	JFET radiation effects example
jrad3.sp	JFET radiation effects example
jrad4.sp	JFET radiation effects example
jrad5.sp	JFET radiation effects example
jrad6.sp	JFET radiation effects example
mrad1.sp	MOSFET radiation effects example
mrad2.sp	MOSFET radiation effects example
mrad3.sp	MOSFET radiation effects example
mrad3p.sp	MOSFET radiation effects example
mrad3px.sp	MOSFET radiation effects example
rad1.sp	total MOSFET dose example
rad2.sp	diode photocurrent test circuit
rad3.sp	diode photocurrent test circuit RLEV=3
rad4.sp	diode photocurrent test circuit

File Name	Description
rad5.sp	BJT photocurrent test circuit with an NPN transistor
rad6.sp	BJT secondary photocurrent effect which varies with R1
rad7.sp	BJT RLEV=6 example (semi-empirical model)
rad8.sp	JFET RLEV=1 example with Wirth-Rogers square pulse
rad9.sp	JFET stepwise increasing radiation source
rad10.sp	GaAs RLEV=5 example (semi-empirical model)
rad11.sp	NMOS E-mode Level=8 with Wirth-Rogers square pulse
rad12.sp	NMOS 0.5x resistive voltage divider
rad13.sp	three-input NMOS NAND gate with non-EPI, EPI, and SOS examples
rad14.sp	GaAs differential amplifier circuit
rad14dc.sp	n-channel JFET DC I-V curves
Sources	*$installdir/demo/hspice/sources*
amsrc.sp	amplitude modulation
exp.sp	exponential independent source
pulse.sp	test of pulse
pwl.sp	repeated piecewise linear source
pwl10.sp	op-amp voltage follower
rtest.sp	voltage controlled resistor inverter chain
sffm.sp	single frequency FM modulation source
sin.sp	sinusoidal source waveform
vcr1.sp	switched capacitor network using G-switch
Transmission Lines	*$installdir/demo/hspice/tline*
fr4.sp	microstrip test FR-4 PC board material
fr4o.sp	optimizing model for microstrip FR-4 PC board material
fr4x.sp	FR4 microstrip test
hd.sp	ground bounce for I/O CMOS driver

File Name	Description
rcsnubts.sp	ground bounce for I/O CMOS driver at snubber output
rcsnubtt.sp	ground bounce for I/O CMOS driver
strip1.sp	two series microstrips (8 mil and 16 mil wide)
strip2.sp	two microstrips coupled together
t14p.sp	1400 mil by 140 mil, 50 ohm tline on FR-4 50 MHz - 10.05 GHz
t14xx.sp	1400 mil by 140 mil, 50 ohm tline on FR-4 optimization
t1400.sp	1400 mil by 140 mil, 50 ohm tline on FR-4 optimization
tcoax.sp	RG58/AU coax with 50 ohm termination
tfr4.sp	microstrip test
tfr4o.sp	microstrip test
tl.sp	series source coupled and shunt terminated transmission lines
transmis.sp	algebraics and lumped transmission lines
twin2.sp	twinlead model
xfr4.sp	microstrip test subcircuit expanded
xfr4a.sp	microstrip test subcircuit expanded, larger ground resistance
xfr4b.sp	microstrip test
xulump.sp	test 5-, 20-, and 100-lump U models