Chapter 6

DC Initialization and Point Analysis

This chapter describes DC initialization and operating point analysis. It covers the following topics:

- Understanding the Simulation Flow
- Performing Initialization and Analysis
- Using DC Initialization and Operating Point Statements
- Setting DC Initialization Control Options
- Specifying Accuracy and Convergence
- Reducing DC Errors
- Diagnosing Convergence

Understanding the Simulation Flow

Figure Figure 6-1 illustrates the simulation flow for Star-Hspice.

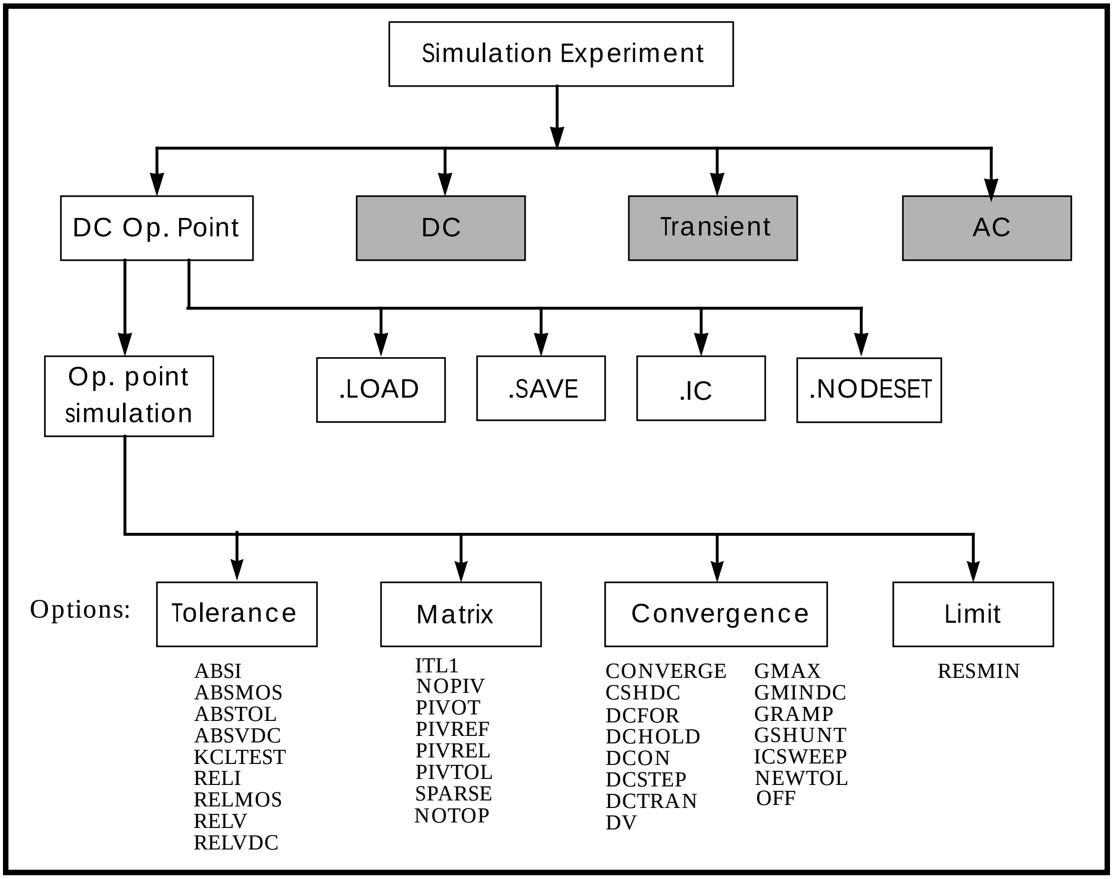

Figure 6-1: DC Initialization and Operating Point Analysis Simulation Flow

Performing Initialization and Analysis

The first task Star-Hspice performs for .OP, .DC sweep, .AC, and .TRAN analyses is to set the DC operating point values for all nodes and sources. It does this either by calculating all of the values or by applying values specified in .NODESET and .IC statements or stored in an initial conditions file. The .OPTIONS OFF statement and the element parameters OFF and IC=val also control initialization.

Initialization is fundamental to the operation of simulation. Star-Hspice starts any analysis with known nodal voltages or initial estimates for unknown voltages and some branch currents, and then iteratively finds the exact solution. Initial estimates close to the exact solution increase the likelihood of a convergent solution and a lower simulation time.

A transient analysis first calculates a DC operating point using the DC equivalent model of the circuit (unless the UIC parameter is specified in the .TRAN statement). The resulting DC operating point is then used as an initial estimate to solve the next timepoint in the transient analysis.

If you do not provide an initial guess, or provide only partial information, Star-Hspice provides a default estimate of each of the nodes in the circuit and then uses this estimate to iteratively find the exact solution. The .NODESET and .IC statements are two methods that supply an initial guess for the exact DC solution of nodes within a circuit. Set any circuit node to any value by using the .NODESET statement. Star-Hspice then connects a voltage source equivalent to each initialized node (a current source with a parallel conductance GMAX set with a .OPTION statement). Next, a DC operating point is calculated with the .NODESET voltage source equivalent connected. Then Star-Hspice disconnects the equivalent voltage sources set with the .NODESET statement and recalculates the DC operating point. This is considered the DC operating point solution.

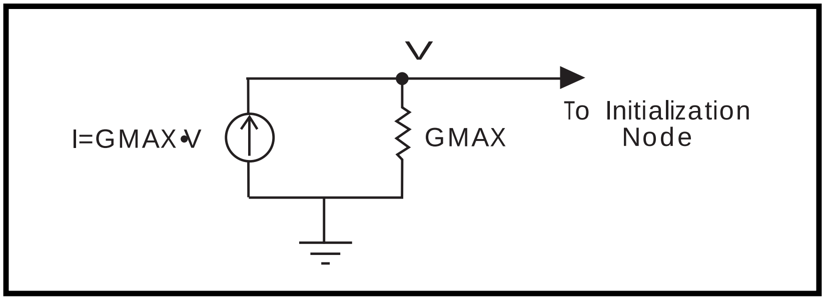

Figure 6-2: Equivalent Voltage Source: NODESET and .IC

Use the .IC statement to provide both an initial guess and final solution to selected nodes within the circuit. Nodes initialized with the .IC statement become part of the solution of the DC operating point.

You can also use the OFF option to initialize active devices. The OFF option works in conjunction with .IC and .NODESET voltages as follows:

1. If any .IC or .NODESET statements exist, node voltages are set according to those statements.
2. If the OFF option is set, the terminal voltages of all active devices (BJT‘s, diodes, MOSFET‘s, JFET‘s, MESFET‘s) that are not set by .IC or .NODESET statements or by sources are set to zero.
3. If any IC parameters are specified in element statements, those initial conditions are set.
4. The resulting voltage settings are used as the initial guess at the operating point.

Use OFF to find an exact solution when performing an operating point analysis in a large circuit, where the majority of device terminals are at zero volts for the operating point solution. You can initialize the terminal voltages for selected active devices to zero by setting the OFF parameter in the element statements for those devices.

After a DC operating point has been found, use the .SAVE statement to store the operating point node voltages in a *<design>.ic* file. Then use the .LOAD statement to restore the operating point values from the *ic* file for subsequent analyses.

Setting Initial Conditions for Transient Analysis

If UIC is included in the .TRAN statement, a transient analysis is started using node voltages specified in a .IC statement.

Use the .OP statement to store an estimate of the DC operating point during a transient analysis.

An “internal timestep too small” error message indicates that the circuit failed to converge. The failure can be due to stated initial conditions that make it impossible to calculate the actual DC operating point.

Using DC Initialization and Operating Point Statements

Element Statement IC Parameter

Use the element statement parameter, IC=<*val*>, to set DC terminal voltages for selected active devices. The value set by IC=<*val*> is used as the DC operating point value, as in the DC solution.

Example

```
HXCC 13 20 VIN1 VIN2 IC=0.5, 1.3
```

The example above describes an H element dependent voltage source with the current through VIN1 initialized to 0.5 mA and the current through VIN2 initialized to 1.3 mA.

.IC and .DCVOLT Initial Condition Statements

The .IC statement or the .DCVOLT statement is used to set transient initial conditions. How it initializes depends upon whether the UIC parameter is included in the .TRAN analysis statement.

When the UIC parameter is specified in the .TRAN statement, Star-Hspice does not calculate the initial DC operating point. In this case, the transient analysis is entered directly. The transient analysis uses the .IC initialization values as part of the solution for timepoint zero (a fixed equivalent voltage source is applied during the calculation of the timepoint zero). The .IC statement is equivalent to specifying the IC parameter on each element statement, but is more convenient. You can still specify the IC parameter, but it does not take precedence over values set in the .IC statement.

When the UIC parameter is *not* specified in the .TRAN statement, the DC operating point solution is computed before the transient analysis. In this case, the node voltages specified in the .IC statement are fixed for the determination of the DC operating point. For the transient analysis, the initialized nodes are released for the calculation of timepoint 0.

Syntax

```
.IC V(node1) = val1 V(node2) = val2 ...
```

or

```
.DCVOLT V(node1) = val1 V(node2) = val2 ...
```

where

val1 ...	specifies voltages. The significance of these specified voltages depends on whether the UIC parameter is specified in the .TRAN statement.
node1 ...	node numbers or node names can include full path names or circuit numbers

Example

```
.IC V(11)=5 V(4)=-5 V(2)=2.2
.DCVOLT 11 5 4 -5 2 2.2
```

.NODESET Statement

.NODESET initializes specified nodal voltages for a DC operating point analysis. The .NODESET statement often is used to correct convergence problems in DC analysis. Setting the nodes in the circuit to values that are close to the actual DC operating point solution enhances the convergence of the simulation. The simulator uses the NODESET voltages for the first iteration only.

Syntax

```
.NODESET V(node1)=val1 <V(node2)=val2 ...>
```

or

```
.NODESET node1 val1 <node2 val2>
```

node1 ...	node numbers or node names can include full path names or circuit numbers

Examples

```
.NODESET V(5:SETX)=3.5V V(X1.X2.VINT)=1V
.NODESET V(12)=4.5 V(4)=2.23
.NODESET 12 4.5 4 2.23 1 1
```

.OP Statement — Operating Point

When an .OP statement is included in an input file, the DC operating point of the circuit is calculated. You can also use the .OP statement to produce an operating point during a transient analysis. Only one .OP statement can appear in a Star-Hspice simulation.

Syntax

```
  .OP <format> <time> <format> <time>
```

format any of the following keywords (only the first letter is required. Default= ALL.)

ALL full operating point, including voltage, currents, conductances, and capacitances. This parameter causes voltage/current output for time specified.

BRIEF produces a one line summary of each element's voltage, current, and power. Current is stated in milliamperes and power in milliwatts.

CURRENT voltage table with element currents and power, a brief summary

DEBUG usually only invoked by the program in the event of a nonconvergent simulation. Debug prints back the nonconvergent nodes with the new voltage, old voltage, and the tolerance (degree of nonconvergence). It also prints back the nonconvergent elements with their tolerance values.

NONE inhibits node and element printouts but allows additional analysis specified to be performed

VOLTAGE voltage table only

Note: The preceding keywords are mutually exclusive; use only one at a time.

time parameter that is placed directly following All, Voltage, Current, or Debug and specifies the time at which the report is printed

Examples

The following example calculates operating point voltages and currents for the DC solution, as well as currents at 10 ns, and voltages at 17.5 ns, 20 ns and 25 ns for the transient analysis.

```
.OP .5NS CUR 10NS VOL 17.5NS 20NS 25NS
```

The following example calculates the complete DC operating point solution. A printout of the solution is shown below.

```
.OP
```

Example Output

```
***** OPERATING POINT INFORMATION     TNOM= 25.000 TEMP=
25.000
***** OPERATING POINT STATUS IS ALL     SIMULATION TIME IS 0.
  NODE     VOLTAGE      NODE     VOLTAGE     NODE    VOLTAGE
+ 0:2    =   0.         0:3   = 437.3258M    0:4  = 455.1343M
+ 0:5    = 478.6763M    0:6   = 496.4858M    0:7  = 537.8452M
+ 0:8    = 555.6659M    0:10  =   5.0000     0:11 = 234.3306M
 **** VOLTAGE SOURCES
SUBCKT
ELEMENT    0:VNCE       0:VN7        0:VPCE       0:VP7
  VOLTS      0.           5.00000     0.           -5.00000
   AMPS     -2.07407U -405.41294P     2.07407U   405.41294P
  POWER      0.          2.02706N     0.            2.02706N
  TOTAL VOLTAGE SOURCE POWER DISSIPATION = 4.0541 N WATTS
**** BIPOLAR JUNCTION TRANSISTORS
SUBCKT
```

```
ELEMENT    0:QN1        0:QN2         0:QN3       0:QN4
MODEL      0:N1         0:N1          0:N1        0:N1
  IB     999.99912N     2.00000U     5.00000U   10.00000U
  IC    -987.65345N    -1.97530U    -4.93827U   -9.87654U
  VBE    437.32588M   455.13437M   478.67632M  496.48580M
  VCE    437.32588M    17.80849M    23.54195M   17.80948M
  VBC    437.32588M   455.13437M   478.67632M  496.48580M
  VS       0.           0.           0.          0.
  POWER    5.39908N   875.09107N     2.27712U    4.78896U
  BETAD-987.65432M -987.65432M  -987.65432M - 987.65432M
  GM       0.           0.           0.          0.
  RPI      2.0810E+06   1.0405E+06 416.20796K  208.10396K
  RX     250.00000M   250.00000M   250.00000M  250.00000M
  RO       2.0810E+06   1.0405E+06 416.20796K  208.10396K
  CPI      1.43092N     1.44033N     1.45279N    1.46225N
  CMU    954.16927P   960.66843P   969.64689P  977.06866P
  CBX      0.           0.           0.          0.
  CCS    800.00000P   800.00000P   800.00000P  800.00000P
  BETAAC   0.           0.           0.          0.
  FT       0.           0.           0.          0.
```

Using .SAVE and .LOAD Statements

Star-Hspice always saves the operating point unless the `.SAVE LEVEL=NONE` statement is used. The saved operating-point file is restored only if the Star-Hspice input file contains a .LOAD statement.

Any node initialization commands, such as .NODESET and .IC, overwrite the initialization done through a .LOAD command if they appear in the netlist after the .LOAD command. This feature helps you to set particular states for multistate circuits such as flip-flops and still take advantage of the .SAVE command to speed up the DC convergence.

.SAVE and .LOAD continues to work even on changed circuit topologies. Adding or deleting nodes results in a new circuit topology. The new nodes are initialized as if no operating point were saved. References to deleted nodes are ignored. The coincidental nodes are initialized to the values saved from the previous run.

When nodes are initialized to voltages, Star-Hspice inserts Norton equivalent circuits at each initialized node. The conductance value of a Norton equivalent circuit is GMAX=100. This conductance value might be too large for some circuits.

If using .SAVE and .LOAD does not speed up the simulation or causes problems with the simulation, you can use .OPTION GMAX=1e-12 to minimize the effect of the Norton equivalent circuits on matrix conductances. Star-Hspice still uses the initialized node voltages for device initialization.

.SAVE Statement

The .SAVE statement stores the operating point of a circuit in a user-specified file. Then you can use the .LOAD statement to input the contents of this file for subsequent simulations to obtain quick DC convergence. The operating point is always saved by default, even if the Star-Hspice input file does not contain a .SAVE statement. To not save the operating point, specify .SAVE LEVEL=NONE.

You can specify that the operating point data be saved as an .IC statement or a .NODESET statement.

Syntax:

```
.SAVE <TYPE=type_keyword> <FILE=save_file>
<LEVEL=level_keyword> <TIME=save_time>
```

where:

type_keyword type of operating point storage desired. The type can be one of the following. Default: NODESET.

.NODESET Stores the operating point as a .NODESET statement. In subsequent simulations, all node voltages are initialized to these values if the .LOAD statement is used. Assuming incremental changes in circuit conditions, DC convergence should be achieved in a few iterations.

	.IC	Causes the operating point to be stored as a .IC statement. In subsequent simulations, node voltages are initialized to these values if .LOAD is included in the netlist file.
save_file	Name of the file in which the DC operating point data is stored. The default is *<design>.ic*.	
level_keyword	Circuit level at which the operating point is saved. The level can be one of the following. Default=ALL.	
	ALL	All nodes from the top to the lowest circuit level are saved. This option provides the greatest improvement in simulation time.
	TOP	Only nodes in the top-level design are saved. No subcircuit nodes are saved.
	NONE	The operating point is not saved.
save_time	Time during transient analysis at which the operating point is saved. A valid transient analysis statement is required to successfully save a DC operating point. Default=0.	

For a parameter or temperature sweep, only the first operating point is saved. For example, if the Star-Hspice input netlist file contains the statement

```
.TEMP -25 0 25
```

the operating point corresponding to .TEMP -25 is saved.

.LOAD Statement

Use the .LOAD statement to input the contents of a file stored with the .SAVE statement. Files stored with the .SAVE statement contain operating point information for the point in the analysis at which the .SAVE was executed.

Do not use the .LOAD command for concatenated netlist files.

Syntax

```
.LOAD <FILE=load_file>
```

load_file name of the file in which an operating point for the circuit under simulation was saved using .SAVE. The default is *<design>.ic*, where *design* is the root name of the design.

Setting DC Initialization Control Options

The DC operating point analysis control options control the DC convergence properties, as well as simulation algorithms. Many of these options also affect transient analysis because DC convergence is an integral part of transient convergence. The absolute and relative voltages, the current tolerances, and the matrix options should be considered for both DC and transient convergence.

Options are specified in .OPTIONS statements. The .OPTIONS statement is discussed in “.OPTIONS Statement” on page 3-45.

The following options are associated with controlling DC operating point analysis. They are described in this section.

ABSTOL
CAPTAB
CSHDC
DCCAP
DCFOR
DCHOLD
DCSTEP
DV
GRAMP
GSHUNT
ICSWEEP
ITL1
KCLTEST
MAXAMP
NEWTOL
NOPIV
OFF
PIVOT
PIVREF
PIVREL
PIVTOL
RESTOL
SPARSE

Some of these options also are used in DC and AC analysis. Many of these options also affect the transient analysis, because DC convergence is an integral part of transient convergence. Transient analysis is discussed in *Chapter 7, Performing Transient Analysis*.

Option Descriptions

ABSTOL=x sets the absolute node voltage error tolerance for DC and transient analysis. Decrease ABSTOL if accuracy is more important than convergence time.

CAPTAB prints table of single plate nodal capacitance for diodes, BJTs, MOSFETs, JFETs and passive capacitors at each operating point.

CSHDC the same option as CSHUNT, but is used only with option CONVERGE.

DCCAP

used to generate C-V plots and to print out the capacitance values of a circuit (both model and element) during a DC analysis. C-V plots are often generated using a DC sweep of the capacitor. Default=0 (off).

DCFOR=x

used in conjunction with the DCHOLD option and the .NODESET statement to enhance the DC convergence properties of a simulation. DCFOR sets the number of iterations that are to be calculated after a circuit converges in the steady state. Since the number of iterations after convergence is usually zero, DCFOR adds iterations (and computational time) to the calculation of the DC circuit solution. DCFOR helps ensure that a circuit has actually, not falsely, converged. Default=0.

DCHOLD=x

DCFOR and DCHOLD are used together for the initialization process of a DC analysis. They enhance the convergence properties of a DC simulation. DCFOR and DCHOLD work together with the .NODESET statement. The DCHOLD option specifies the number of iterations a node is to be held at the voltage values specified by the .NODESET statement. The effects of DCHOLD on convergence differ according to the DCHOLD value and the number of iterations needed to obtain DC convergence. If a circuit converges in the steady state in fewer than DCHOLD iterations, the DC solution includes the values set by the .NODESET statement. However, if the circuit requires more than DCHOLD iterations to converge, the values set in the .NODESET statement are ignored and the DC solution is calculated with the .NODESET fixed source voltages open circuited. Default=1.

DCSTEP=x

used to convert DC model and element capacitors to a conductance to enhance DC convergence properties. The value of the element capacitors are all divided by DCSTEP to obtain a DC conductance model.
Default=0 (seconds).

DV=x

the maximum iteration-to-iteration voltage change for all circuit nodes in both DC and transient analysis. Values of 0.5 to 5.0 can be necessary for some high-gain bipolar amplifiers to achieve a stable DC operating point. CMOS circuits frequently require a value of about 1 volt for large digital circuits. Default=1000 (or 1e6 if DCON=2).

GRAMP=x

value is set by Star-Hspice during the autoconvergence procedure. GRAMP is used in conjunction with the GMINDC convergence control option to find the smallest value of GMINDC that results in DC convergence. GMINDC is described in *Convergence Control Option Descriptions, page -23 in , DC Initialization and Point Analysis*.

GRAMP specifies the conductance range over which GMINDC is to be swept during a DC operating point analysis. Star-Hspice substitutes values of GMINDC over this range and simulates at each value. It then picks the lowest value of GMINDC that resulted in the circuit converging in the steady state.

If GMINDC is swept between 1e-12 mhos (the default) and 1e-6 mhos, GRAMP is set to 6 (the value of the exponent difference between the default and the maximum conductance limit). In this case, GMINDC is first set to 1e-6 mhos, and the circuit is simulated. If convergence is achieved, GMINDC is next set to 1e-7 mhos, and the circuit simulated again. The sweep continues until a simulation has been performed at all values on the GRAMP ramp. If the combined conductance of GMINDC and GRAMP is greater than 1e-3 mho, a false convergence can occur. Default=0.

GSHUNT

conductance added from each node to ground. The default value is zero. Add a small GSHUNT to each node to possibly solve “Timestep too small” problems caused by high frequency oscillations or by numerical noise.

ICSWEEP for a parameter or temperature sweep, saves the results of the current analysis for use as the starting point in the next analysis in the sweep. When ICSWEEP=1, the current results are used in the next analysis. When ICSWEEP=0, the results of the current analysis are not used in the next analysis. Default=1.

ITL1=x sets the maximum DC iteration limit. Increasing this value is unlikely to improve convergence for small circuits. Values as high as 400 have resulted in convergence for certain large circuits with feedback, such as operational amplifiers and sense amplifiers. Something is usually wrong with a model if more than 100 iterations are required for convergence. Set .OPTION ACCT to obtain a listing of how many iterations are required for an operating point. Default=200.

KCLTEST activates the KCL test (Kirchhoff's Current Law) function. This test results in a longer simulation time, especially for large circuits, but provides a very accurate check of the solution. Default=0.

When set to 1, Star-Hspice sets the following options:
RELMOS and ABSMOS options are set to 0 (off).
ABSI is set to 1e-16 A
RELI is set to 1e-6

To satisfy the KCL test, the following condition must be satisfied for each node:

$$\left|\Sigma i_b\right| < RELI \cdot \Sigma\left|i_b\right| + ABSI$$

where the i_bs are the node currents.

MAXAMP=x sets the maximum current through voltage defined branches (voltage sources and inductors). If the current exceeds the MAXAMP value, an error is issued. Default=0.0.

NEWTOL calculates one more iterations past convergence for every DC solution and timepoint circuit solution calculated. When NEWTOL is not set, once convergence is determined, the convergence routine is ended and the next program step begun. Default=0.

NOPIV prevents Star-Hspice from switching automatically to pivoting matrix factorization when a nodal conductance is less than PIVTOL. NOPIV inhibits pivoting. Also see PIVOT.

OFF initializes the terminal voltages of all active devices to zero if they are not initialized to other values. For example, if the drain and source nodes of a transistor are not both initialized using .NODESET or .IC statements or by connecting them to sources, then the OFF option initializes all of the nodes of the transistor to zero. The OFF option is checked before element IC parameters, so if an element IC parameter assignment exists for a particular node, the node is initialized to the element IC parameter value even if it was previously set to zero by the OFF option. (The element parameter OFF can be used to initialize the terminal voltages to zero for particular active devices).

The OFF option is used to help find exact DC operating point solutions for large circuits.

PIVOT=x provides different pivoting algorithm selections. These can be used effectively to reduce simulation time and achieve convergence in circuits that produce hard-to-solve matrix equations. The pivot algorithm is selected by setting PIVOT to one of the following values:

0	Original nonpivoting algorithm
1	Original pivoting algorithm
2	Pick largest pivot in row algorithm

3	Pick best in row algorithm
10	Fast nonpivoting algorithm, more memory required
11	Fast pivoting algorithm, more memory required than for PIVOT values less than 11
12	Pick largest pivot in row algorithm, more memory required than for PIVOT values less than 12
13	Fast best pivot: faster, more memory required than for PIVOT values less than 13

Default=10.

The fastest algorithm is PIVOT=13, which can improve simulation time by up to ten times on very large circuits. However, the PIVOT=13 option requires substantially more memory for the simulation. Some circuits with large conductance ratios, such as switching regulator circuits, might need pivoting. If PIVTOL=0, Star-Hspice automatically changes from nonpivoting to a row pivot strategy upon detection of any diagonal matrix entry less than PIVTOL. This strategy provides the time and memory advantages of nonpivoting inversion, while avoiding unstable simulations and incorrect results. Use .OPTION NOPIV to prevent pivoting from being used under any circumstances.

For very large circuits, PIVOT=10, 11, 12, or 13 can require excessive memory.

If Star-Hspice switches to pivoting during a simulation, the message “pivot change on the fly” is printed, followed by the node numbers causing the problem. Use .OPTION NODE to obtain a node-to-element cross reference.

SPARSE is the same as PIVOT.

PIVREF pivot reference. Used in PIVOT=11, 12, 13 to limit the size of the matrix. Default=1e+8.

PIVREL=x sets the maximum/minimum row/matrix ratio. Use only for PIVOT=1. Large values for PIVREL can result in very long matrix pivot times. If the value is too small, however, no pivoting occurs. It is best to start with small values of PIVREL, using an adequate but not excessive value for convergence and accuracy. Default=1E-20 (max=1e-20, min=1).

PIVTOL=x sets the absolute minimum value for which a matrix entry is accepted as a pivot. PIVTOL is used as the minimum conductance in the matrix when PIVOT=0. Default=1.0e-15.

Note: PIVTOL should always be less than GMIN or GMINDC. Values approaching 1 yield increased pivot.

RESMIN=x specifies the minimum resistance value for all resistors, including parasitic and inductive resistances. Default=1e-5 (ohm). Range: 1e-15 to 10 ohm.

SPARSE=x same as PIVOT

Specifying Accuracy and Convergence

Convergence is defined as the ability to obtain a solution to a set of circuit equations within a given tolerance criteria. In numerical circuit simulation, the designer specifies a relative and absolute accuracy for the circuit solution and the simulator iteration algorithm attempts to converge onto a solution that is within these set tolerances.

Accuracy Tolerances

Star-Hspice uses accuracy tolerance specifications to help assure convergence by determining whether or not to exit the convergence loop. For each iteration of the convergence loop, Star-Hspice takes the value of the previously calculated solution and subtracts it from the present solution, then compares this result with the accuracy tolerances.

$$| Vn^{k} - Vn^{k-1} | <= accuracy\ tolerance$$

where

Vn^{k} is the solution at timepoint n and iteration k

Vn^{k-1} is the solution at timepoint n and iteration k - 1

Absolute and Relative Accuracy Tolerances

As shown in Table 6-1:, Star-Hspice defaults to specific absolute and relative values. You can change these tolerance levels so that simulation time is not excessive and accuracy is not compromised. The options in the table are described in the following section.

Table 6-1: Absolute and Relative Accuracy Tolerances

Type	Option	Default
Nodal Voltage Tolerances	ABSVDC	50 µv
	RELVDC	.001 (.1%)

Table 6-1: Absolute and Relative Accuracy Tolerances

Type	Option	Default
Current Element Tolerances	ABSI	1 nA
	RELI	.01 (1%)
	ABSMOS	1 uA
	RELMOS	.05 (5%)

Nodal voltages and element currents are compared to the values from the previous iteration. If the absolute value of the difference is less than ABSVDC or ABSI, the node or element is considered to be convergent. ABSV and ABSI set the floor value below which values are ignored. Values above the floor use the relative tolerances of RELVDC and RELI. If the iteration-to-iteration absolute difference is less than these tolerances, then it is considered to be convergent. ABSMOS and RELMOS are the tolerances for MOSFET drain currents.

The number of iterations required is directly affected by the value of the accuracy settings. If the accuracy tolerances are tight, a longer time is required to converge. If the accuracy setting is too loose, the resulting solution can be inaccurate and unstable.

Table 6-2: shows an example of the relationship between the RELVDC value and the number of iterations.

Table 6-2: RELV vs. Accuracy and Simulation Time for 2 Bit Adder

RELVDC	Iteration	Delay (ns)	Period (ns)	Fall time (ns)
.001	540	31.746	14.336	1.2797
.005	434	31.202	14.366	1.2743
.01	426	31.202	14.366	1.2724
.02	413	31.202	14.365	1.3433
.05	386	31.203	14.365	1.3315

Table 6-2: RELV vs. Accuracy and Simulation Time for 2 Bit Adder

RELVDC	Iteration	Delay (ns)	Period (ns)	Fall time (ns)
.1	365	31.203	14.363	1.3805
.2	354	31.203	14.363	1.3908
.3	354	31.203	14.363	1.3909
.4	341	31.202	14.363	1.3916
.4	344	31.202	14.362	1.3904

Accuracy Control Options

Star-Hspice is shipped with control option settings designed to maximize accuracy without significantly degrading performance. The options and their settings are discussed in “Testing for Speed, Accuracy and Convergence” on page 7-18.

Convergence Control Option Descriptions

The options listed below are described in this section.

ABSH
ABSI
ABSMOS
ABSVDC
CONVERGE
DCON
DCTRAN
DI
GMAX
GMINDC
RELH
RELI
RELMOS
RELV
RELVDC

ABSH=x sets the absolute current change through voltage defined branches (voltage sources and inductors). In conjunction with DI and RELH, ABSH is used to check for current convergence. Default=0.0.

ABSI=x sets the absolute branch current error tolerance in diodes, BJTs, and JFETs during DC and transient analysis. Decrease ABSI if accuracy is more important than convergence time.

If you want an analysis with currents less than 1 nanoamp, change ABSI to a value at least two orders of magnitude smaller than the minimum expected current.

Default: 1e-9 for KCLTEST=0, 1e-6 for KCLTEST=1

ABSMOS=x current error tolerance used for MOSFET devices in both DC and transient analysis. Star-Hspice uses the ABSMOS setting to determine if the drain-to-source current solution has converged. If the difference between the last and the present iteration's drain-to-source current is less than ABSMOS, or if it is greater than ABSMOS, but the percent change is less than RELMOS, the drain-to-source current is considered converged. Star-Hspice then checks the other accuracy tolerances and, if all indicate convergence, the circuit solution at that timepoint is considered solved, and the next timepoint solution is calculated. For low power circuits, optimization, and single transistor simulations, set ABSMOS=1e-12. Default=1e-6 (amperes).

ABSVDC=x sets the absolute minimum voltage for DC and transient analysis. Decrease ABSVDC if accuracy is of more concern than convergence. If voltages less than 50 microvolts are required, ABSVDC can be reduced to two orders of magnitude less than the smallest desired voltage. This ensures at least two digits of significance. Typically ABSVDC need not be changed unless the circuit is a high voltage circuit. For 1000-volt circuits, a reasonable value can be 5 to 50 millivolts. Default=VNTOL (VNTOL default=50 μV).

CONVERGE invokes different methods for solving nonconvergence problems:

CONVERGE=-1	together with DCON=-1, disables autoconvergence

CONVERGE=1	uses the Damped Pseudeo Transient Algorithm. If the simulation fails to converge within the amount of CPU time set by the CPTIME control option, the simulation halts.
CONVERGE=2	uses a combination of DCSTEP and GMINDC ramping
CONVERGE=3	invokes the source stepping method

Even if it is not set in an .OPTIONS statement, the CONVERGE option is activated in the event of a matrix floating point overflow, or a timestep too small error. Default=0.

In the event of a matrix floating point overflow, Star-Hspice sets CONVERGE=1.

DCON=x In the case of convergence problems, Star-Hspice automatically sets DCON=1 and the following calculations are made:

$$DV = max\left(0.1, \frac{V_{max}}{50}\right), \textit{if } DV = 1000$$

$$GRAMP = max\left(6, \log_{10}\left(\frac{I_{max}}{GMINDC}\right)\right)$$

$$ITL1 = ITL1 + 20 \cdot GRAMP$$

where V_{max} is the maximum voltage and $I_{max}$is the maximum current.

If convergence problems still exist, Star-Hspice sets DCON=2, which is the same as the above except DV=1e6. The above calculations are used for DCON =1 or 2. DCON=1 is automatically invoked if the circuit fails to converge. DCON=2 is invoked if DCON=1 fails.

If the circuit contains uninitialized flip-flops or discontinuous models, the simulation might be unable to converge. Setting DCON=–1 and CONVERGE=–1 disables the autoconvergence algorithm and provides a list of nonconvergent nodes and devices.

DCTRAN

DCTRAN is an alias for CONVERGE. See CONVERGE.

DI=x

sets the maximum iteration to iteration current change through voltage defined branches (voltage sources and inductors). This option is only applicable when the value of the ABSH control option is greater than 0. Default=0.0.

GMAX=x

the conductance in parallel with the current source used for .IC and .NODESET initialization conditions circuitry. Some large bipolar circuits can require GMAX set to 1 for convergence. Default=100 (mho).

GMINDC=x

a conductance that is placed in parallel with all pn junctions and all MOSFET nodes for DC analysis. GMINDC helps overcome DC convergence problems caused by low values of off conductance for pn junctions and MOSFET devices. GRAMP can be used to reduce GMINDC by one order of magnitude for each step. GMINDC can be set between 1e-4 and PIVTOL. Default=1e-12.

Large values of GMINDC can cause unreasonable circuit response. If large values are required for convergence, a bad model or circuit is suspect. In the event of a matrix floating point overflow, if GMINDC is 1.0e-12 or less, Star-Hspice sets it to 1.0e-11.

GMINDC is manipulated by Star-Hspice in autoconverge mode, as described in the “Autoconverge Process” section following.

RELH=x sets relative current tolerance through voltage defined branches (voltage sources and inductors). It is used to check current convergence. This option is applicable only if the value of the ABSH control option is greater than zero. Default=0.05.

RELI=x sets the relative error/tolerance change, in percent, from iteration to iteration to determine convergence for all currents in diode, BJT, and JFET devices. (RELMOS sets the tolerance for MOSFETs). This is the percent change in current from the value calculated at the previous timepoint. Default=1 (0.01%) for KCLTEST=0, 1e-6 for KCLTEST=1.

RELMOS=x sets the relative drain-to-source current error tolerance, in percent, from iteration to iteration to determine convergence for currents in MOSFET devices. (RELI sets the tolerance for other active devices.) This is the percent change in current from the value calculated at the previous timepoint. RELMOS is only considered when the current is greater than the floor value, ABSMOS. Default=5 (0.05%).

RELV=x sets the relative error tolerance for voltages. When voltages or currents exceed their absolute tolerances, the RELV test is used to determine convergence. Increasing RELV increases the relative error. In general, RELV should be left at its default value. RELV controls simulator charge conservation. For voltages, RELV is the same as RELTOL. Default=1e-3.

RELVDC=x sets the relative error tolerance for voltages. When voltages or currents exceed their absolute tolerances, the RELVDC test is used to determine convergence. Increasing RELVDC increases the relative error. In general, RELVDC should be left at its default value. RELVDC controls simulator charge conservation. Default=RELTOL (RELTOL default=1e-3).

Autoconverge Process

If convergence is not achieved in the number of iterations set by ITL1, Star-Hspice initiates an autoconvergence process, in which it manipulates DCON, GRAMP, and GMINDC, as well as CONVERGE in some cases. The autoconverge process is illustrated in Figure 6-3:.

Notes:

1. Setting .OPTIONS DCON=–1 disables steps 2 and 3.
2. Setting .OPTIONS CONVERGE=–1 disables step 4.
3. Setting .OPTIONS DCON=–1 CONVERGE=–1 disables steps 2, 3, and 4.
4. If you set the DV option to a value different from the default value, the value you set for DV is used in step 2, but DV is changed to 1e6 in step 3.
5. Setting GRAMP in a .OPTIONS statement has no effect on the autoconverge process. The autoconverge process sets GRAMP independently.
6. If you specify a value for GMINDC in a .OPTIONS statement, GMINDC is ramped to the value you set instead of to 1e-12 in steps 2 and 3.

DCON and GMINDC

GMINDC is important in stabilizing the circuit during DC operating point analysis. For MOSFETs, GMINDC helps stabilize the device in the vicinity of the threshold region. GMINDC is inserted between drain and bulk, source and bulk, and drain and source. The drain to source GMINDC helps linearize the transition from cutoff to weakly on, helps smooth out model discontinuities, and compensates for the effects of negative conductances.

The pn junction insertion of GMINDC in junction diodes linearizes the low conductance region so that the device behaves like a resistor in the low conductance region. This prevents the occurrence of zero conductance and improves the convergence of the circuit.

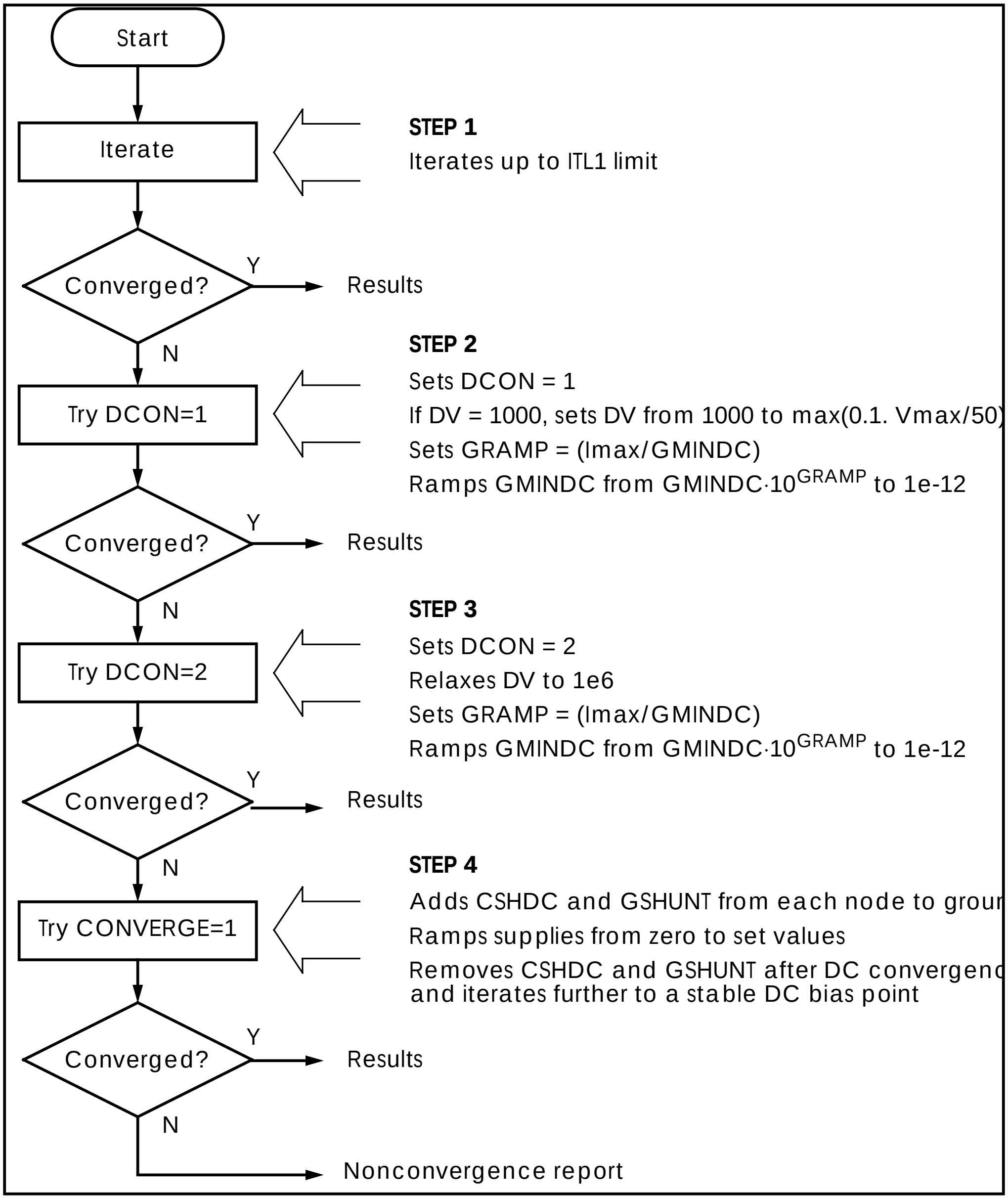
Start
Iterate
STEP 1
Iterates up to ITL1 limit
Converged?
Y
Results
N
STEP 2
Try DCON=1
Sets DCON = 1
If DV = 1000, sets DV from 1000 to max(0.1. Vmax/50)
Sets GRAMP = (Imax/GMINDC)
Ramps GMINDC from GMINDC·10^{GRAMP} to 1e-12
Converged?
Y
Results
N
STEP 3
Try DCON=2
Sets DCON = 2
Relaxes DV to 1e6
Sets GRAMP = (Imax/GMINDC)
Ramps GMINDC from GMINDC·10^{GRAMP} to 1e-12
Converged?
Y
Results
N
STEP 4
Try CONVERGE=1
Adds CSHDC and GSHUNT from each node to grour
Ramps supplies from zero to set values
Removes CSHDC and GSHUNT after DC convergenc
and iterates further to a stable DC bias point
Converged?
Y
Results
N
Nonconvergence report

Figure 6-3: Autoconvergence Process Flow Diagram

DCON is an option that Star-Hspice sets automatically in case of nonconvergence. It invokes the GMINDC ramping process in steps 2 and 3 in Figure 6-3:. GMINDC is shown for various elements in Figure 6-4:.

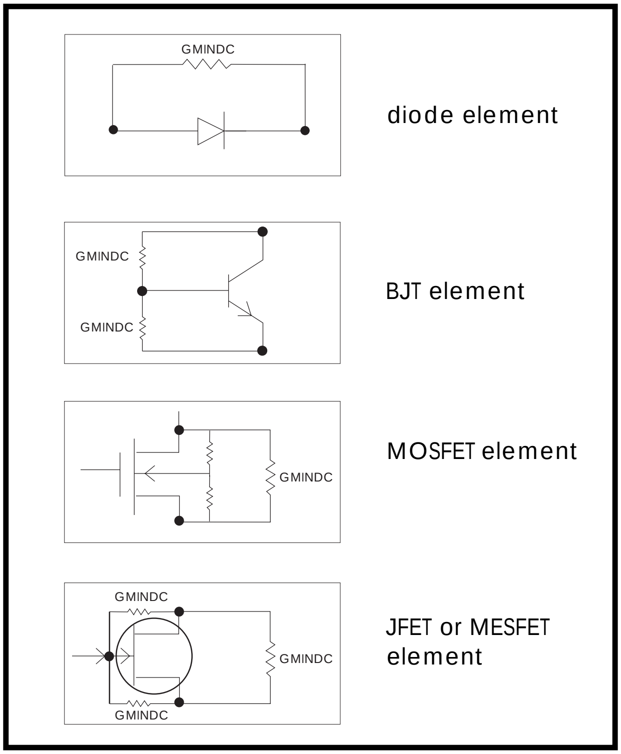

Figure 6-4: GMINDC Insertion

Reducing DC Errors

You can reduce DC errors by performing the following steps.

1. Check topology, set .OPTION NODE to get a nodal cross reference listing if you are in doubt.

   Are all MOS p-channel substrates connected to VCC or positive supplies?

   Are all MOS n-channel substrates connected to GND or negative supplies?

   Are all vertical NPN substrates connected to GND or negative supplies?

   Are all lateral PNP substrates connected to negative supplies?

   Do all latches have either an OFF transistor or a .NODESET or an .IC on one side?

   Do all series capacitors have a parallel resistance, or is .OPTION DCSTEP set?

2. Check your .MODEL statements.

   Be sure to check your model parameter units. Use model printouts to verify actual values and units, since some model parameters are multiplied by scaling options.

   Do MOS models have subthreshold parameters set (NFS=1e11 for SPICE models 1, 2, and 3 and N0=1.0 for Star-Hspice models BSIM1, BSIM2, and Level 28)?

   Avoid setting UTRA in MOS Level 2 models.

   Are JS and JSW set in MOS model for DC portion of diode model? A typical JS value is 1e-4A/M^2.

   Are CJ and CJSW set in MOS diode model?

   Do JFET and MESFET models have weak inversion NG and ND set?

   If MOS Level 6 LGAMMA equation is used, is UPDATE=1?

   DIODE models should have nonzero values for saturation current, junction capacitance, and series resistance.

Use MOS ACM=1, ACM=2, or ACM=3 source and drain diode calculations to automatically generate parasitics.

3. General remarks:

   Ideal current sources require large values of .OPTION GRAMP, especially for BJT and MESFET circuits because they do not ramp up with the supply voltages and can force reverse bias conditions, leading to excessive nodal voltages.

   Schmitt triggers are unpredictable for DC sweep and sometimes for operating points for the same reasons oscillators and flip-flops are. Use slow transient.

   Large circuits tend to have more convergence problems because they have a higher probability of uncovering a modeling problem.

   Circuits that converge individually and fail when combined are almost guaranteed to have a modeling problem.

   Open loop op-amps have high gain, which can lead to difficulties in converging. Start op-amps in unity gain configuration and open them up in transient analysis with a voltage-variable resistor or a resistor with a large AC value for AC analysis.

4. Check your options:

   Remove all convergence-related options and try first with no special options settings.

   Check nonconvergence diagnostic tables for nonconvergent nodes. Look up nonconvergent nodes in the circuit schematic. They are generally latches, Schmitt triggers, or oscillating nodes.

   For stubborn convergence failures, bypass DC altogether with .TRAN with UIC set. Continue transient analysis until transients settle out, then specify .OP time to obtain an operating point during the transient analysis. An AC analysis also can be specified during the transient analysis by adding an .AC statement to the .OP time statement.

   SCALE and SCALM scaling options have a significant effect on the element and model parameter values. Be careful with units.

Shorted Element Nodes

Star-Hspice disregards any capacitor, resistor, inductor, diode, BJT, or MOSFET that has all its leads connected together. The component is not counted in the component tally Star-Hspice produces. Star-Hspice issues the following warning:

```
** warning ** all nodes of element x:<name> are connected
together
```

Conductance Insertion Using DCSTEP

In a DC operating point analysis, failure to include conductances in a capacitor model results in broken circuit loops (since a DC analysis opens all capacitors), which might not be solvable. By including a small conductance in the capacitor model, the circuit loops are complete and can be solved.

Modeling capacitors as complete opens often results in the following error message:

> “No DC Path to Ground”

For a DC analysis, .OPTION DCSTEP is used to give a conductance value to all capacitors in the circuit. DCSTEP calculates the value as follows:

> conductance = capacitance/DCSTEP

Figure 6-5: illustrates how Star-Hspice inserts conductance G in parallel with capacitance Cg to provide current paths around capacitances in DC analysis.

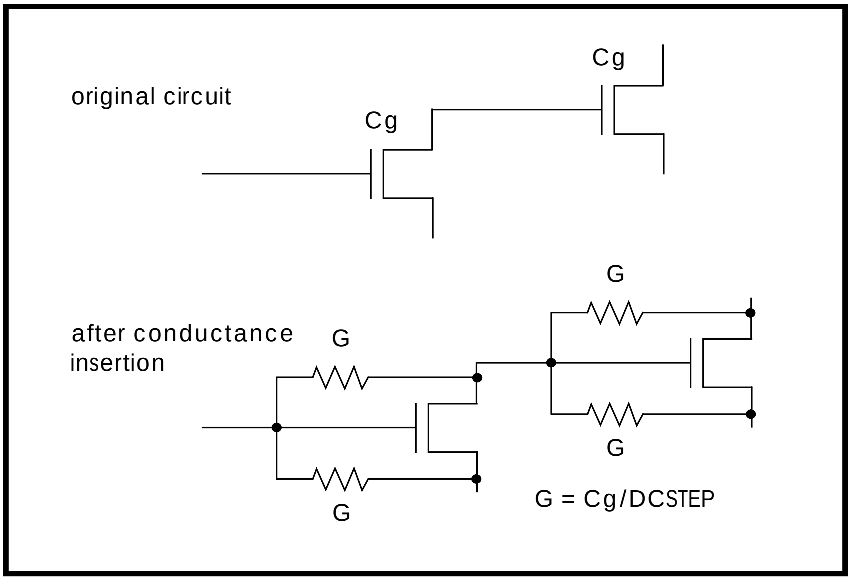

Figure 6-5: Conductance Insertion

Floating Point Overflow

Negative or zero MOS conductance sometimes results in Star-Hspice having difficulty converging. An indication of this type of problem is a floating point overflow during matrix solutions. Star-Hspice detects floating point overflow and invokes the Damped Pseudo Transient algorithm (CONVERGE=1) to try to achieve DC convergence without requiring user intervention. If GMINDC is 1.0e-12 or less when a floating point overflow occurs, Star-Hspice sets it to 1.0e-11.

Diagnosing Convergence

Before simulation, Star-Hspice diagnoses potential convergence problems in the input circuit, and provides an early warning to help debugging. When a circuit condition that indicates possible convergence problems is detected, Star-Hspice prints the following message into the output file:

```
“Warning: Zero diagonal value detected at node ( ) in
equation solver, which might cause convergence problems. If
your simulation fails, try adding a large resistor between
node ( ) and ground.”
```

Nonconvergence Diagnostic Table

Two automatic printouts are generated when nonconvergence is encountered: the nodal voltage printout and the element printout (the diagnostic tables). The nodal voltage printout prints all nonconvergent node voltage names and the associated voltage error tolerances (tol). The element printout lists all nonconvergent elements, along with their associated element currents, element voltages, model parameters, and current error tolerances (tol).

To locate the branch current or nodal voltage resulting in nonconvergence, analyze the diagnostic tables for unusually large values of branch currents, nodal voltages or tolerances. Once located, initialize the node or branch using the .NODESET or .IC statements. The nonconvergence diagnostic table is automatically generated when a circuit simulation has not converged, indicating the quantity of recorded voltage failures and the quantity of recorded branch element failures. A voltage failure can be generated by any node in the circuit, including “hidden” nodes, such as the extra nodes created by parasitic resistors.

The element printout lists the subcircuit, model name, and element name of all parts of the circuit having nonconvergent nodal voltages or currents. Table 6-3: identifies the inverters, xinv21, xinv22, xinv23, and xinv24 as problem subcircuits of a ring oscillator. It also indicates that the p-channel transistor of subcircuits xinv21, xinv22, xinv24 are nonconvergent elements. The n-channel transistor of xinv23 is also a nonconvergent element. The table gives the voltages and currents of the transistors, so the designer can quickly check to see if they are of a reasonable value. The tolds, tolbd, and tolbs error tolerances indicate how close the element currents (drain to source, bulk to drain, and bulk to source) were to a convergent solution. For tol variables, a value close to or below 1.0 indicates a convergent solution. As shown in Table 6-3:, the tol values in the order of 100 indicate the currents were far from convergence. The element current and voltage values are also given (id, ibs, ibd, vgs, vds, and vbs). These values can be examined for realistic values and determination of the transistor regions of operation.

Table 6-3: Voltages, Currents, and Tolerances for Subcircuits

subckt element model	xinv21 21:mphc1 0:p1	xinv22 22:mphc1 0:p1	xinv23 23:mphc1 0:p1	xinv23 23:mnch1 0:n1	xinv24 24: mphc1 0:p1
id	27.5809f	140.5646u	1.8123p	1.7017m	5.5132u
ibs	205.9804f	3.1881f	31.2989f	0.	200.0000f
ibd	0.	0.	0.	-168.7011f	0.
vgs	4.9994	-4.9992	69.9223	4.9998	-67.8955
vds	4.9994	206.6633u	69.9225	-64.9225	2.0269
vbs	4.9994	206.6633u	69.9225	0.	2.0269
vth	-653.8030m	-745.5860m	-732.8632m	549.4114m	-656.5097m
tolds	114.8609	82.5624	155.9508	104.5004	5.3653
tolbd	0.	0.	0.	0.	0.
tolbs	3.534e-19	107.1528m	0.	0.	0.

Traceback of Nonconvergence Source

To locate a nonconvergence source, trace the circuit path for error tolerance. In an inverter chain, for example, the last inverter can have a very high error tolerance. If this is the case, the error tolerance of the elements driving the inverter should be examined. If the driving tolerance is high, the driving element could be the source of nonconvergence. However, if the tolerance is low, the driven element should be checked as the source of nonconvergence.

By examining the voltages and current levels of a nonconvergent MOSFET, you can discover the operating region of the MOSFET. This information can flow to the location of the discontinuity in the model, for example, subthreshold-to-linear or linear-to-saturation.

When considering error tolerances, check the current and nodal voltage values. If the current or nodal voltage values are extremely low, nonconvergence errors can be induced because a relatively large number is being divided by a very small number. This results in nonconvergence because the calculation produces a large result. A solution is to increase the value of the absolute accuracy options.

Use the diagnostic table in conjunction with the DC iteration limit (ITL1 statement) to find the sources of nonconvergence. By increasing or decreasing ITL1, output for the problem nodes and elements for a new iteration is printed—that is, the last iteration of the analysis set by ITL1.

Solutions for Nonconvergent Circuits

Nonconvergent circuits generally result from:

- Poor initial conditions
- Inappropriate model parameters
- PN junctions

These conditions are discussed in the following sections.

Poor Initial Conditions

Multistable circuits need state information to guide the DC solution. You must initialize ring oscillators and flip-flops. These multistable circuits either give the intermediate forbidden state or cause a DC convergence problem. Initialize a circuit using the .IC statement to force a node to the requested voltage. Ring oscillators usually need only one stage set.

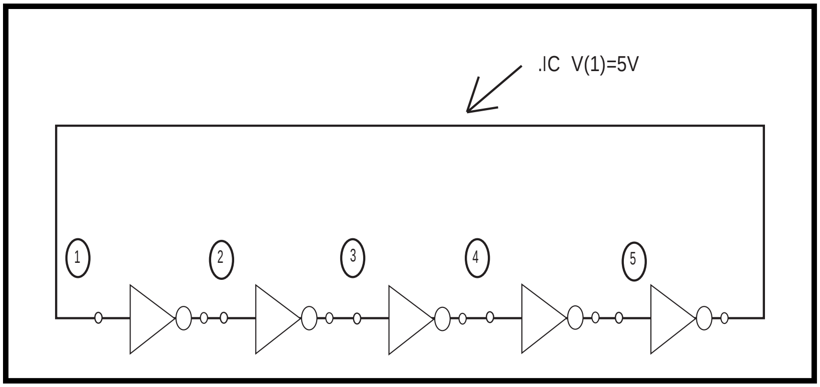

Figure 6-6: Ring Oscillator

It is best to set up the flip-flop with an .IC statement inside the subcircuit definition. In the following example, a local parameter “Qset” is set to 0. It is used as the value for the .IC statement to initialize the latch output node “Q”. This results in all latches having a default state of “Q” low. This state is overridden by the call to a latch by setting “Qset” to vdd.

Example

```
.subckt latch in Q Q/ d Qset=0
.ic Q=Qset
...
.ends
.Xff data_in[1] out[1] out[1]/ strobe LATCH Qset=vdd
```

Inappropriate Model Parameters

It is possible to create a discontinuous IDS or capacitance model by imposing nonphysical model parameters. This can cause an “internal timestep too small” error during the transient simulation. The demonstration file *mosivcv.sp* shows IDS, VGS, GM, GDS, GMB, and CV plots for MOS devices. A sweep near threshold from Vth–0.5 V to Vth+0.5 V using a delta of 0.01 V sometimes discloses a possible discontinuity in the curves.

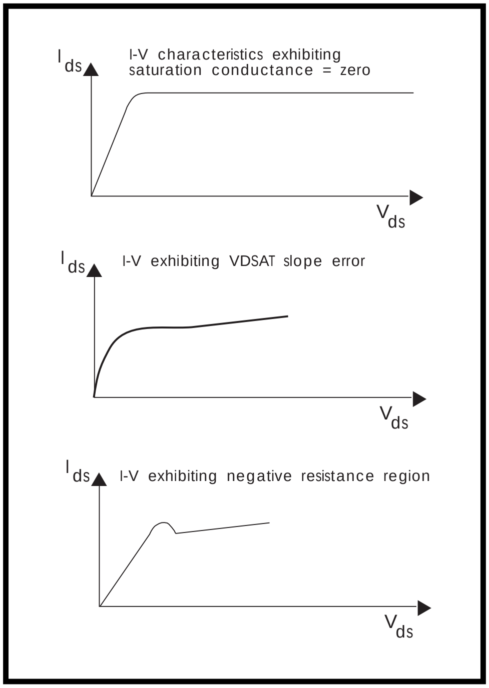

Figure 6-7: Discontinuous I-V Characteristics

If the simulation no longer converges when a component is added or a component value is changed, the model parameters are inappropriate or do not correspond to the physical values they represent. Check the Star-Hspice input netlist file for nonconvergent elements. Devices with a “TOL” greater than 1 are nonconvergent. Find the devices at the beginning of the combined logic string of gates that seem to start the nonconvergent string. Check the operating point of these devices very closely to see what region they operate in. The model parameters associated with this region are most likely inappropriate.

Circuit simulation is based on using single-transistor characterization to simulate a large collection of devices. If a circuit fails to converge, it can be caused by a single transistor somewhere in the circuit.

PN Junctions (Diodes, MOSFETs, BJTs)

PN junctions found in diode, BJT, and MOSFET models can exhibit nonconvergent behavior in both DC and transient analysis. For example, PN junctions often have a high off resistance, resulting in an ill-conditioned matrix. To overcome this, the options GMINDC and GMIN automatically parallel every PN junction in a design with a conductance. Nonconvergence can occur by overdriving the PN junction. This happens when a current-limiting resistor is omitted or has a very small value. In transient analysis, protection diodes often are temporarily forward biased (due to the inductive switching effect), overdriving the diode and resulting in nonconvergence if a current-limiting resistor is omitted.