Low-Voltage Pipeline A/D Converter

by

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

LOW-VOLTAGE PIPELINE A/D CONVERTER

1. INTRODUCTION

1.1. Motivation of the Project

There are three driving forces for low-voltage analog circuits. The first is the increasing density of components on a chip. A silicon chip can only dissipate a limited amount of power mainly due to the package heat limitation. Since the density and chip area of analog and digital circuits are increasing, the power must be lowered in proportion. In digital circuits reducing the power supply leads to lower power dissipation since power consumption is proportional to the square of the supply voltage according to the equation $P = CV^2f$. In analog circuits, however, this relation does not necessarily hold true. To compensate the reduced signal swing to achieve the same dynamic range (DR), power consumption sometimes even increases under the lower supply voltage [3]. But as a part of a mixed signal system and acting as the interface between the real analog world and the digital signal processor, analog circuits such as filters, A/D and D/A converters, etc. have to be integrated with digital blocks and operate under the same low supply voltage.

The second reason is the wide emerging market for portable electronic systems such as wireless communication devices, consumer electronics, hearing aids, etc. calls for low voltage operation and low power consumption. Low voltage is desirable so that we can use as few batteries as possible for size and weight consideration. Low power is necessary to extend the battery life.

The third and the most critical reason is the continuous scaling down of the digital process. As the channel length is scaled down, the gate oxide thickness must be scaled also. For device reliability reasons, the supply voltage needs to be reduced to ensure gate oxide integrity over time and prevent p-n junction from breakdown. Present-day CMOS processes are making the transition from 3.3 V to 1.8 V supplies. One forecast made by Semiconductor Industry Association (SIA) in

1997 predicts that circuits will need to operate under 1.5 V and below within a decade. [1]

Switched-capacitor (SC) technique is one of the most important methods to build analog circuit due to its sample-hold (S/H) functionality and good linearity. SC technique is widely used in the design of precision filters, sigma-delta modulators, and other kinds of A/D converters such as pipeline, successive-approximation (SAR) ADC, etc. Under low-voltage conditions, SC circuits will encounter a severe switch-driving problem. The low supply voltage does not allow enough overdrive to turn on the transistors used as switches to sample the signal. Currently there are three solutions to this problem. They are: 1. Low threshold voltage process; 2. Bootstrapped clock signals; 3. Switched opamps. All above methods have their limitations either in terms of cost, reliability or speed.

In this project, we will use a new scheme for the low-voltage SC circuit. No special process or multiplied voltage is needed. The opamp will never be switched off, so this solution can achieve high speed. In order to verify the speed advantage of the new scheme, a 10-bit 20 MS/s pipeline A/D converter with a 1.5 V voltage supply is built.

The design is based on transistor models of Lucent 0.25μm 3.3 V CMOS process. The main technology parameters for minimum channel transistors are shown in Table 1.1.

V_{Tn}	0.55 V	K_n	59 $\mu A/V^2$
V_{Tp}	-0.90 V	K_p	39 $\mu A/V^2$

TABLE 1.1: Lucent 0.25μm CMOS process parameters

1.2. Thesis Organization

The thesis is organized into five chapters:

Chapter 1 introduces the problem.

Chapter 2 contains a brief overview of available low-voltage SC techniques. Three different methods together with their drawbacks will be illustrated in Section 2.1. The new scheme is introduced in Section 2.2.

Chapter 3 deals with the pipeline A/D converter. In Section 3.1, several different high-speed A/D converters are outlined. The general architecture for the pipeline ADC is presented. In Section 3.2, the low-voltage version of pipeline ADC based on the new SC circuitry will be proposed. The special issues in the new structure will be discussed in detail in Section 3.3.

Chapter 4 describes the key circuit blocks used in the ADC. Among them are the operational amplifier, comparator, input stage, clock generator and digital correction block. Transistor-level simulation and the layout floorplan will be presented.

Chapter 5 points out the potential problems which could degrade the speed and accuracy performance of the converter and some possible remedies. Future work is suggested to improve the current design.

2. LOW-VOLTAGE SC TECHNIQUES

The integrator and gain stage shown in Fig. 2.1 are two basic SC building blocks. Integrators are often used in SC filters and sigma-delta modulators, while the gain stages are usually used in the sample-hold (S/H) and interstage signal processing blocks of multi-step ADC.

There are two categories of switches in the SC circuits. One contains switches (S2, S3 and S4) that have one terminal fixed to a reference level Vref or virtual Vref. Another contains switches (S1) that have to operate in the entire signal range, which are typically at the outputs of opamps. The former ones can always be turned on if we choose ground (in the following text we use gnd to stand for ground) or Vcc (in the following text we sometimes use Vdd) as the reference voltage. The minimum power supply required for these switches is the transistor threshold voltage plus certain overdrive margin. The switches in the second category are the ones which will cause trouble. Under low-voltage conditions, the traditionally used transmission gates (complementary switches) will be ineffective.

Fig. 2.2 shows the conductance of a switch in on-state versus input signal V_i for three different supply voltages. The dashed line shows the individual conductances of the NMOS and PMOS devices, and the solid line shows the combined conductance. In the first case, where V_{dd} is much larger than $V_{tn} + V_{tp}$, it is easy for V_i to achieve a large on-conductance from rail to rail. In the second case, where V_{dd} is comparable to $V_{tn} + V_{tp}$, there is a substantial drop in conductance when V_i approaches $V_{dd}/2$. In the last case, where V_{dd} is less than $V_{tn} + V_{tp}$, there is a range of V_i where the switches will not conduct. In this case, although we can use the reduced signal range near ground or V_{dd}, in order to achieve the same dynamic range much larger sampling capacitor need to be used due to kT/C noise consideration. This is not practical for the high-speed applications. The other reason to avoid doing this is that the range near the supply voltage is not the optimal operation range for the output of amplifier. The DC gain decreases drastically and will cause severe nonideality for some applications such as pipeline ADC which is sensitive to the finite gain of the opamp.

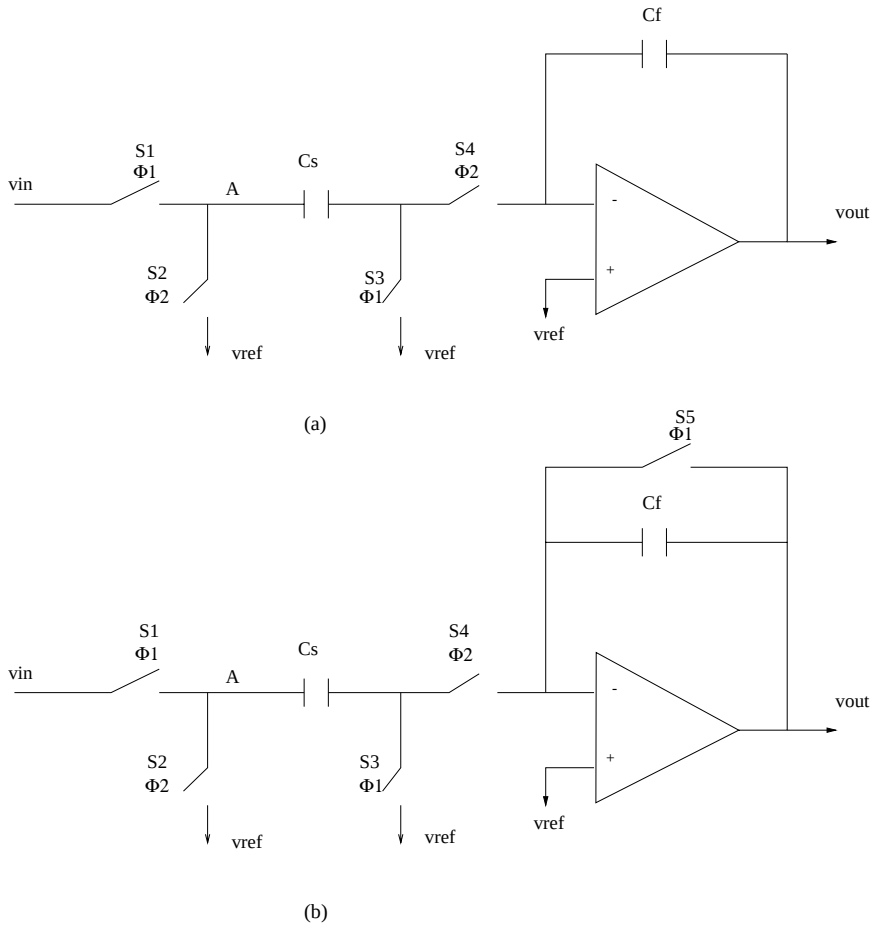

FIGURE 2.1: SC building blocks: (a) SC integator (b) SC gain stage

2.1. Conventional Low-Voltage SC Techniques

There exist three approaches to address the switch overdrive problem:

- Multi-threshold process

  Special doping process can be used to reduce the threshold voltage of either NMOS or PMOS transistors such that at a level $V_{dd}/2$ one of the devices will be on. This solution is at the expense of a few extra mask steps in the process, which are not available in typical digital CMOS process. Higher cost is the main concern of this solution. Another drawback of the

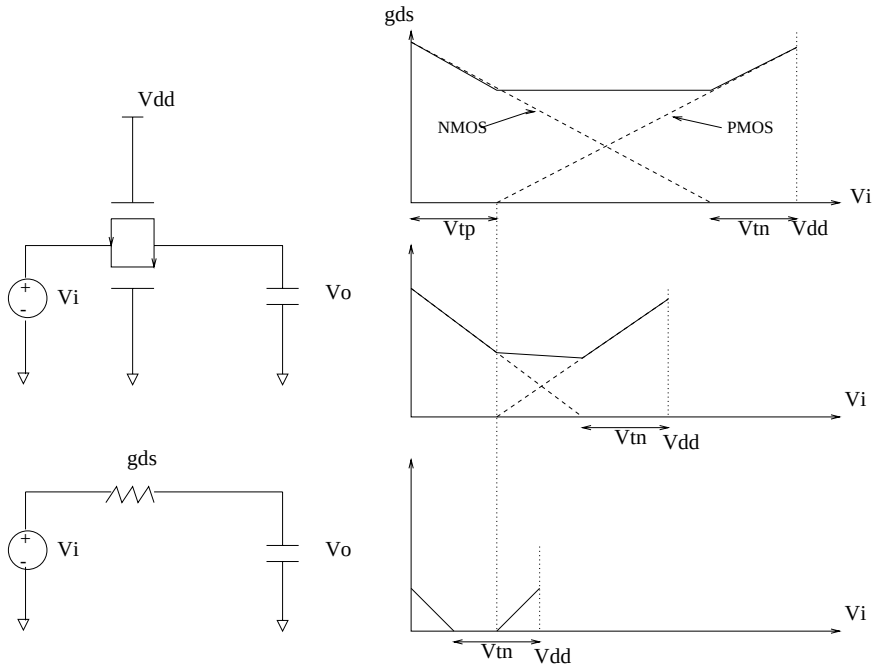

FIGURE 2.2: Switch conductance under different supply voltage

low-threshold devices is the increased leakage current. This will limit the resolution of SC circuits whose operation is based on charge conservation.

- Clock-boosting technique

  Instead of reducing V_{tn} or V_{tp}, this approach tries to increase V_{dd}. One option is to increase the supply voltage globally by a DC-DC converter. In the strict sense this is not a low-voltage design any more. Since the bottleneck under low-voltage conditions is only the switches which sample the input signals, we can boost the clock signals applied to these switches individually. This option minimizes the part of circuit operating at a higher voltage.

  The commonly used clock boosting circuit is shown in Fig. 2.3 [19]. By applying a input clock signal with an amplitude of V_{dd}, the capacitors C1 and C2 are alternatively charged to V_{dd} through the cross-coupled NMOS transistors. When the input clock is low, an inverted clock will pump the voltage at the top terminal of C2 to be near the double of V_{dd} and the PMOS device M1 will be ”on” to pass the boosted voltage to the gates of the sampling NMOS switches. When the input clock is high, switch M2 pulls the gates of sampling switches down

to ground. The peak voltage of the output clock signal is determined by

$$V_{HI} = 2V_{dd}\frac{C2}{C2 + C_p + C_{G,switch}} \tag{2.1}$$

Here, C_p is the parasitic capacitance at the top plate of C2, and $C_{G,switch}$ is the gate capacitance of the sampling switches. To avoid latch-up, the n-well potential of the PMOS M1 needs to be higher than $V_{HI} - V_{pn}$. A separate high voltage generator may be needed to provide this bias.

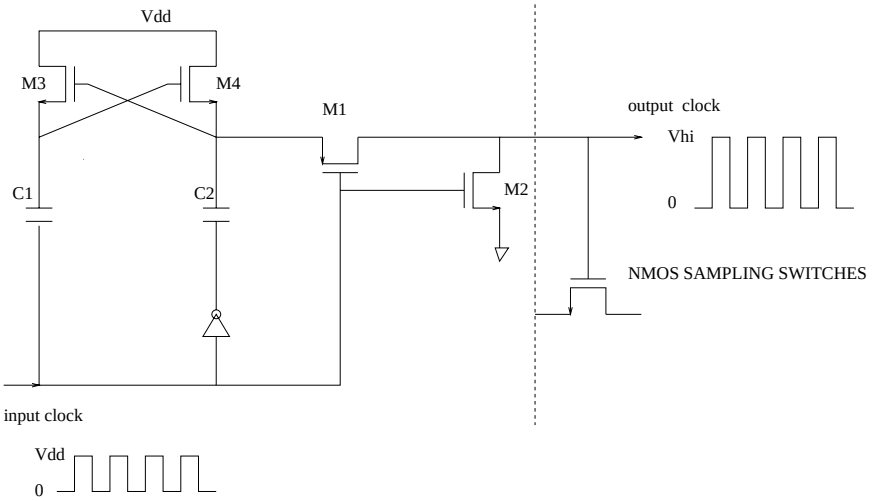

FIGURE 2.3: Schematic of clock-boosting (version 1)

Another scheme shown conceptually in Fig. 2.4 can generate a boosted clock with constant Vgs for all levels of Vin. This has two advantages over the previous scheme. One is that the constant R_{on} due to the fixed Vgs makes the time constant $R_{on}C$ independent of the input signal. This will decrease the harmonic distortion when in high-speed application. The fixed Vgs also eliminates the high gate oxide voltage when the input signal is low. This is beneficial to the reliability issues which we will discuss later.

The problems with clock-boosting approach are many:

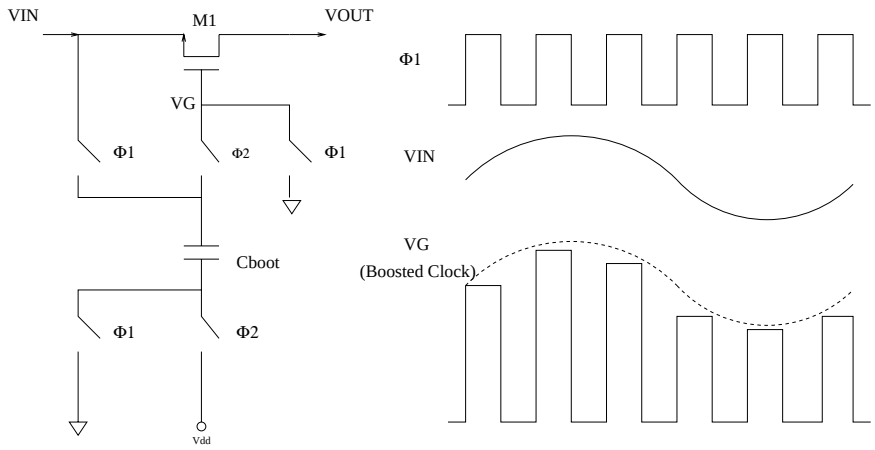

FIGURE 2.4: Schematic of clock-boosting (version 2)

1. Extra hardware. In high-precision SC circuits, a four-phase clock scheme is usually used to reduce signal-dependent charge injections. This means that at least four clock boosting circuits are needed. In order to avoid the crosstalk between different sampling switches and to reduce the loading of clock-boosting circuit, more generators are needed.

2. A boosted clock will unavoidably increase the switching noise of the circuit, which is harmful for the noise-sensitive analog blocks.

3. The most important issue is about long-term reliability. With the physical feature of transistors scaled down, the rated supply voltage decreases accordingly to assure a long circuit lifetime. There are several mechanisms of device breakdown which can cause CMOS circuit failure. Among them are oxide breakdown, gate-induced drain leakage, hot-electron effects and punch-through [2]. If the critical terminal voltages V_{gs}, V_{gd} and V_{ds} are kept within the rated operating voltage V_{dd} for certain technology, device reliability can be assured. The boosted clock strategy violates this criterion, and will hence reduce the circuit lifetime. A recent paper [5] describes a clock boosting scheme conceptually similar to Fig. 2.4 for low-voltage pipeline ADC design. Although the devices are not subject to large terminal voltages as in Fig. 2.3, transient reliability problems still exist.

- Switched-opamp technique

  The two approaches described above try to increase the conductance of sampling switches. Switched-opamp technique tackles the problem in another way. It eliminates the sampling switches altogether. The input signal (or the output signal from the previous stages) is connected to the sampling capacitor directly. As shown in Fig. 2.5, the circuit operates as follows: in phase1, the output from the previous stage is valid and is sampled by Cs by closing S3. In phase2, switch S2 connects to ground and the charge in Cs transfers to the feedback capacitor Cf. In this phase, both the opamp output of the prior stage and ground are connected to node A. This two signals will conflict with each other and there will be a significant current flowing into switch S2. This causes node A not to be reset to ground accurately. To overcome this problem, the opamp in previous stage need to be switched off in phase2 so that its output impedance is high.

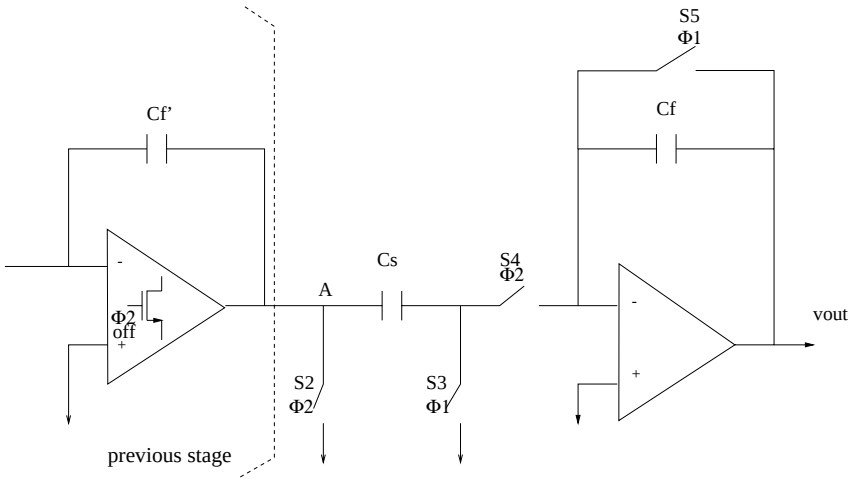

FIGURE 2.5: Switched-opamp SC

A switchable opamp is shown in Fig. 2.6 [8]. It is a Miller-compensated OTA with two added switches. The OTA is turned on and off by means of its bias current. In the off phase, transistor M10 pulls the Vgs of top current mirrors to zero. M9 is used to interrupt the current path through M7, so that the Miller compensation capacitor Cc will not be discharged. Otherwise, from the off-phase to the on-phase, long time would be needed to recharge Cc.

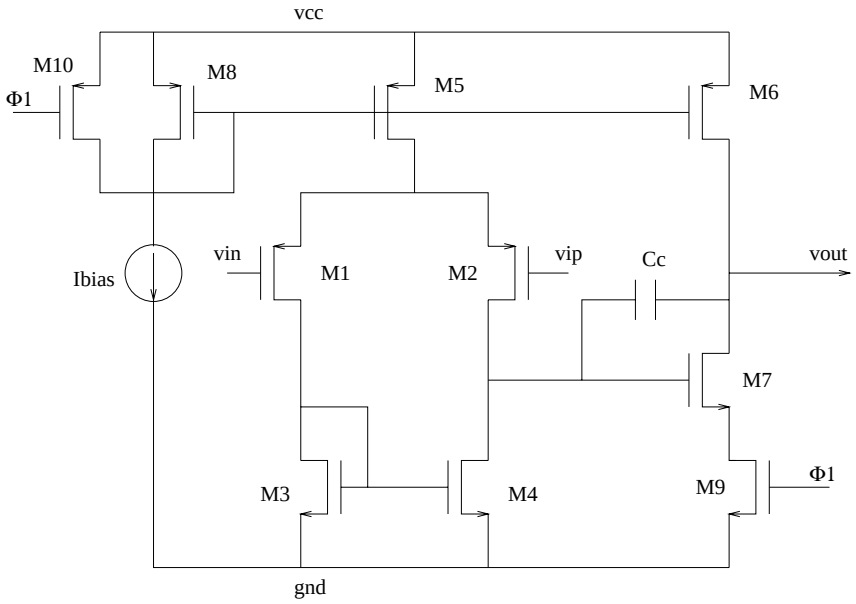

FIGURE 2.6: Switchable opamp

The switched-opamp technique has shown promising performance in applications such as voice-band and audio-band SC filters and sigma-delta modulators [6] [7]. But for higher sampling rate($> 10MHz$) , this technique is too slow. This is due to the fact that extra time is needed for the opamp to recover from its switched-off state to the active state. Although there are some improved schemes that are proposed which only switch off the opamp partially, instead of the whole bias, the speed problem has not been solved completely.

2.2. A New Low-Voltage SC Technique

Eliminating the sampling switches, such as used in the switched-opamp scheme, makes the special process to lower the device threshold or the special circuits to boost the sampling clock unnecessary. The drawback caused by slow recovery time can be overcome by allowing the opamp to remain active in both clock phases. Thus the opamp will never be switched off, and high speed can

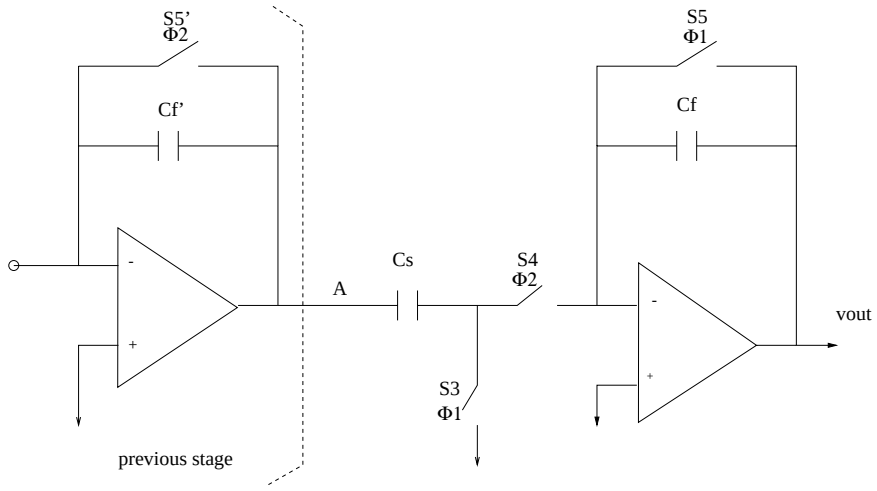

FIGURE 2.7: A new scheme for a low-voltage SC gain stage

be achieved.

A new low-voltage SC scheme is shown in Fig. 2.7 [9] [10]. As in the switched-opamp schemes, the input sampling switch S1 is omitted and the bottom plate of sampling capacitor Cs is connected directly to the output of previous stage. This solves the overdrive problem when S3 samples the input signal in phase1. The difference from the switched-opamp structure is that in the new scheme the grounding sampling switch S2 is also eliminated. In phase2, instead of connecting node A to ground with switch S2 and switch off the opamp so there is no signal conflict, in the new scheme the switch S5' connects the output of opamp with its inverting input to configure it as a unity-gain buffer. Node A is set to the virtual ground in phase2 without switching off the opamp. In the new scheme all switches are tied to ground or Vdd. So the minimum supply voltage needed for the proper operation of switches is the threshold voltage plus the overdrive margin. The inputs of the opamp is near ground so the supply needed for the proper operation of opamp is minimized.

This architecture was first suggested by Maloberti [9] for reducing the offset and 1/f noise in SC filters. Low-voltage SC integrators using this structure were described in [10]. In the integrator conceptually shown in Fig. 2.8, switch S6 is added so that in phase1 the integrating capacitor Cf stores the information from the previous phase, instead of being reset by switch S5. One problem encountered is that in phase1 the voltage of node B may be lower than ground due to the negative

vout drop. It will cause the pn junction of switch S6 to be forward biased. The resulting leakage current violates the charge conservation, and greatly degrades the accuracy of the performance. Extra circuits are needed to address this problem at the expense of complicated switching or clock scheme and speed penalty [10]. Fortunately, the gain stage shown in Fig. 2.7, which is used in interstage signal processing in multi-step A/D converters, does not encounter this problem.

One point which needs to be mentioned is that although the new scheme is expected to be much faster than the switched-opamp version, the speed performance will not be as good as the traditional SC scheme due to the fact that in phase2 there are two settling events happening at the same time: the opamp of previous stage settles to gnd, and the current stage output settles to the desired value. But the total settling time is far less than the sum of two settling times, and the speed advantage over the switched-opamp is significant.

A high-speed medium-resolution pipeline ADC was designed based on this scheme to verify the speed advantage. Detailed discussion will be given in the next chapter.

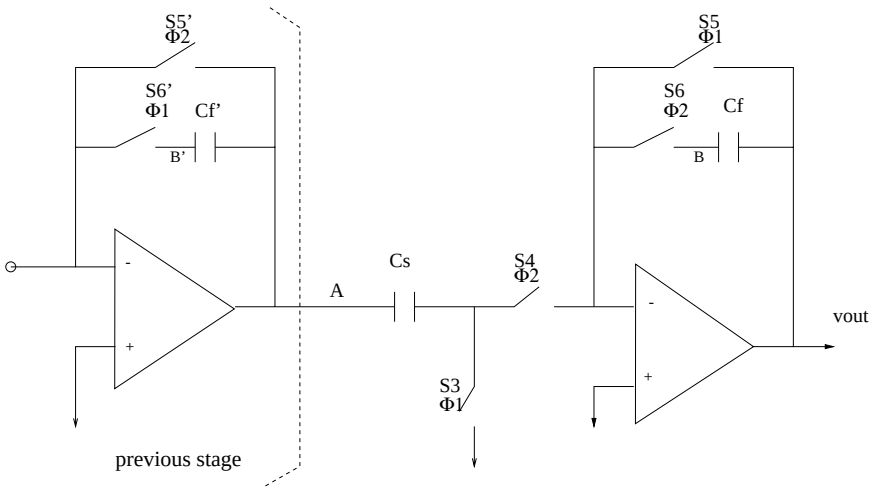

FIGURE 2.8: A new scheme for a low-voltage SC integrator

3. LOW-VOLTAGE PIPELINE ADC

3.1. High-Speed A/D Converters

For video-band ($> 10\ MHz$) medium resolution ($8 \sim 10$ bits) applications, there are several different approaches to implement the A/D converter. Full flash ADC is the most straightforward way. It needs $2^n - 1$ comparators to compare the input signal with $2^n - 1$ reference voltages usually generated by a resistor string. The chip size and power dissipation grow exponentially with the increase of number of bits. It makes this structure impractical for a resolution higher than 8 bits. The offset of comparators caused by the mismatch of devices limits the static accuracy of the converter, and the input capacitance limits the bandwidth of input signal.

Two-step ADCs divide the converter into two stages. The coarse conversion stage generates the most significant bits (MSBs). The interstage block converts the MSBs into an analog signal and subtracts it from input signal. The error signal goes to the fine conversion stage and the least significant bits (LSBs) are generated. In this structure, each conversion stage consists of a flash ADC and the total number of comparator is reduced to the order of $2^{n/2+1}$. The reduced hardware is at the expense of increased conversion time and latency.

Unlike the two-step ADC, the folding and interpolating ADC generates the MSBs and LSBs simultaneously. Analog continuous-time pre-processing by folding the input signal into a smaller region replaces the interstage discrete-time signal processing. No opamp is used in closed-loop configuration at high speed. This structure can achieve the same conversion rate and latency time as a full flash ADC with less hardware and lower power dissipation. The drawback is that the internal signal frequency is higher than the input signal frequency by the folding factor. This limits the input signal bandwidth.

The pipeline ADC is the extension of the two-step structure. The conversion is divided into several stages with each stage generating a certain number of digital bits. The general block diagram is shown in Fig. 3.1. There are M stages and the *ith* stage generates m_i digits. If no redundancy is used, the sum of m_i equals to N, the resolution of ADC. The stages perform the following functions: the sample-hold circuits sample the output from the previous stage; the sub-ADC converts the analog signal into m_i digital bits; the sub-DAC generates the estimated analog input signal; the subtraction and multiplication circuits generate the error signal between the input and the estimated signal and multiply it into the full scale. This residue signal goes to the next stage. All stages operate concurrently. When a stage works on the current sample, the next stage processes the previous one. The nature of concurrence makes the throughput of the converter independent of its resolution, and the same as for a flash ADC. Compared to the flash structure, the hardware increases linearly with the increase of resolution. The disadvantage of this structure is the large latency time between valid digital output and the analog input signal. In some applications, such as data recovery in the Local Area Network (LAN) and disk drive read/write channels, the ADC is inside a feedback loop. Excessive latency will make the loop unstable. For most video applications, latency is not an issue.

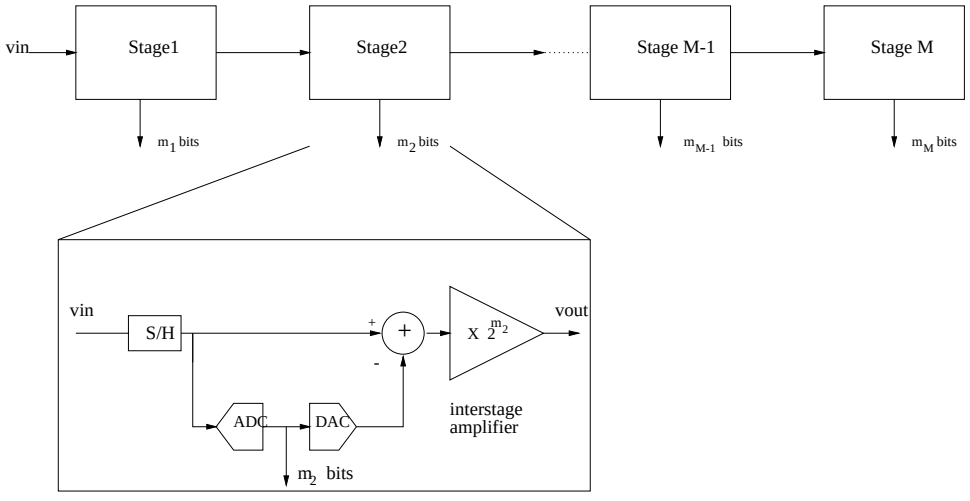

FIGURE 3.1: General pipeline ADC block diagram

3.2. Pipeline A/D Converter

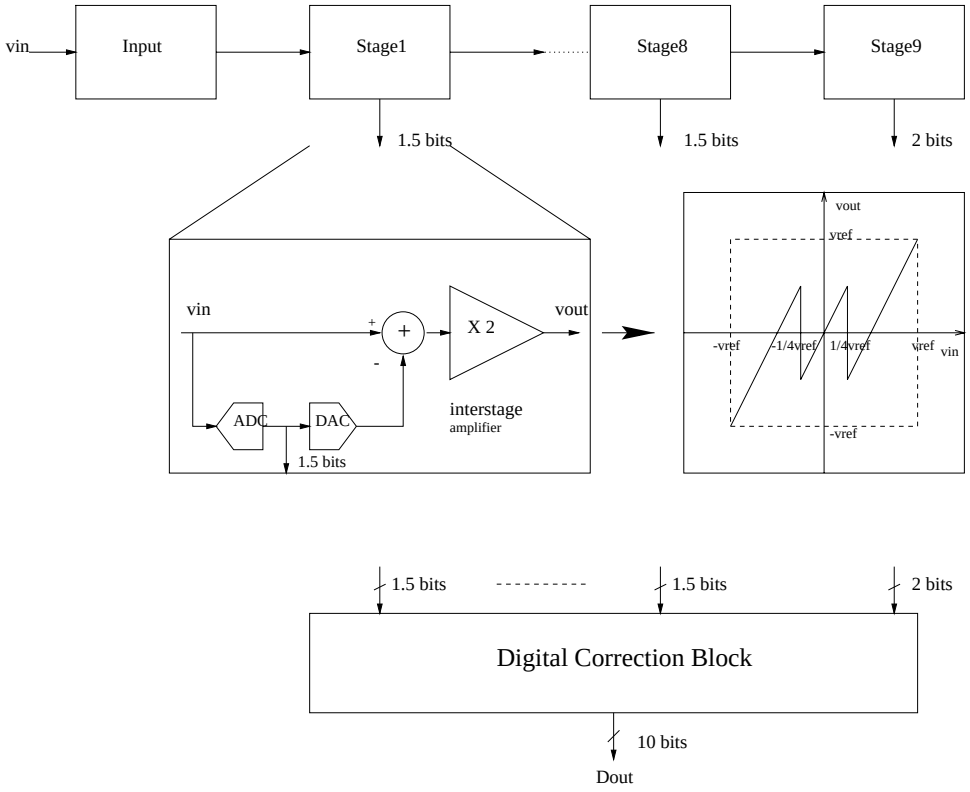

FIGURE 3.2: Pipeline ADC 1.5-bit/stage structure

The diagram of the pipeline ADC used in this project is shown in Fig. 3.2. [11] It consists of 9 cascaded stages together with the input stage, which is needed specially for this low-voltage scheme. Stage1 through stage8 are identical; each performs a coarse 1.5-bit quantization, a D/A function on the quantization results, subtraction and amplification of the remainder. The residue generated will be sampled and processed by the next stage, such that the A/D conversion is operated concurrently. The last stage is a 2-bit A/D converter. The 2 bits from all stages (1.5 effective bits for the first 8 stages and 2 true bits for the last stage) are collected by the digital correction block to produce a 10-bit digital representation of analog signal. The adjacent stages operate in opposite phases. The conversion rate is 1 clock cycle per sample and the latency time is about 5 clock cycles.

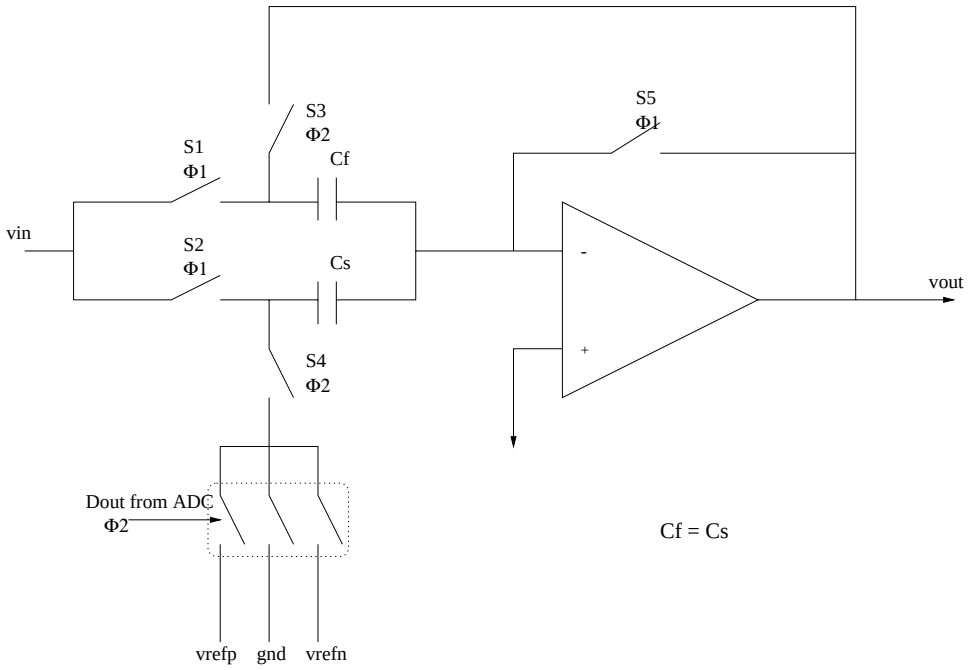

FIGURE 3.3: Conventional MDAC

There are two converter blocks inside each stage: one is a coarse ADC and the other is a multiplying DAC(MDAC). Due to the interstage gain and the digital correction algorithm, the resolution of the ADC is determined by the resolution of each stage. It is chosen to be 1.5-bit per stage based on the following reasons:

1. This maximizes the closed-loop bandwidth of the SH/Gain SC circuit which limits the overall conversion rate. By using 1.5-bit per stage, the required interstage gain is two, which results in the large feedback factor (around 1/3).

2. It maximizes the correction range for comparator offsets in the sub A/D converters. In this scheme, digital correction allows comparator offsets up to $\pm Vref/4$. For a supply voltage of 1.5V, the signal swing is set to be $Vcc/2 \pm Vcc/4$ or $(0.75 \pm 0.375)V$. Vref is $Vcc/2$ or 0.75V and hence offsets of 187.5mV can be tolerated. This relaxed specification on comparator resolution could be satisfied easily.

The most critical block is the MDAC, which performs four functions: sample and hold, D/A conversion, subtraction and multiplication. The analog residue signal generated by the MDAC will be processed by the remaining stages, so that its accuracy needs to be within half an LSB voltage

of the following ADC. The requirement for the first stage MDAC is the most strict. It relaxes stage after stage.

In order to implement the S/H function which is crucial for the concurrent operation, and to achieve high linearity, switched-capacitor (SC) circuit is the only feasible implementation for the MDAC. The conventional structure of an SC MDAC in single-ended form is shown in Fig. 3.3. In phase1, the input signal is sampled into both Cs and Cf. Here the opamp is autozeroed for easy illustration. This could be unnecessary because the ADC is offset insensitive due to the digital correction schemes. In phase2, the bottom plate of Cf is connected to the output of opamp and the bottom plate of Cs is connected to one of three voltage levels (+vref, -vref or ground) determined by the digital output of ADC. The transfer function of MDAC is:

$$Vout = \frac{Cs + Cf}{Cf} Vin - D_{out} Vref \tag{3.1}$$

Here, if Cs is equal to Cf, a multiply-by-two function is performed. The equation assumes that the opamp is ideal. In reality, the gain and settling error of opamp, matching between Cs and Cf, and charge injection of the switches determine the accuracy of this transfer function, and therefore the final resolution of the whole ADC.

3.3. Low-Voltage MDAC

Under low supply voltage conditions, the conventional MDAC structure shown in Fig. 3.3 is no longer applicable due to the switch overdrive problems mentioned in previous chapter. All switches connected to the input signal, reference voltage and output of opamp will have problems unless the clock is boosted or the threshold voltage is extremely low. In this work we will use the new scheme proposed in chapter 2 to solve this problem. The single-ended version of the low-voltage MDAC is shown in Fig. 3.4. The circuit consists of three functional parts as indicated by the dotted lines. Cs and Cf together with switches S5', S3, S4 and S5 perform the S/H and multiplying-by-two functions. The DAC function is done by the two SCs CrefA and CrefB together with a

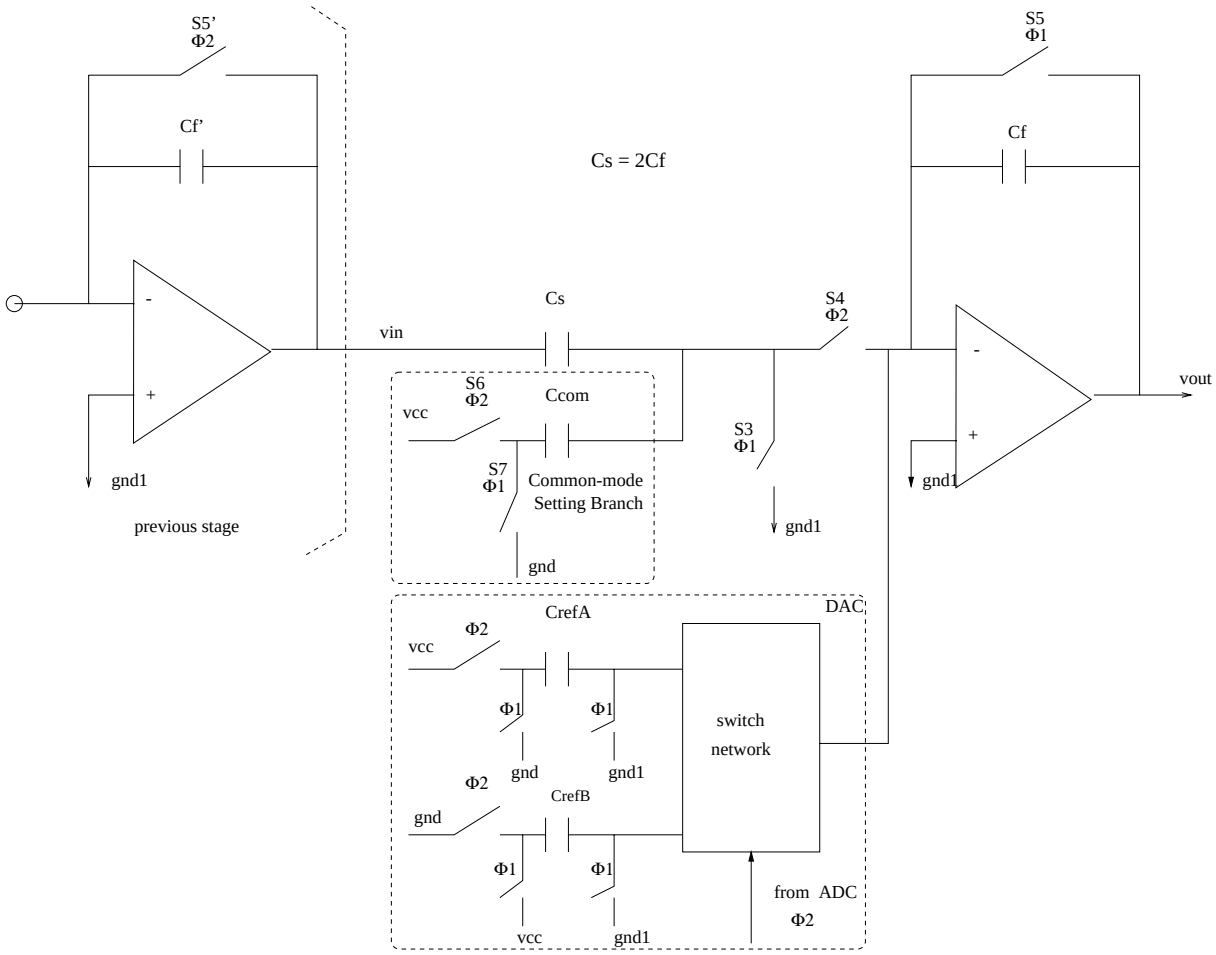

FIGURE 3.4: Low-voltage MDAC: single-ended structure

switch network controlled by the digital output from the ADC. The Common-mode setting branch will be explained later.

The operation of multiply-by-two function is done as follows: during phase1, S3 is closed and the output of previous stage settles to the proper value, which is sampled by Cs. In the meantime switch S5 is closed so the interstage gain amplifier is configured as an unity-gain buffer and Cf is reset. During phase2, S5' in the previous stage is closed, and the node A is set to be virtual ground. At same time S5 opens and S4 closes. The charge in Cs is transferred to capacitor Cf. Since Cs is two times Cf, multiplying by two takes place. In this scheme, all switches are either connected to ground and virtual ground (actually gnd1, which is above ground for the reasons explained later). Signals are fed to the bottom plates of the capacitors directly without any switch.

The new MDAC structure suffers in speed compared to the conventional one due to three factors:

1. Smaller feedback factor. In a conventional structure, the multiplication-by-two is performed in the way that two identical capacitors sample the input signal in phase1 and one capacitor acts as feedback cap in phase2. The feedback factor is 1/2 (not considering the opamp input capacitance) when the opamp settles in phase2. In the new low-voltage scheme, the factor is 1/3. This means that the opamp for the new scheme needs to be 50% faster than for the conventional one to achieve the same conversion rate. Actually the difference is about 30% if we take the input capacitance of the opamp into account. The conventional structure could not be used under low voltage conditions, since the switch could be connected only to ground or the voltage supply to guarantee the overdrive. No signal path is allowed for the sampling switch.

2. Concurrent settling. Another factor to slow down the speed is concurrent settling in phase2 in the new scheme. In this phase, the previous opamp settles to ground while the present stage settles to the proper residue value. Another point needs to be mentioned about switches S3 and S4. These two switches could be eliminated without effecting functionality, or even reduce the amount of charge injection which would cause common-mode voltage drift issue which we will discuss later. But without S4, the opamp of the present stage will see more load when configured as unity-gain buffer in phase2. That will increase the settling time and limit the conversion rate.

3. Large signal slewing. This is the third factor which slows down the speed. In the new scheme, from phase1 to phase2, the output of the opamp needs to slew from near ground to $\frac{Vcc}{2} + \frac{Vcc}{4} = \frac{3}{4}Vcc$ in the worst case, instead of from $\frac{Vcc}{2}$ to $\frac{3}{4}Vcc$ in the conventional structure. But fortunately this structure is used under low voltage conditions, and the slewing difference is compensated by the smaller signal swing.

Compared to the conventional structure, the new scheme is expected to have worse capacitor matching property. This is because in the conventional scheme $Cs = Cf$, and in the new scheme

$Cs = 2Cf$. Matching of the former is more accurate than the latter.

For the DAC part, unlike in the conventional structure which could afford generating Vrefp, Vrefn, and using switches to connect one of them to the bottom plate of the sampling capacitor, in the low voltage scheme we need to generate a positive and a negative charge packet with supply voltage Vcc and gnd, capacitor CrefA and CrefB, and switches. The digital output of the ADC decides whether to deliver the charge and its polarity. If the digital code is 00, a positive charge packet will be delivered to the feedback capacitor; if the code is 10, a negative charge will be delivered. When the code is 01, no charge will be delivered.

One point needs to be mentioned is the way how to deliver zero charge. We can not simply disconnect the top plate of CrefA and CrefB from the summing node during phase2. Instead we always connect them in phase2 and switch their bottom plate to the same voltage(gnd to gnd or Vcc to Vcc). The scheme in differential form is shown in Fig. 3.6. In this way a constant error charge caused by the opamp offset will always be delivered to the feedback capacitor Cf independent of the ADC output. If we use the former method, the offset charge will be signal dependent, and therefore harmonic distortion will occur. In the fully differential implementation, a cross-coupled scheme is used to simplify the circuit. The ratio of Cref over Cf determines the reference voltage level. In Fig. 3.6, Cf equals to $(Cmoon1 + Cmoon2)/2$. This will be explained later.

The gnd1 in Fig. 3.4 is set to 0.2 V, instead of the real ground. This is based on the consideration that when opamp is connected as a buffer, the *Vds* of the output device should be greater than *Vdsat* to prevent it from out of saturation. Although there exist some schemes which add a switched-capacitor battery between the inverting input and the output of opamp such that generating gnd1 is not necessary [10], we believe these complicated schemes will affect the speed and accuracy of the circuit. Setting gnd1 above gnd also alleviates the instantaneous charge leakage problem discussed in the next section. Generating gnd1 inside the chip is not a trivial thing. It has to have enough drive ability and settle sufficiently fast to the specified value so that it doesn't slow down the circuit

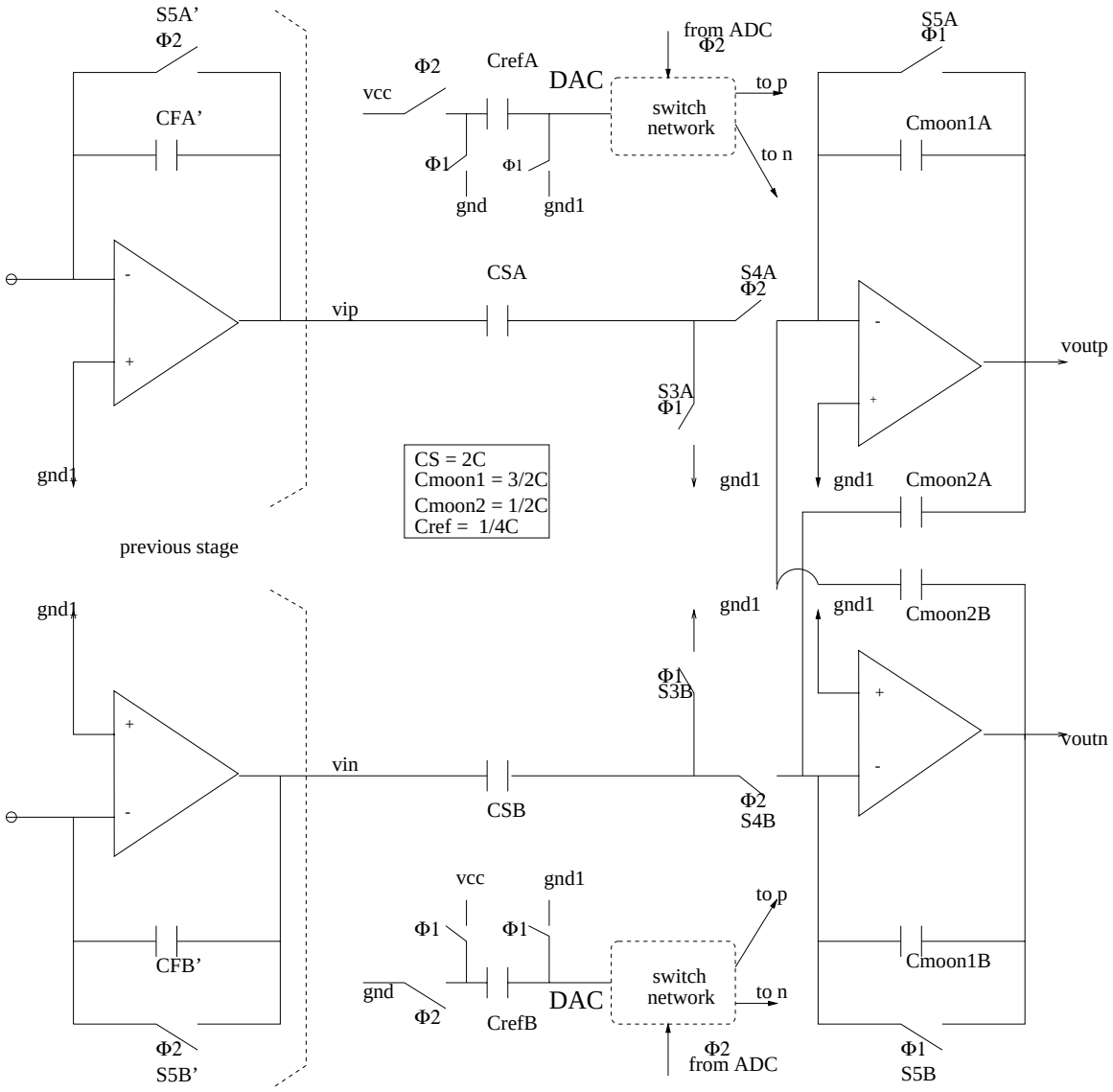

FIGURE 3.5: Pseudo-differential MDAC

further. Separated buffers are needed for different stages to reduce the crosstalk among them. In order to simplify the design, we plan to use an external source as gnd1 in the prototype chip. Gnd1 could be adjusted.

3.4. Design Issues

Following issues are considered in the process of the design:

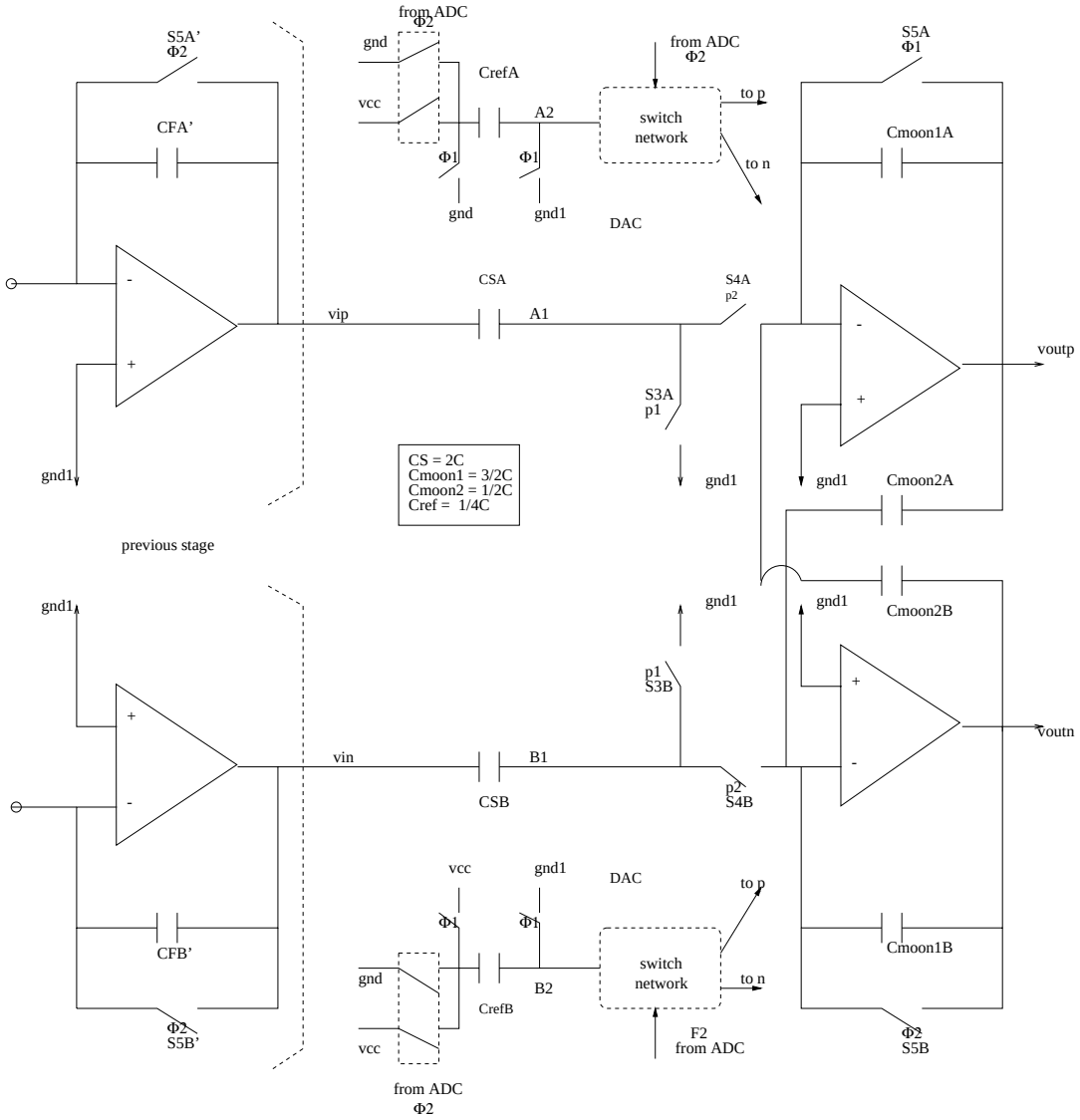

FIGURE 3.6: Pseudo-differential MDAC (version 2)

1. Single-ended vs. differential realization

   Fully differential structure has the following advantage over their single-ended counterpart:

   (a) increased dynamic range(DR)

   This is due to the fact that with a differential structure the power of the differential signal quadruples, while the power of noise only doubles due to uncorrelated noise sources. Thus the signal-to-noise ratio (SNR) gets 3 dB improvement over the single-ended version.

(b) better power supply rejection ratio (PSRR)

With fully differential structure, if the circuits are well matched, all noises coming from the power supply and the shared substrate can be treated as common-mode signals, which are suppressed by the common-mode rejection ratio (CMRR) of the circuits.

(c) charge injection cancellation

In the SC circuits the channel charge injected into the sampling capacitor when the switches turn off is one of the major nonidealities to compromise the accuracy of the signal processing. Fully differential structure cancels the charge injection errors imposed on the differential signal to the first order. Only the mismatch between switches in the two channels contributes to the error.

(d) better linearity

The even-order harmonic distortions will be canceled due to the differential operation of the circuit.

But under low voltage conditions, a true fully differential structure is hard to implement, especially under the constraint of high speed, mainly due to the difficulty of common-mode feedback (CMFB). This difficulty is caused by the limitation of both the opamp and the switches under low-voltage supply. In order to get a maximum signal swing, the common-mode voltage of the output signal is usually set to be at half of the power supply. At this level, no switch can sample the common-mode information as in the conventional switched-capacitor CMFB scheme. Even if the common-mode signal could be acquired by using a resistor divider as in the continuous-time CMFB, it cannot be the input to the CMFB amplifier directly unless it is level-shifted or scaled down to around the gnd or Vcc. There exist some complex schemes which use switched capacitors to get a level-shifted common-mode voltage, the extra load capacitance and switching activity will deteriorate the speed and accuracy performance. Furthermore, in the neww scheme we proposed, there exist two different common-mode levels in phase1 and phase2. In phase1 it is $gnd1$ and in phase2 it is $Vcc/2$. This makes the CMFB circuitry much more complicated.

To overcome the difficulty of CMFB and keep the advantage of differential structure to some extent, we use two opamps to act as a pseudo-differential one. The advantage of the increased DR and charge injection cancellation will be as same as for the true one. If two opamps are well matched in layout, then better PSRR and THD than for the single-ended structure are expected, although they may not be as good as for the fully-differential structure. Two opamps in pseudo-differential structure will consume more power than one fully differential opamp, due to the redundant current branches.

2. Common-mode control in pseudo-differential structure

   Since there is no common-mode feedback inside the pseudo-differential structure, another issue arises for the pipeline application. In the Fig. 3.4, the common-mode levels in phase1 and phase2 are different. Multiply-by-two operation will double this difference, which is not desirable. So a separate branch composed of switches S6, S7 and capacitor $Ccom$ can be added to set the $vout$ to have the right common-mode voltage in phase2. If we use two singled-ended circuits in Fig. 3.4 to form a pseudo-differential structure, the transfer functions for both differential and common-mode signals are as shown in the following equations:

$$Voutp - Voutn = 2(Vip - Vin) \tag{3.2}$$

$$Voutp + Voutn = 2(Vip + Vin) - Vcc \tag{3.3}$$

   Ideally the input common-mode $(Vip + Vin)/2$ is set to $Vcc/2$ so the output common-mode is as same as that of the input. But any mismatches between signal channels p and n, such as the ratio of $C1$, $C2$ and $Ccom$, charge injection, the gain and offset of the opamps, will cause the common-mode level to deviate from the ideal one. Although this slight deviation will not cause trouble for the proper operation of the differential signals, the interstage gain will amplify this deviation by a factor of two from stage to stage. Eventually at the last stage the accumulated error is in the order of 2^8 times the error per stage and will drive the opamp out of its operation region.

   This problem can be solved partially by the improved scheme shown in Fig. 3.5 [12]. The feedback capacitor Cf in Fig. 3.4 is split into two capacitors: feedback capacitor $Cmoon1$

and cross-coupled cap $Cmoon2$. Their values are $\frac{3}{2}Cf$ and $\frac{1}{2}Cf$, respectively. The switched-capacitor common-mode setting branch in Fig. 3.4 is no longer necessary. With this scheme, we can implement the gains of differential signal and common-mode signal separately as shown in the following equations:

$$Voutp - Voutn = \frac{Cs}{Cmoon1 - Cmoon2}(Vip - Vin) \tag{3.4}$$

$$Voutp + Voutn = \frac{Cs}{Cmoon1 + Cmoon2}(Vip + Vin) \tag{3.5}$$

In our case, $Cmoon1$ is $\frac{3}{2}Cf$ and $Cmoon2$ is $\frac{1}{2}Cf$, where $Cs = 2Cf$. So the differential gain is two and the common-mode gain is one. This means that any common-mode level deviation from the previous stage will pass to the next stage without any amplification. This solution is still based on an open-loop structure. No feedback is present to suppress the common-mode error as in the real fully differential circuits, and the error accumulation from stage to stage still exists. But the error only grows linearly and at the output of stage8, the accumulated error is in the order of 8 times the error per stage. SWITCAP and Hspice simulation show that this error could be controlled to be within 100mV so that all outputs of the opamps are in the linear operating region. The main source for this common-mode drift is the charge injection of the switches connected to the input of opamp. For differential signals their effect is negligible due to the differential cancellation. However, for common-mode signal no cancellation exists. Since all these switches are n-channel devices, the negative charge injection will pull the common-mode level of the output down. The sizes of the switches are optimized to trade off RC time constant with charge injection.

We also can set the common-mode voltage gain between adjacent stages to be less than unity so the error could be attenuated from one stage to the next [14]. But the capacitors $Cmoon1$ and $Cmoon2$ will be bigger and the common-mode setting branch needs to be used again. All of these will be at the cost of circuit complexity and speed performance and they will not be used in the test chip.

3. Stage accuracy requirement

   As mentioned previously, the accuracy requirement for each stage in pipeline structure is different. For the first stage, it is the most strict and is determined by the resolution of the ADC. For the following stages, it becomes more and more relaxed due to the gain of the previous stages. The following discussion focuses on the first stage. For the circuit shown in Fig. 3.6, the transfer function is as shown in the following equations:

$$Vout = G_1(Vin - G_2 D_{out} Vref) \tag{3.6}$$

$$G_1 = \frac{Cs}{Cf}(1 - e^{(-t/\tau)})\frac{1}{1+Af} \tag{3.7}$$

$$G_2 = 4\frac{Cref}{Cs} \tag{3.8}$$

$$f = \frac{Cf}{Cs + Cf + Cp + Cref} \tag{3.9}$$

   In the above equations, $Vout$ and Vin are the differential output and input signals, respectively. $Vref$ is set to be $Vcc/2$, D_{out} is the digital output of the ADC with the values 0 and ± 1. A is the DC gain of the opamp and f is the feedback factor. Cf is the equivalent feedback capacitor which equals $(Cmoon1 + Cmoon2)/2$. The nominal values of $\frac{Cs}{Cf}$ and $\frac{Cref}{Cs}$ are set to be 2 and 1/8 respectively. Cp is the input capacitance of the opamp, including the parasitic capacitor associated with the top plate of Cs, $Cmoon1$, $Cmoon2$ and $Cref$, the junction capacitors associated with the switches, and the gate capacitor of the input transistor of the opamp.

   From Eq. 3.6, the resolution of the transfer function is determined by the following factors:

   - Matching between Cs and Cf

     For a 10-bit resolution, in the first stage the matching error between these two capacitors needs to be less than $1/2^{10}$ or 0.1%. For the first two stages, 0.8pF and 0.4pF are used for Cs and Cf. So $Cmoon1$ is 0.6pF and $Cmoon2$ is 0.2pF.

   - Gain of opamp

     The Af term in the Eq. 3.7 should be greater than 2^{10} to keep the error induced by the finite gain of the opamp within 10-bit resolution. Since $f = \frac{1}{3}$, if Cp and $Cref$ are

ignored, the DC gain of the opamp needs to be greater than 3000 or about 70 dB for the entire output swing range.

- Bandwidth of opamp

  The error term $e^{(-t/\tau)}$ in Eq. 3.7 is determined by the settling behavior of the opamp if the RC time constant caused by on-resistance of switches is small enough to be ignored. Assuming that the opamp can be treated as a single pole system, we have the following equation:

$$\tau = \frac{1}{\omega_{CL}} = \frac{1}{\omega_{opamp} f} \tag{3.10}$$

  To achieve 10-bit resolution, the total allowed settling time $1/2fs$ should be 7τ. Since the feedback factor $f \simeq 1/3$ and $2\pi f_{opamp} = \omega_{opamp}$, f_{opamp} need to be $\frac{21fs}{\pi}$. In this design, the sampling frequency is 20 MHz, therefore the unity-gain bandwidth requirement of the opamp is greater than 140 MHz. Considering the opamp used in this work is a two-pole system, the bandwidth requirement needs to be higher.

- Matching between $Cref$ and Cs

  As seen in Eq. 3.6 and Eq. 3.8, the resolution of DAC depends on the accuracy of G_2, which is determined by the matching between $Cref$ and Cs. The nominal value is set to be 1:8. If the deviations from this value are constant for all stages, it is equivalent to changing the reference voltage and will not degrade the linearity of the converter severely. So the matching is only needed between $(\frac{Cref}{Cs})_{stage1} : (\frac{Cref}{Cs})_{stage2}$, and so on.

Another approach to increase the minimum value of $Cref$ is shown in Fig. 3.7 (only the DAC branches are shown for simplicity). CrefA is divided into two capacitors CrefA1 and CrefA2. CrefA1 transfers negative charge to the feedback capacitors CFA or CFB. CrefA2 transfers positive charge. If CFA and CFB are C, CrefA1 and CrefA2 will be C and (3/4)C respectively. The net charge transferred to the feedback capacitor by CrefA1 and CrefA2 combined is negative and is equivalent to what is generated by CrefA with value of 1/4C. Similarly, CrefB1 and CrefB2 substitute CrefB to transfer positive and

negative charge. Net charge is positive. With this scheme, the minimum capacitance increases from (1/4)C to (3/4)C. The matching of these capacitors among stages becomes much easier. The drawback is the increased number of switches and capacitors [13].

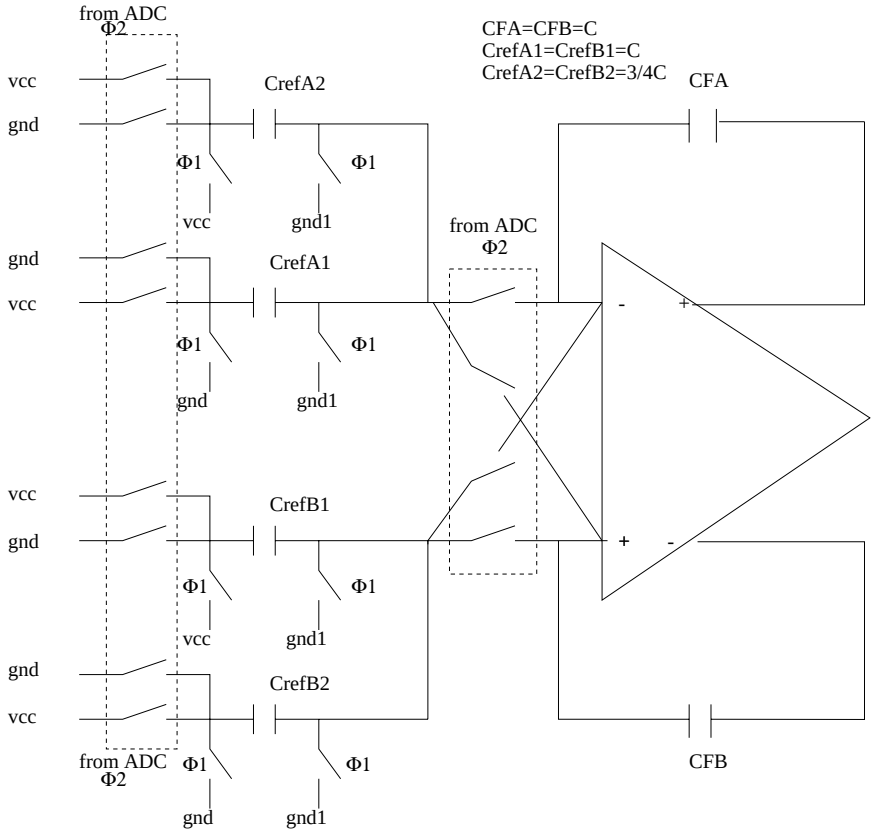

FIGURE 3.7: Improved MDAC scheme for better matching of Cref

- Resolution of the coarse ADC

  The D_{out} in Eq. 3.6 is determined by the coarse ADC of the stage. Due to the digital correction techniques the resolution requirement for this part of circuit is low. For this design, $\pm Vref/4$ offset in the decision level can be tolerated.

Other issues that affect the accuracy of the stage are:

- kT/C noise

  In a 10-bit ADC, the circuit thermal noise is dominated by the kT/C noise. Noise from the operational amplifier could be ignored. All switch thermal noises sampled by the capacitors in each stage can be referred to the input of the ADC. Since in the latter stages the noises are divided by the prior interstage gain when referred to the input, they become quite small to be negligible. The noise from the first stage dominates the total noise and can be expressed as:

$$V_{noisein} = \sqrt{\frac{kT}{Cs}}(1 + \sqrt{\frac{Cref}{Cs}}) \tag{3.11}$$

  The ratio of Cref to Cs is 1:8, so the kT/C noise associated with Cref is negligible. Considering the fact that the maximum differential signal is ± 0.75V, to achieve the signal to noise ratio (SNR) of 65 dB, the minimum value of Cs is 0.36pF. This requirement is more relaxed than the matching requirement. So the minimum capacitor size is eventually limited by the matching between capacitors, instead of the kT/C noise consideration.

- Sizes of switches

  The sizes of switches are designed to be as small as possible to reduce the parasitic capacitance and the charge injection. In this design, reducing charge injection is crucial. Unlike in the conventional structures in which only the charge injection mismatch between the differential channels causes trouble for the differential signals, the absolute amount of the charge inject here also matters because it may lead to the drift of the common-mode level. The minimum sizes of the switches are determined by the RC time constant formed by the on-resistance of the switch and the sampling capacitor. To make the settling time due to RC less significant than the opamp settling time, design equation $\frac{1}{2fs} \geq 10RC$ is satisfied. The other equations in the design are shown as follows:

$$R = \frac{1}{\mu C_{ox}\frac{W}{L}(Vgs - V_T)} \tag{3.12}$$

$$Q = WLC_{ox}(Vgs - V_T) \tag{3.13}$$

$$RQ = \frac{1}{L^2\mu} \tag{3.14}$$

From Eq. 3.14 [15] we can see that the on-resistance and the charge injection are a trade-off which is technology dependent. In this design, we use $4\mu m/0.28\mu m$ for the n-channel switches and $8\mu m/0.28\mu m$ for the p-channel switches. The common-mode drift due to the charge injection is within 10mV/stage. Dummy transistors could be used to reduce the charge injection but will increase the parasitic input capacitance which will reduce the feedback factor. Four-phase clock sampling scheme is used to reduce the signal-dependent part of charge injection for the differential signals.

- Instantaneous charge leakage

  In Fig. 3.6, node A1 and B1 are likely to change from gnd1 to a negative voltage after switches S3A and S3B are opened and the outputs of the previous stage reset to gnd1 from a higher level. Since the switches S3A, S3B, S4A and S4B connected to node A1 and B1 are both NMOS transistors, the negative voltage in node A1 and B1 will cause the pn-junction forward biased and leakage currents result. The accuracy of the charge transfer from Cs to Cf will be degraded. To prevent this from happening, switches S4A and S4B need to be closed before the reset switches S5A' and S5B' in the previous stage close. Four-phase clock scheme used here for charge injection issues helps to solve this problem. The clock for S4A and S4B is phi2a and clock for S5A' and S5B' is phi2 (delayed version of phi2a).

  Proper timing does not necessarily eliminate this leakage problem. Since the speed of the opamps is limited, node A1 and B1 take time to settle to the virtual ground (gnd1) after signal changes in the bottom plate of CsA and CsB. Negative glitches in these charge conservation nodes are harmful. This is one of the reasons that gnd1 must be above real ground to give some margins for these trouble-making glitches. Another node one needs to be careful about is B2. In phase2, when the ADC output is 00 or 10, the bottom plate of CrefB will be changed from Vcc to gnd and the top plate will follow this negative jump if the switches inside the dotted network haven't been connected to the input of the opamp. Extra digital circuits are needed to make sure that switches at the right side of capacitor CrefB are closed before the switches at the left side are con-

nected to gnd.

4. Scaling of the pipeline stages

   Based on the fact that the resolution requirement decreases from first stage to the last stage, we plan to scale down the capacitors and bias currents of the opamps in the latter stages to reduce the power consumption and the chip size [16]. For the first and second stage, the Cs, Cf and $Cref$ are 0.8pF, 0.4pF and 0.1pF respectively. The large capacitance is needed for the matching between Cs and Cf. Two opamps acting as a pseudo-differential one consume 3mA per stage. In the latter stages the sizes of the capacitors are reduced by half to 0.4pF, 0.2pF and 50fF. The bias current will be reduced to 2mA per stage.

The SWITCAP simulation for the whole pipeline ADC verifies the functionality of the new structure. Transient waveforms of eight residue outputs are shown in Fig. 3.8. The FFT spectrum of the digital output is shown in Fig. 3.9. Extensive simulation shows that the structure is insensitive to the comparator offsets and opamp offsets. If the capacitor mismatch is within 0.1% and the DC gain of the opamp greater than 70 dB, the achievable SNDR is 60 dB or 10-bit resolution.

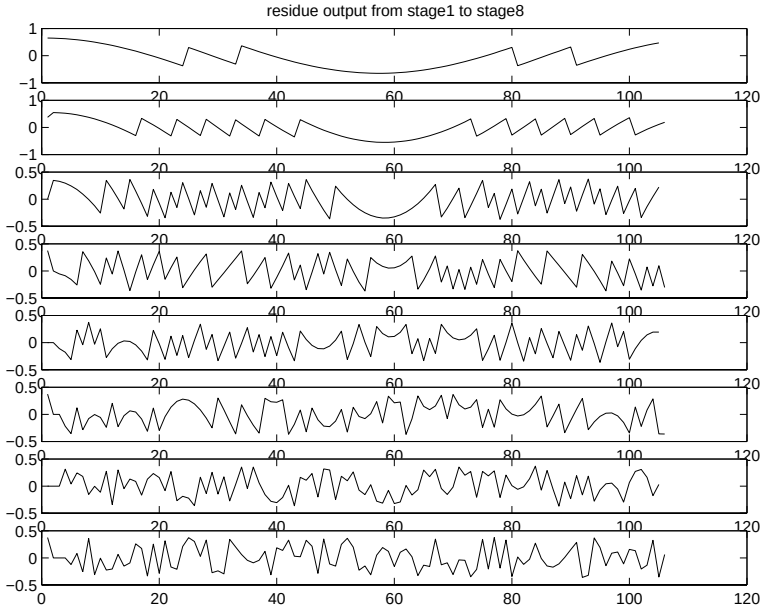

FIGURE 3.8: Waveform of residue outputs from stage1 to stage8 (SWITCAP simulation)

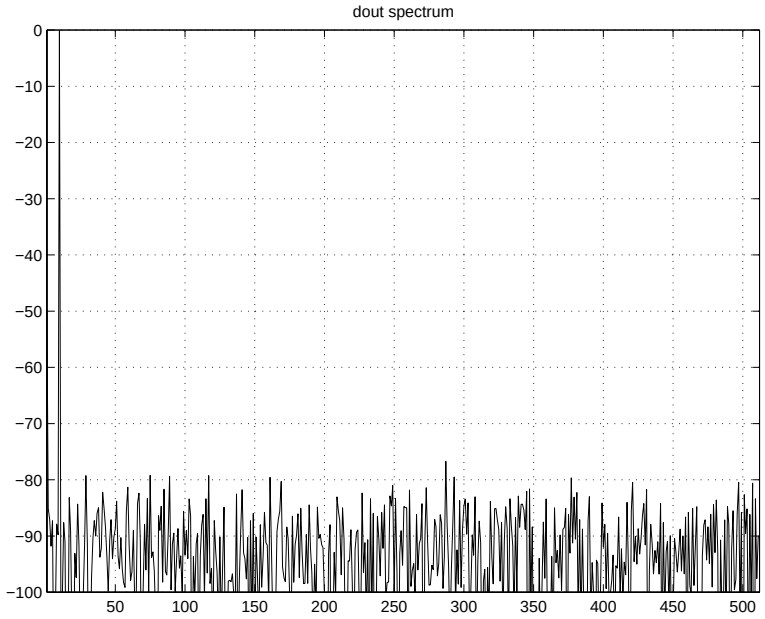

FIGURE 3.9: Spectrum of pipeline ADC digital output (SWITCAP simulation)

4. CIRCUIT IMPLEMENTATION

4.1. Low-Voltage Opamp

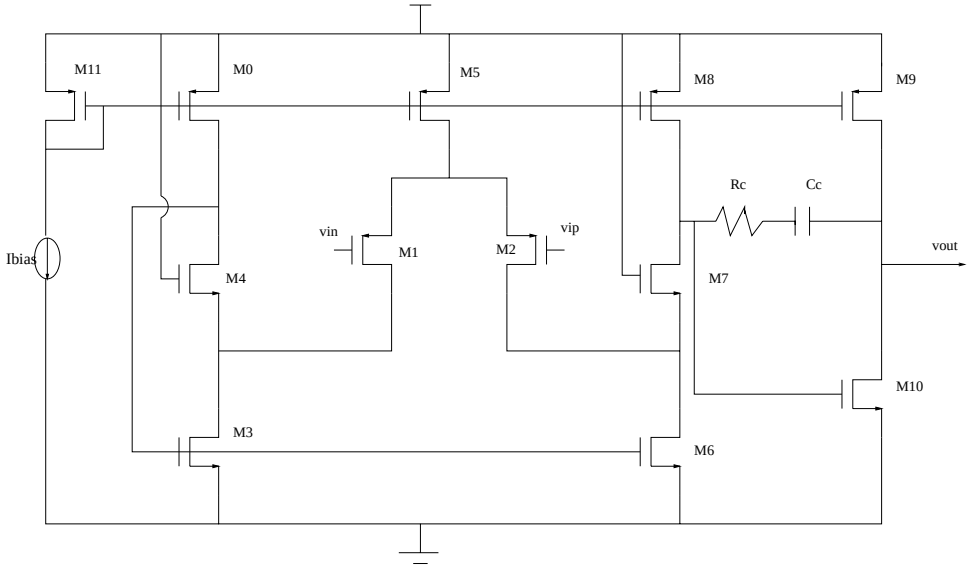

FIGURE 4.1: Schematic of a low-voltage opamp

The operational amplifier used in the MDAC is the most important part to determine the speed and accuracy performance of the converter. For the 10-bit resolution , or the signal to noise plus distortion ratio (SNDR) to be greater than 60 dB, DC gain of 70 dB is needed for the opamp in the first stage. For the conversion rate of 20 MS/s, the opamp needs to be settled within 0.1% of the final value in less than 25 ns. This specification is a challenge for the opamp design at low voltage condition since the high-speed structure, such as telescopic or folded-cascode can not be used due to the limited headroom.

The opamp used here is shown in Fig. 4.1. It is a differential-input single-ended output two-stage Miller-compensated opamp [17]. The input stage is a modified folded cascode for low-voltage supply. Transistors M3, M4, M6 and M7 form a high-swing current mirror. Cascode devices M4 and M7 are biased by Vcc for simplicity. The second inverting stage consists of M9 and M10 to

achieve high swing. Cc and Rc make up the standard Miller-compensation.

The input of the opamp is set to gnd1, around the *Vdsat* of transistor of M10. Thus, when the opamp is configured as an unity-gain buffer, output device M10 will not be out of saturation. Supply voltage should be greater than $Vdsat10 + V_{Tp} + Vdsat1 + Vdsat5$. In Lucent $0.25\mu m$ process, V_{Tp} is around 1V and we set *Vdsat* to be over 0.1 V. So the minimum supply voltage for this opamp is 1.5 V.

If using the complementary structure with NMOS as input transistors, the required supply voltage could be reduced to 1.2 V because the nominal NMOS threshold voltage is 0.35V less than PMOS. The reasons to choose the current structure are as follows: 1)If using NMOS as input transistors, the input voltage would be biased around Vcc and most of switches need to be changed to PMOS transistors which will be much bigger than NMOS switch. This will increase the parasitic capacitance and charge injection. 2)The bandwidth of the opamp is limited by the second pole associated with the gm of the common-source transistor in the second stage. Second pole needs to be about 3 times of unity-gain bandwidth to achieve enough phase margin. With current configuration, the input transistor in the second stage is NMOS with bigger gm than PMOS under the same bias condition. 3)PMOS input transistors can be put into a n-well to reduce the body effect and substrate noise. 4)PMOS devices have lower 1/f noise. The last two advantages are not critical for this 10-bit resolution circuit.

The simulated frequency response is shown in Fig. 4.2. Cascoded compensation is claimed to have bandwidth advantage over Miller compensation used here and is less sensitive to the process variations. This could be improved in the future.

The sizes of the devices, including 11 of MOS transistors, the capacitor and the resistor for Miller compensation, are listed in Table 4.1.

Hspice simulation results are listed in Table 4.2.

M1/M2	150/0.3	M0/M8	75/0.5
M4/M7	40/0.4	M3/M6	40/0.4
M5	200/0.5	M9	400/0.5
M10	200/0.5	M11	10/0.5
Cc	1.1pF	Rc	400
Ibias	20uA		

TABLE 4.1: Transistor sizes of the opamp

DC Gain	80 dB
UGB	180 MHz
PM	80 degree
SR	100 V/us
Settling Time(0.1%)	20 ns
Power Consumption(1.5 V)	2.2 mW

TABLE 4.2: Opamp characteristics

The transient response was not satisfactory due to the peaking problem. This peaking is about 10 mV around the sampling point and greatly degrades the settling performance. Extensive simulation shows that the peaking is proportional to the gate-drain capacitance of M9. Large-swing signal in the output will be coupled to the gate bias node of M9 through C_{gd} and attenuated by a capacitor divider formed by C_{gd} and the total capacitor from bias of M9 to supply. Adding a cascode device between drain of M9 and the output can isolate the output from the bias node and reduce this peaking. But this solution will need more headroom and deems not practical for the low-voltage operation. Using a big decoupling capacitor (with value of 30pF) between the bias and the supply could attenuate the coupled signal greatly and therefore reduce the peaking. Further simulation

opamp ac response simulation

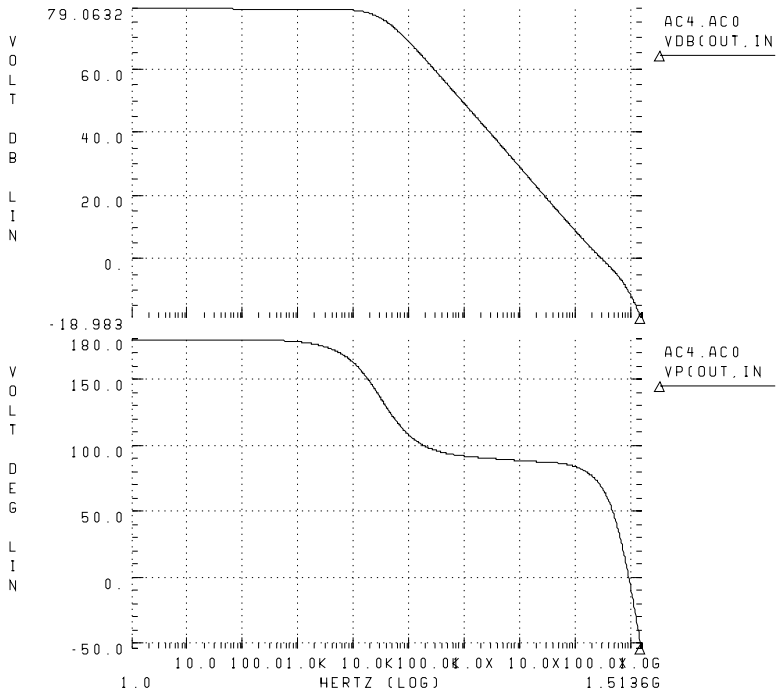

FIGURE 4.2: Opamp frequency response

shows that if we bias transistor M9 separately, a 10pF decoupling capacitor can achieve the same peaking suppression effect. This phenomenon is suspected to happen only in a single-ended structure, such as our pseudo-differential configuration. In the conventional fully-differential structure, the coupled signals due to the steps at opposite directions will cancel each other. This is illustrated in Fig. 4.3.

The transient step response is shown in Fig. 4.4. The output can settle to the final value with 0.1% error within 22ns.

Similar opamp is used in the input stage. When a full-scale sine wave is applied into the input stage, the FFT spectrum of the output after the first stage is shown in Fig. 4.5. The SNDR is about 70 dB. This proves that the settling requirement can be met for both stages.

The stage transfer function simulation by Hspice is shown in Fig. 4.6. The gain of two is

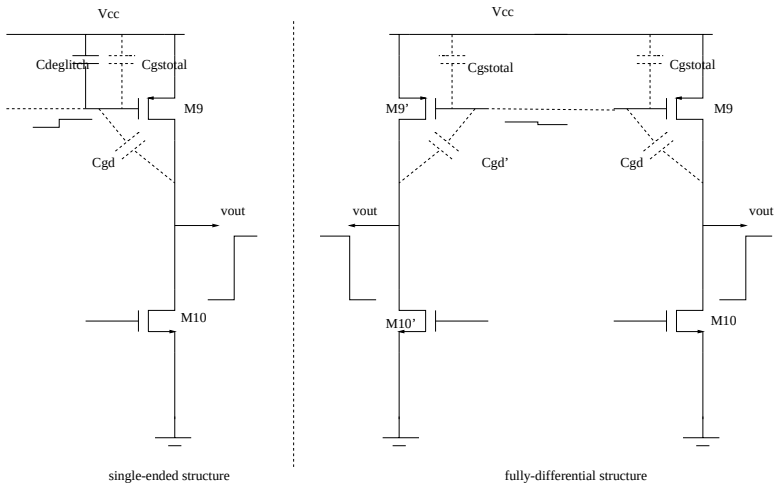

FIGURE 4.3: Peaking problem and a solution

opamp step response simulation

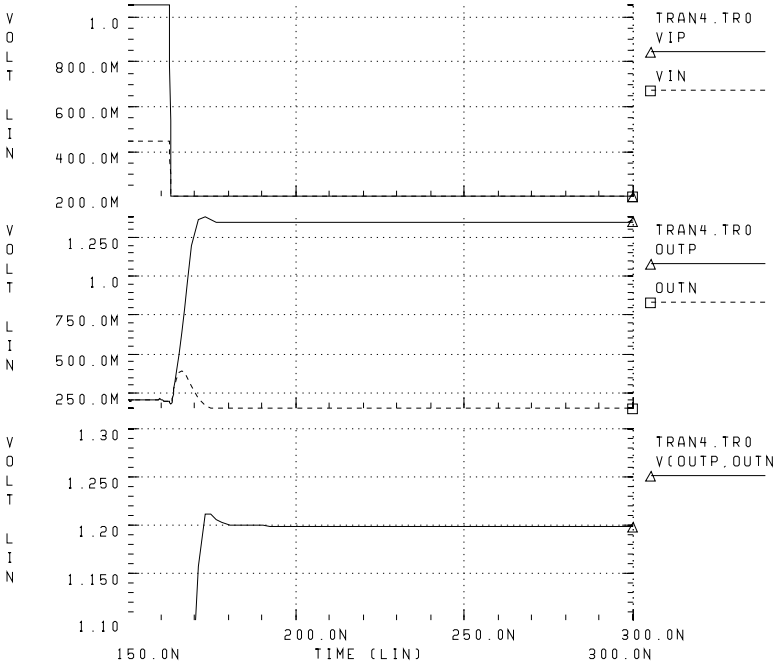

FIGURE 4.4: Opamp step response

within the 10-bit specification.

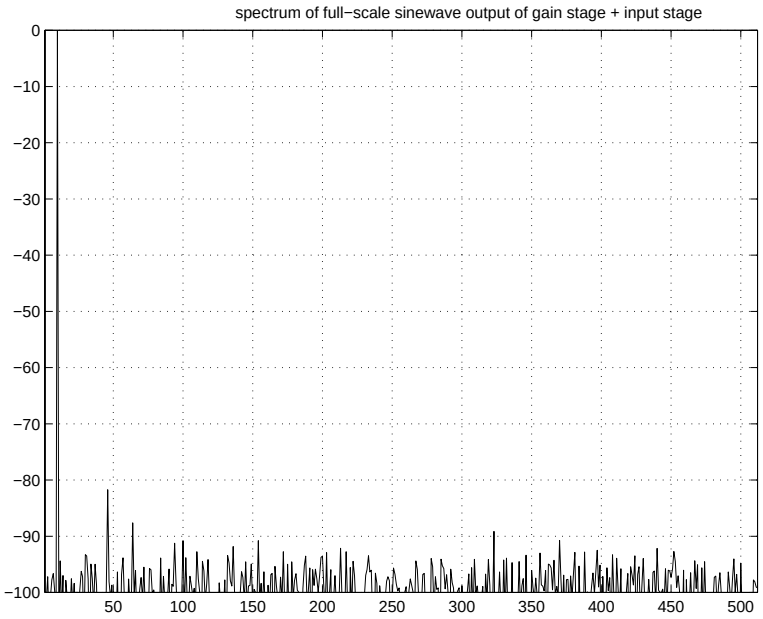

FIGURE 4.5: FFT simulation of the gain stage + input stage

stage transfer function simulation

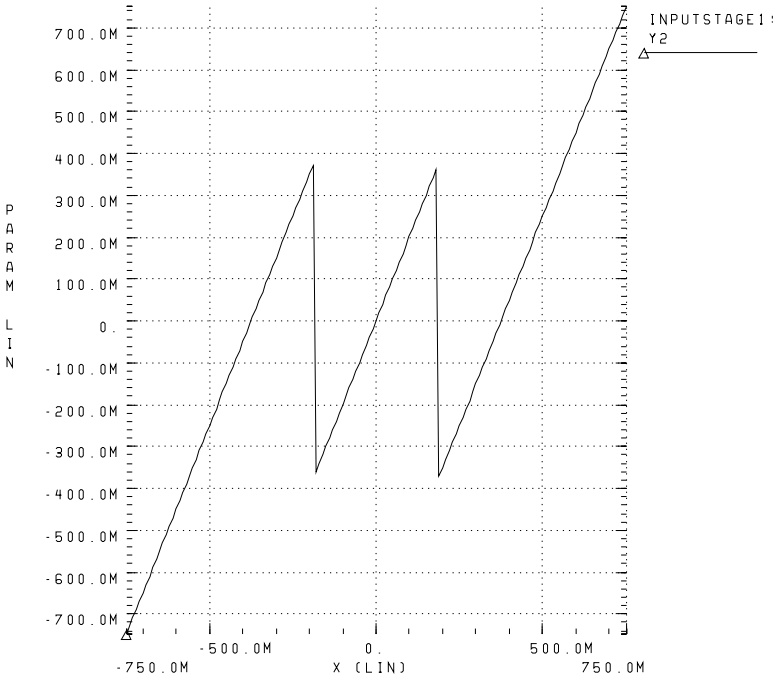

FIGURE 4.6: Hspice simulation of the stage transfer function

4.2. Low-Voltage Comparator

The coarse ADC in the first eight stages consists of two comparators shown in Fig. 4.7, which compare the differential input signal with two decision levels and generate one of three different digital outputs 00, 01 or 10. The switched-capacitor implementation operates as follows: During phase2 (of the previous cycle), Vip and Vin are both reset to gnd1. Switches S2A and S2B connect the bottom plates of C2A and C2B to gnd, while switches S3A and S3B set the input voltage of the preamp to Vcc. During phase1, S1A and S1B are connected to gnd and Vcc respectively. The signal $Vip - Vin - \frac{C2}{C1}(Vcc - gnd)$ appears at the differential input of the preamp. The Vref is set to be the half of Vcc, so the ratio of C2 over C1 is 1:8 such that the decision level is $Vref/4$. Exchanging the position of Vip and Vin is equivalent to set the decision level to be $-Vref/4$. A common-mode setting branch could be added so that in phase1 and phase2 the common-mode level of V1 and V2 are constant.

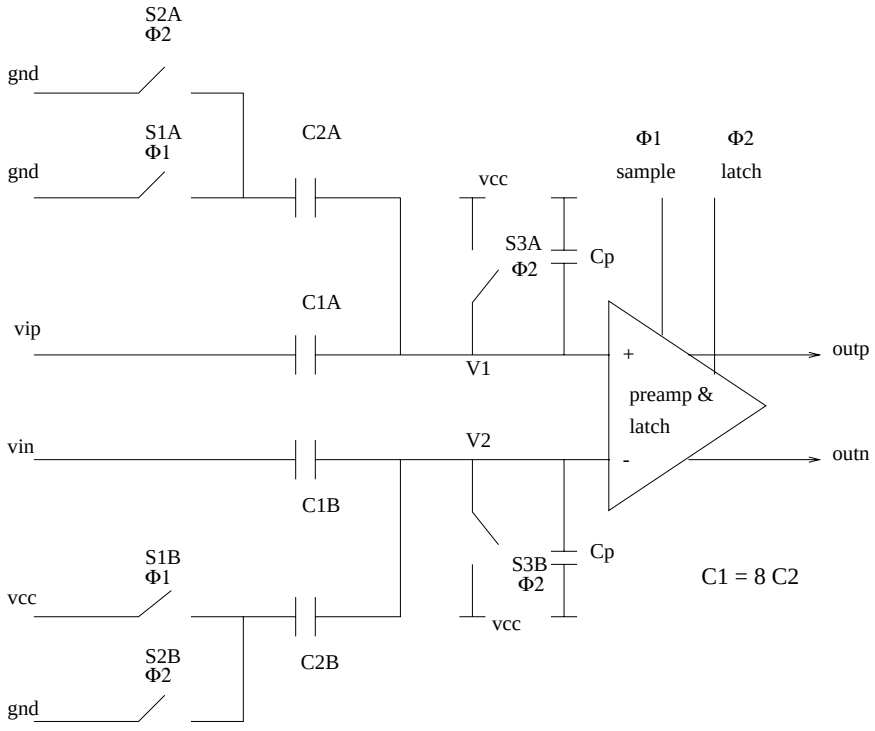

FIGURE 4.7: Schematic of a low-voltage comparator

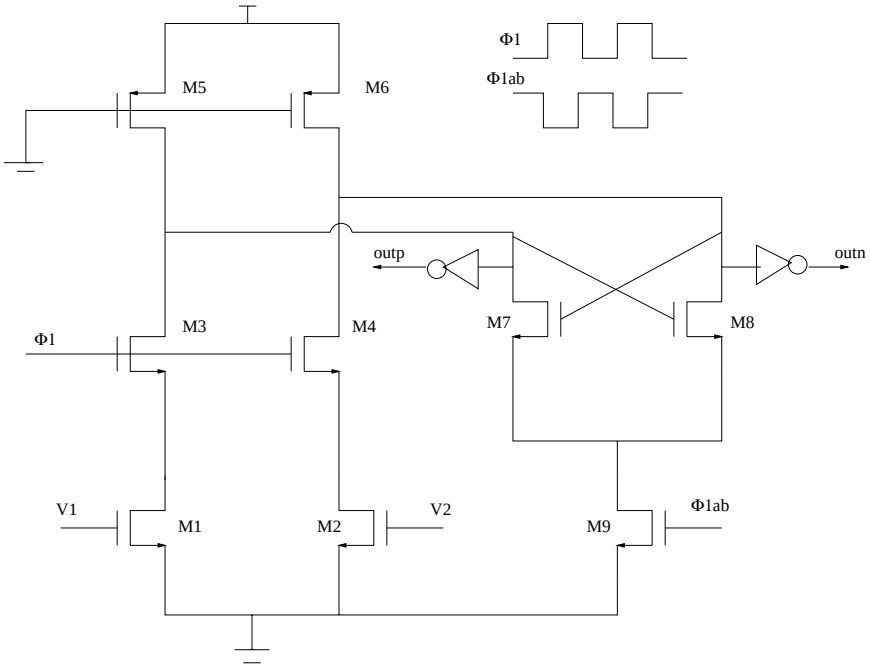

FIGURE 4.8: Schematic of the preamp and latch

The preamp and latch is shown in Fig. 4.8. The input signal is amplified by the preamp composed of input transistors M1, M2 and load transistors M5, M6. It is sampled at the end of phase1 by opening the switches made by M3 and M4. A latch composed of M5-M8 regenerates the difference signal into a logic level during phase2.

The common-mode level of the input to the preamp is set to be Vcc in phase2 so that either M1 or M2 will be on. One problem needs to be addressed is: when Vcc is connected to C2B in phase1, there will be a jump in node V2. If V2 exceeds Vcc too much, pn-junction between the drain of PMOS transistor (as switch) and its n-well will be forward biased. The leakage current is likely to cause inaccuracy. Charge sharing capacitor Cp is used to attenuate the voltage appeared in V1 and V2. The value of Cp is chosen to be 0.6pF so that when $V2-V1=\frac{Vref}{4}$, the most sensitive point for the comparator, V2 will not exceed Vcc by 0.3 V. In the other cases, the input is a large signal and any leakage will not cause significant error. The differential signal is also attenuated by $\frac{C1}{C1+C2+Cp}$, which will be compensated by the gain of the preamp stage.

$$V1 - V2 = (Vip - Vin - Vcc\frac{C2}{C1})\frac{C1}{C1 + C2 + Cp} \tag{4.1}$$

In this comparator scheme, input signals are connected to the capacitors directly without any switches so that the overdrive problem is avoided at the low-voltage condition. This is different from what is used in [5]. One drawback of this circuit is that the capacitance spread of $C1$ and $C2$ is too big, which will increase the load of the interstage amplifier. $C2$ is designed to be as small as 25fF to reduce the loading. The matching here is not as critical as in the gain stage. Capacitor mismatch changes the decision level of the ADC. The resulting offset could be digitally corrected by the redundant coding.

The ninth stage is a true 2-bit ADC. There are three comparators with decision levels set at $-Vref/2$, 0 and $Vref/2$. The comparators have the same structure. For the decision level of $-Vref/2$ and $Vref/2$, the ratio of $C1$ over $C2$ is 4. For the decision level of 0, $C2$ branches are omitted.

4.3. Input Stage

The new low-voltage SC scheme fulfills the charge transfer function with the help of the previous stage resetting to the virtual ground. A dedicated input stage will play this role to transfer a continuous analog input into a signal which tracks the input in phase1 and resets to gnd1 in phase2. As shown in Fig. 4.9, in phase1 switch S1 is closed. The identical resistors R1 and R2 together with the opamp act as an inverting buffer. During phase2, S2 is closed, and Vout resets to the virtual ground (gnd1). In this phase, switch S1 is open to reduce the driving current of the opamp. The signals seen by switches S1 and S2 are all gnd1, so there is no switch drive problem.

In order to set the common-mode level of Vout to be $Vcc/2$, the input common-mode voltage need to be $2gnd1 - Vcc/2$. Since gnd1 is lower than $Vcc/2$, a normal signal around the middle

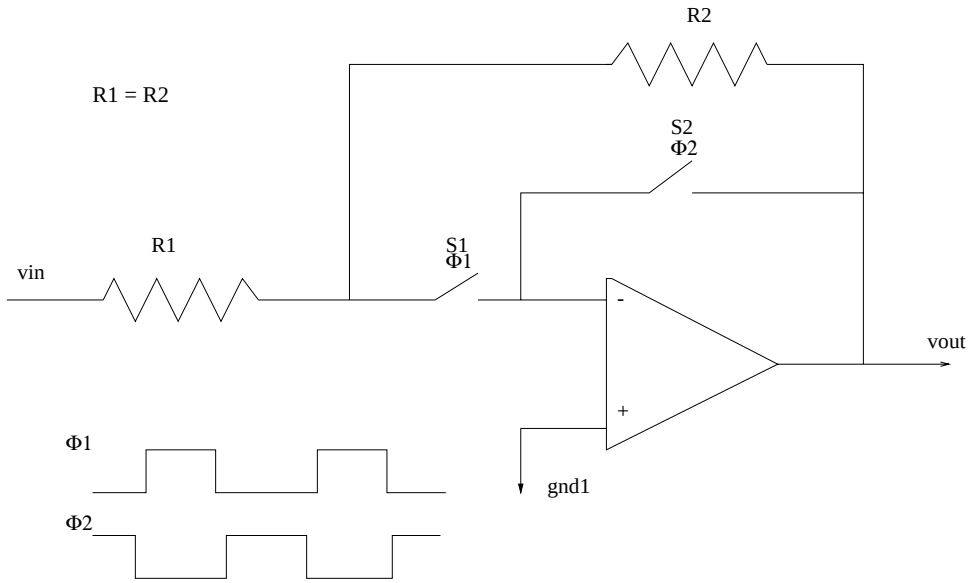

FIGURE 4.9: Schematic of input stage

of the supply could not be used. Part of the input signal will be negative. There is a solution to this problem in [18] by using a switched-capacitor battery to adjust the input and the output to have the same common-mode level. But the added circuitry is harmful for the high-speed and high-resolution requirement. Since our main motive is to verify the performance of the new SC structure, the input stage is designed to be as simple as possible not to degrade the input signal to the ADC. External input signal with adjustable DC level will be applied to test the chip. With this external input source, we can also adjust the input common-mode level to compensate the common-mode drift in the following stages.

The structure of the opamp used in the input stage is similar to the one used in the gain stage for the ease of design. The DC gain will suffer a little due to the resistance load, but is still above 60 dB, which will be enough for the distortion requirement. Resistor R1 and R2 will be layed by poly-silicon. The resistance is $5K\ \Omega$. The FFT of the simulated output after input stage and first gain stage is shown in Fig. 4.5.

4.4. Clock Generator and Digital Circuitry

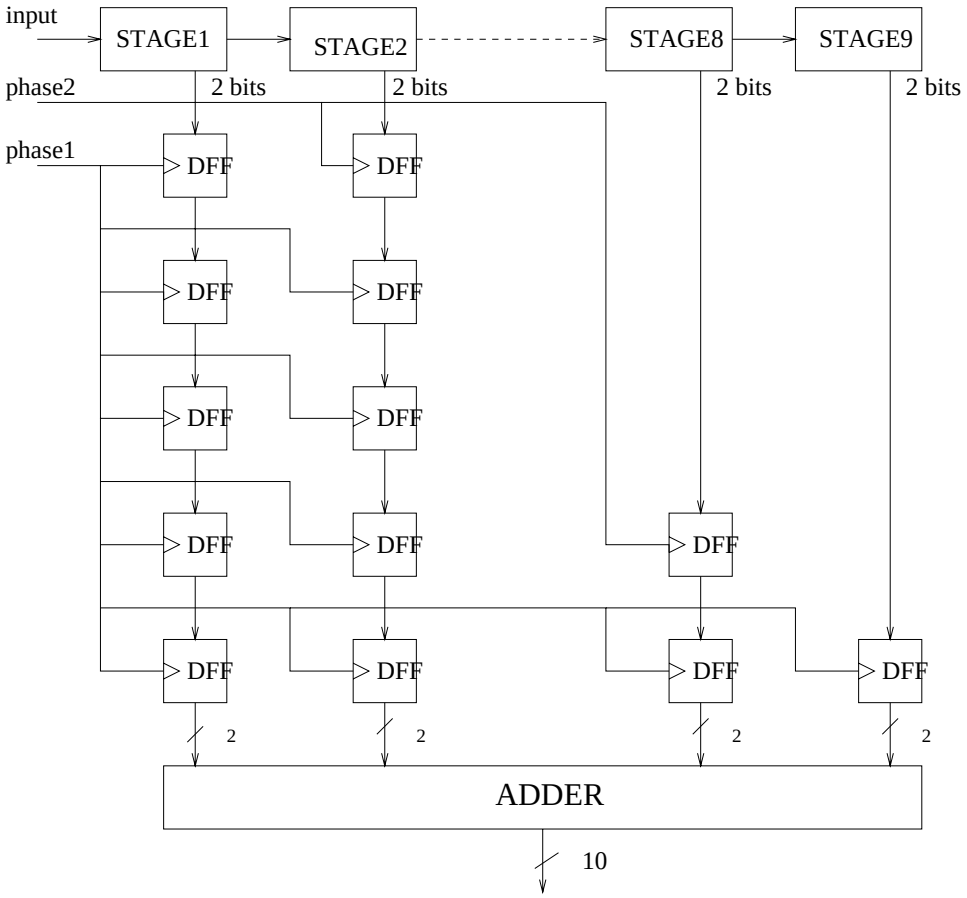

FIGURE 4.10: Schematic of the digital circuitry

The digital outputs for a given input analog sample are not generated at the same time. MSB comes first and LSB last. The time delay between adjacent bits is one half clock cycle. All bits need to be synchronized before go to the digital correction block. Shown in Fig. 4.10, the 2-bit digital output from the first stage is delayed by 9 half cycles and the output from the second stage is delayed by 8 half cycles, and so on. The output from the last stage is delayed by a half cycle.

The digital correction is done by adding the (n+1)th stage output to the nth stage output with the LSB of nth stage overlapping with the MSB of the (n+1)th stage. The carry will propagate in the direction of the MSB. The maximum code of the first 8 stages is 10 and for the last stage the

ADC output is a true 2-bit (four possible codes from 00 to 11). There will be no carry generated eventually and the 10-bit output is the final digital data of the pipeline ADC.

The delay block is made of D flip-flops (DFF) implemented with transmission gate and static inverter. Since sampling rate is only 20 MS/s and the wordlength is 10 bits, the carry ripple is not an issue under $0.25\mu m$ process. No special efforts are made to design a high-speed adder. Full adder is used.

The four-phase clock signals used in SC circuits are generated by the scheme shown in Fig. 4.11. From the master clock *clockin* running at 20 MHz, non-overlapping clocks phi1a and phi2a are generated. phi1 and phi2 are their delayed version for the purpose of making charge injection signal-independent and preventing leakage. Inverted clocks phi1ab, phi1b, phi2ab and phi2b are also generated for pmos switches. Buffers are added at each output to drive the wiring capacitance and the input capacitance of switches. The rise and fall time were simulated to be less than 1ns for 20 MHz clock input. Non-overlap time is about 1ns and delay between two versions is less than 1ns. A better scheme shown in Fig. 4.12 may be used instead. In this scheme the delay between phi1a, phi1 and phi2a, phi2 is only for the falling edge (sampling edge). More time could be saved for settling.

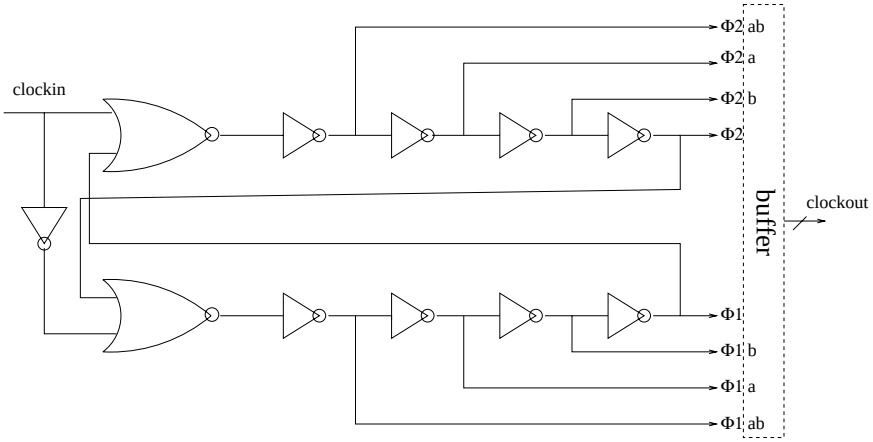

FIGURE 4.11: Schematic of clock generator (version 1)

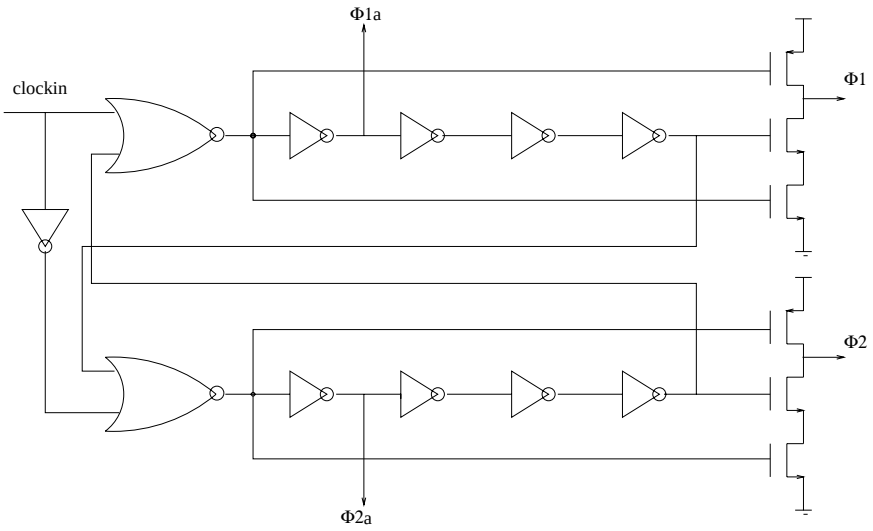

FIGURE 4.12: Schematic of clock generator (version 2)

4.5. Layout Floorplan

The chip will be fabricated in a triple-metal double-poly $0.25\mu m$ CMOS process in Lucent Technologies. The first draft of the layout floorplan is shown in Fig. 4.13. Differential P channel and N channel are strictly symmetrical. Clock lines and digital outputs are routed in the middle. Analog signal lines are routed at both sides. Switches and comparator latches in each stage are put inside guard rings to reduce digital switching noise upon the analog signals. Double-poly capacitors are above the grounded n-well to reduce the interference. Common-centroid geometryand dummy devices are used to achieve good capacitor matching. Power supplies are separated for the analog and digital parts. Decoupling capacitor will fill the empty area inside the chip.

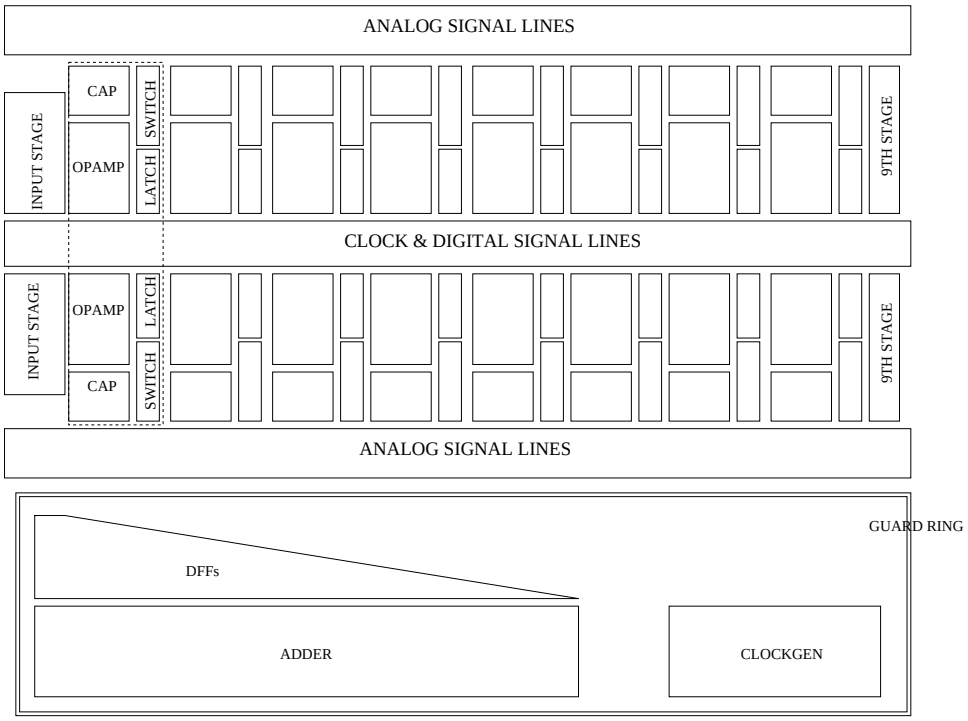

FIGURE 4.13: Layout floorplan of pipeline ADC

5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

In this project, a low-voltage high-speed pipeline ADC was implemented by using a novel low-voltage SC structure different from the other existing techniques. No special process or boosted clock signal are needed. The resolution of the converter is 10 bits and the conversion rate is 20 MS/s. The circuit will be fabricated with Lucent $0.25\mu m$ CMOS process and operate under 1.5 V power supply.

5.2. Potential Problems and Future Work

Although SWITCAP simulation verifies the functionality of the low-voltage converter and Hspice simulation shows that the design target on resolution and speed could be met within normal process variations, there are still some factors which would degrade the final silicon performance:

- Common-mode drift issue

  Since there is no common-mode feedback inside the loop, the common-mode drift caused by the mismatch of capacitors, offset of opamp and charge injection will accumulate stage by stage. Careful design and layout are supposed to minimize the total drift within 100 mV such that the residue output signal will not be out of saturation. But this problem is likely to cause trouble if the common-mode signal is not controlled well as expected.

- Mismatch of capacitors

  In the first two stages the Cs, Cf and Cref are taken to be 0.8pF, 0.4pF and 0.1pF respectively. There is no solid process data to show whether these values are large enough to achieve 10-bit matching (esp. between Cs and Cf). Since the spread ratio of Cs and Cref is 8:1, we cannot use bigger capacitances, otherwise the speed of opamp will be compromised. Since one of the major objective of this project is to verify the speed advantage of the new low-voltage

scheme over the switched-opamp technique, we don't want to compromise the speed too much in favor of resolution. On the other hand, digital calibration could solve the mismatch problems even under low-voltage supply.

- Settling behavior of opamp

  Although the Hspice simulation shows that the speed of opamp is fast enough to settle to the specified value with 10-bit accuracy, it is still likely the opamp will cause trouble due to the inaccuracy of the model, process and temperature variation, etc. In the test phase, the resulting SNDR degradation due to this factor can be distinguished from that from the degradation due to the capacitor mismatch by lowering the sampling clock. Bias current also could be increased to help setting.

To overcome the above potential problems, some works could be done for the future research:

- A closed common-mode feedback loop could be used to suppress the common-mode drift problem of pseudo-differential structure. The feedback loop could be inside each stage or among stages. For the latter the delay between stages will make the stability an issue.

- Substitute the pseudo-differential scheme with a fully-differential one. Thus common-mode problem could be solved. Circuit may be more symmetrical and get better PSRR and charge injection cancellation. Power consumption can also be reduced.

- General digital calibration algorithm could be used to reduce the requirement on opamp DC gain, settling time and capacitor mismatch. No special problem will be encountered for the low-voltage design.

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