IMPLEMENTATION OF A WIDE RANGE DIGITIZER FOR A CHEM-BIO LIDAR

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ABSTRACT

The Frequency Agile Laser (FAL) Sensor is an active standoff chemical detector, developed at the Edgewood Chemical Biological Center (ECBC), for the purpose of remotely sensing chemical warfare agents. The Wide Range Digitizer (WRD) is a small component of the FAL System that provides the necessary data acquisition and processing capability that, in the past, has been one of the major limitations. The WRD receives the analog signals from the LIDAR and, through the use of a unique configuration of A/D converters, can amplify and digitize the signal to a high degree of resolution, without distortion or clipping, regardless of the voltage range. In addition, the WRD uses a custom Digital Signal Processor (DSP) configuration to offload some of the processing capabilities by converting the digitized data into a 32-bit Floating-Point format of the actual voltage value, run a Low-Pass digital filter over the data, and acquire key characteristics of the data needed for the identification phase. The data is then sent to the central control unit via a High-Speed USB 2.0 serial link.

Preliminary results indicate that the WRD system exceeds initial expectations by recreating nearly identical signals to that produced by the laser for a wide range of voltage levels. Moreover, only a fraction of the total processing power of the DSP is used for the acquisition and data processing, which implies that the DSP is capable of handling additional off-chip processing duties. This paper discusses the entire implementation of the WRD system and presents the preliminary testing and results of the system.

1. INTRODUCTION

The *Frequency Agile Laser* (FAL) Sensor is an active standoff chemical detector, developed at the Edgewood Chemical Biological Center (ECBC), for the purpose of remotely sensing chemical warfare agents. The FAL LIDAR operates by transmitting pulses of light at various infrared wavelengths into the atmosphere and measuring the return energy as it is scattered back to the sensor from a hard target and/or an aerosol cloud. One major limitation of the FAL system has been data acquisition and processing capability. The received analog signal in a LIDAR system is detected, amplified, and digitized for subsequent computer processing. Typically, receiver amplifier gain is adjusted so that the signal amplitude applied to the digitizer is not too large, resulting in signal clipping, nor too small, resulting in poor digitizer resolution. In LIDAR applications, the received signal amplitude changes rapidly and thus proper gain adjustment in real-time is difficult. In addition, due to the high frequency with which the received data is sampled, data acquisition is made increasingly difficult.

Therefore, this paper discusses the design and implementation of the *Wide Range Digitizer* (WRD) system that addresses both the amplifier gain issue and the data acquisition problems. The WRD system provides a special A/D digitizer that eliminates the need for manual or automatic gain control amplifier

and off-chip processing capabilities to convert the acquired data into 32-bit floating-point values, run a variety type of digital filters over the acquired data, and communicate with the central control unit via USB. The rest of this paper is organized as follows: Section 2 presents the design approach used for implementing WRD. Section 3 discusses the implementation of the A/D converters. Section 4 covers the Digital Signal Processing unit of the WRD system. Preliminary results are explained in Section 5 and the paper is concluded in Section 6.

2. DESIGN APPROACH

The WRD system is composed of two main components; (1) a unique circuit of Analog-to-Digital (A/D) converters that can convert a wide range of voltage inputs without signal clipping or degradation in data resolution, and (2) a Digital Signal Processing (DSP) component that provides accurate data acquisition, conversion, and filtering on the LIDAR received signals. Four A/D converters, each with a progressively higher voltage range, are configured in a circuit in which the input signal is applied simultaneously to all A/D converters. A/D voltage ranges are, ± 0.55 volts, ± 1.1 volts, 0 to 2 volts, and 0 to 4 volts. Digital output signals are selected from the A/D converter having the lowest voltage range, which is not exceeded by the input signal. This digital data comprises of 16-bit words, which are sent to the DSP. Two of the A/D converters have a 2's complement, 14-bit binary output signal and the other two have a 12-bit straight binary output signal. The two MSB in the word comprise the A/D identifier that is used by the DSP.

The DSP is synchronized to the A/D in a way to accurately capture each generated digital value. In addition, the DSP off loads some of the processing power from the Central Control Unit (CCU) by converting the binary data into a more useable 32-bit floating-point representation of the actual voltage values. The DSP can be configured to run any type of digital filter that is required on the data. The preprocessed data is then sent to the CCU through a high-speed USB 2.0 serial link. A custom USB configuration allows CCU to control all aspects of the WRD's data acquisition and processing capabilities. Figure 1 shows a block diagram of the overall WRD implementation.

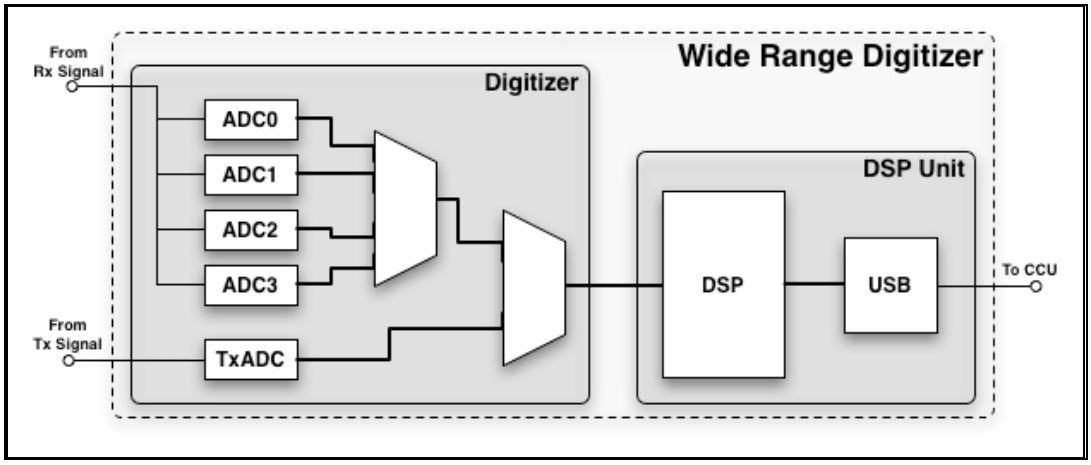

Figure 1. A block diagram representing the WRD system.

3. ANALOG-TO-DIGITAL CONVERTERS

The digitizer configuration requires multiple A/D circuits, with progressively higher input voltage ranges. Although the voltage ranges differ, many A/D characteristics must match to insure seamless operation over the entire input voltage range. These matching characteristics include operating frequency and pipeline delay (latency) of both output and OTR (out-of-range) signals. For circuit design simplification, it is desirable that digital output levels and power supply requirements match. A/D voltage ranges

were dictated by the FAL preamplifier characteristics as well as specifications of the A/D integrated circuits. Although most FAL preamplifier output signals are positive, the circuit is AC coupled and produces some small negative signals. Maximum preamplifier output voltage is +1.2 volts. For compatibility with the present FAL signal, the digitizer will accommodate bipolar input signals.

The Analog Devices AD6645, 14-bit A/D, was selected for the two lowest voltage digitizer stages. This is a 14-bit 2's complement A/D, which satisfies the bipolar signal requirement with adequate signal resolution. The most sensitive digitizer stage includes a preamplifier with gain of 2, to extend the input voltage range from ±1.1 to ±0.55 volts. The second stage utilizes the AD6645 without pre-amplification to provide an input voltage range of ±1.1 volts. The two higher voltage stages use the AD9224, which is coded in straight binary since large bipolar signals are not encountered. The third stage voltage range is 0 to 2 volts and the fourth stage range is 0 to 4 volts. Input voltage range of the AD9224 is changed from 2 volts to 4 volts by a reference voltage modification. To take advantage of the 4-volt range of the AD9224, an analog amplifier with gain of 3.54 is interposed before the A/D converters.

4. DIGITAL SIGNAL PROCESSOR IMPLEMENTATION

The DSP acts as the control unit for the WRD system by facilitating user initiated commands while simultaneously acquiring, processing, and packaging the digitized LIDAR signals from the A/D converters. An Analog Devices ADSP-21262 SHARC Processor was chosen as the DSP component for its dual, dedicated bus lines, data acquisition capabilities, and SIMD architecture that allow for efficient execution of the digital filter. Figure 2 illustrates the DSP configuration along with the two other major components; (1) a Cypress Semiconductor CY7C68001 FX2 USB Controller and (2) a Quick Logic QL3012 pASIC FPGA.

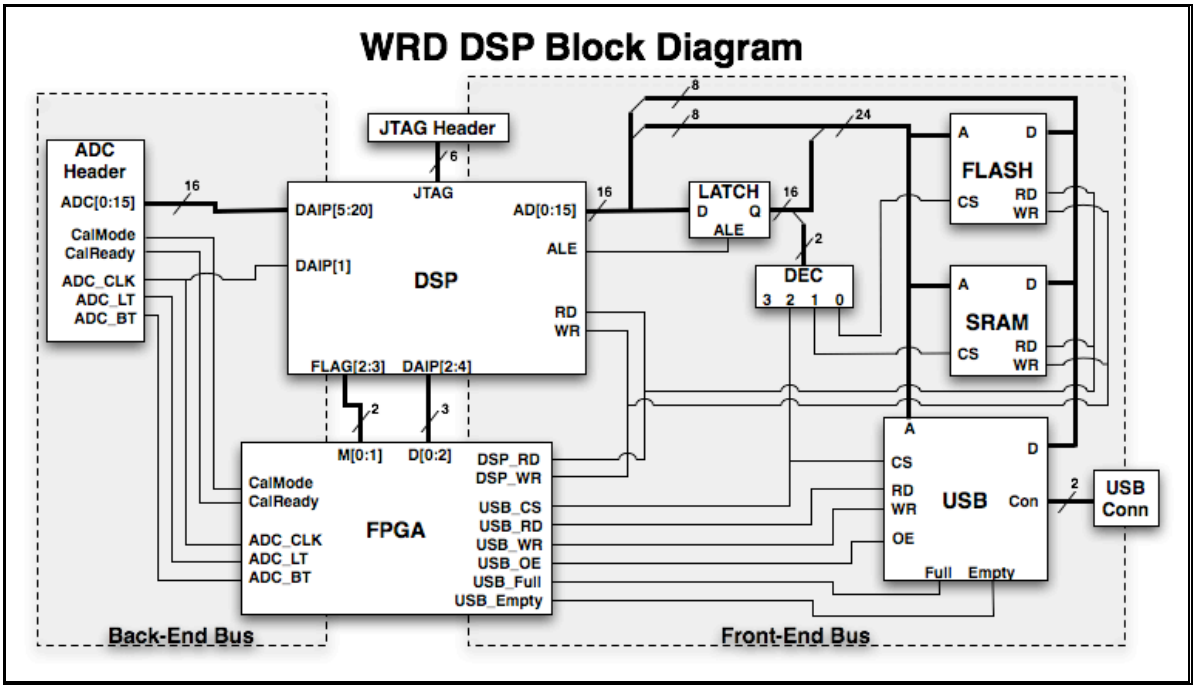

Figure 2. A block diagram of the DSP component.

A/D data is acquired through a 16-bit, back-end data bus. In order to meet the LIDAR requirements, the back-end bus is synchronized to the A/D clock and can capture up to 2500, 16-bit data words for the receive signal, plus an additional 1000 data words for the LIDAR transmit signal every 5 ms. The LIDAR can transmit up to 20 laser lines per second, which compromises a laser signal burst. In order to

facilitate data synchronization, a Laser Trigger signal is sent to the DSP indicating the beginning of each laser line and a Laser Burst signal is sent to indicate the beginning of a laser burst period. Once initiated for data acquisition, the DSP configures the back-end bus to start acquiring the data based an external control signal, thus insuring that no data elements are lost due to initialization overhead.

Once a line of laser data has been acquired, the DSP will begin converting the 16-bit binary data to a 32-bit floating-point voltage value. The actual binary data is first isolated based on the 2-bit A/D identifier and then an appropriate offset value is subtracted from the binary data. Finally, the remaining binary value is converted to a 32-bit floating-point value and multiplied by the appropriate A/D multiplier value. Both the A/D voltage offset and voltage multiplier are calculated by the DSP during the calibration phase initiated by the user.

The front-side bus consists of a standard 8-bit parallel data bus with a 24-bit address line. A non-volatile FLASH chip is used to hold the DSP firmware, which is loaded into the DSP automatically upon power-on. An external SRAM is used to temporally hold each laser line data since the DSP's internal memory is not sufficient enough to hold all 20 lines of 3500 values. As each line of data is acquired, it is then converted to a 32-bit floating-point representation of the voltage value and then sent to the SRAM. Once all 20 lines of data have been received and processed, each line is applied with a digital filter, packaged with a custom header file, and sent to the USB controller.

The USB controller facilitates communication between the DSP and the CCU by supporting high-speed USB 2.0 protocols. The USB is also connected to the DSP by the front-side bus and is accessed as a typical external memory. A high-speed, USB Bulk Transfer protocol is incorporated into the USB controller as the primary transfer method and data is temporarily buffered into one of two Endpoint USB FIFOs. The USB Controller's internal hardware automatically facilitates USB communication when a data is written to the IN FIFO from the DSP. In addition, special command packets can be sent to the USB controller from the CCU. When a command packet is received, the USB Controller will interrupt the DSP and the DSP will read in the command to perform the necessary action.

Unfortunately, the USB FIFO configuration was not designed for fast memory access such as the SRAM or FLASH. Therefore, an FPGA is needed to alter the DSP's Read and Write strobes so that they can be correctly interpreted by the USB. Moreover, the FPGA expands the DSP's I/O capability by expanding five of the DSP External Flag I/O signals into 12 multiplexed I/O signals. The new signals provided enough I/O signals to properly handle the necessary signal communication for the system.

5. USER INTERACTION

The WRD is designed to adapt to the current needs of the FAL system and incorporates the ability to accept user-initiated commands via USB. The commands can control all aspects for the WRD system including the number of lines to capture, the size of the lines, and even providing the ability to only capture a window of laser data. In addition, the DSP firmware is integrated with generic FIR and IIR filters, which may be necessary when trying to isolate specific return signals. The user can upload the coefficients for either a types of filters, thus allowing the ability to run any type of digital filter over the data.

Another vital feature of the WRD is the ability for the user to have the DSP calibrate the WRD system by computing the voltage offset and multiplier values for each A/D. The calibration routine begins with additional circuitry that supplies both a known voltage values for each A/D and then a constant voltage ramp function. The DSP will then determine the offset voltages by averaging the received data values from the A/D and subtracting the known voltage. The multiplier is then statistically calculated from the voltage ramp using a 16-point linear regression algorithm to insure a smooth transition in values across A/D voltage boundaries.

6. PRELIMINARY RESULTS

Initial testing of the WRD system was performed with off-the-shelf demo boards for the DSP, USB, and FPGA at Oregon State University. These boards were correctly configured and wired together to accurately prototype the entire DSP system. Example A/D data and timing signals were built into a custom WRD test box that simulated the actual A/D digital data transfers. Using this system, the current DSP implementation was found to be accurate and returned the exact voltage values for each test that were used to generate the A/D data.

In addition, it was found that the current DSP exceeded expectations by leaving ample room for additional processing capabilities. For each 5 ms of line data, the DSP acquired the data within 67.56 μs, converted the data in 461.1 μs, and sent the entire line of data to the SRAM in 187.5 μs, leaving the DSP running idly for the remaining 4.28 ms. Per each laser burst of one second intervals, 100 ms were need to capture 20 lines of data and 29.76 ms were needed to fetch each line of data from the SRAM, run the digital filter, and transmit all the lines over the USB connection. This left the DSP idle for 870.24 ms and when including the idle time in each 5 ms line acquisition, the DSP was at an idle state for a total of 955.84 ms or 95.6% of the time. This indicates that the WRD system can perform a significantly more amount of off-chip processing on the capture LIDAR data, and thus reducing the processing load on the CCU.

Currently, the WRD system is in the final stages of implementation at ECBC in a vector-board prototype form. The WRD system will then be installed into the actual FAL system for field-testing and evaluation.

7. CONCLUSION

This design eliminates the need for manual or automatic gain control amplifiers in the LIDAR data acquisition process and provides off-chip processing of the LIDAR data. The digital signal resolution is maintained for small signals, yet large amplitude signals are not distorted due to signal clipping. The processing capabilities of the DSP far exceeded initial expectations and leaves room for future processing capabilities.

ACKNOWLEDGEMENTS

The assistance of Senior Technician, Mr. Stanley Businsky of STC in wiring, fabricating, and testing the electronics hardware and preparing drawings is acknowledged and greatly appreciated. The valuable assistance in the software designed provided by Mr. Pascal Lim and Mr. Kevin Hung of Advanced Technologies and Applications, Inc. is acknowledged and appreciated.