ECE/CS 472/572
Computer Architecture:
Concluding Remarks

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Spring 2016
Key Concepts: Part I

- **Instruction Set Architecture (ISA)**
  - Performance, speedup
  - CPU time = Instruction Count x CPI x Clock cycle time
  - MIPS: R-format, I-format, J-format, addressing mode
  - RISC vs. CISC

- **Single-Cycle Processor**
  - Components, Combinational & Sequential, Clocking
  - Datapath: Add/Sub, load/store, branch/jump
  - Control: Main control unit, ALU control
  - Put together
Single-Cycle Processor
Key Concepts: Part II

- Pipelined Processor
  - 5-stage: IF - ID - EX - MEM - WB
  - Datapath & How pipeline increases performance
  - Hazard: Structure, Data, and Control hazards
  - Solution 1: Insert Stall (Bubbles), where & how many
  - Solution 2: Forwarding
    - Within registers, EX->EX, EX->MEM (datapath & detecting)
    - Load-use data hazard
  - Solution 3: Code scheduling
  - Solution 4: Branch prediction, static & dynamic
  - Pipeline Control: carry signals along the stages
  - Put together
Final datapath and control
Key Concepts: Part III

- Memory Hierarchy
  - Principle of Locality: Temporal & Spatial
  - SRAM – DRAM – Flash SSD/Disk

- Cache
  - Basic concepts: hit/miss, AMAT, write-back vs. write through, replacement, multi-level, 3-C model
  - Structure: tag, block, valid bit, index, offset
  - Associativity: direct mapped, set & fully-associative
  - Interaction w/ CPUs and Software (sorting example)

- Virtual Memory
  - Physical vs. virtual address, page table, TLB
  - TLB miss, page fault, replacement, writes
Broader Vision

- **Real examples**
  - Opening the iPad, A5 processor
  - ARM Cortex-A8 and Intel Core i7

- **Terminology**
  - ITRS, Superpipeline, Superscalar, Static multiple Issue, Dynamic multiple Issue (Tomasulo), Speculation, VLIW, ILP, MLP, TLP, Multithreading, SISD, MIMD, SPMD, SIMD, Massive parallel processing, GPGPU, on-chip networks

- **Videos**
  - How computer is made ([link](#))
  - Thermal issue in CPUs ([cooling](#), [cooking](#))
  - 3D NAND Memory by Micron & Intel ([link](#))
  - HPC simulations for Science and Industry ([link](#))
Broader Vision

- Special Topics
  - Terminology
  - Security and AES
  - Abstract and Virtual Machines
  - Computer architecture in machine learning
Research Openings

- Multiple openings available in the STAR Lab
  - HPC/datacenters, GPUs, Acceleration for deep learning, wearables, security in processors, dark silicon, ...

- Requirements
  - Get an A from this class
  - Major in CS (or ECE with strong coding in C++)
  - Interested in doing research

- What you need to do
  - Send me an email with your CV
  - If selected, work with me for some time to prove yourself
CS519 / ECE599 in Fall 2016

- GPU Architecture
  - TR 8:30-9:50, 4-credit, prerequisite 472/572
  - Load: 1 HW, 1 paper presentation, 1 project
  - Might be 1 take-home exam
CS519 / EE599 in Winter 2017

- Interconnection Networks
  - Time/location: TBD, 4 credits
  - Load: 1 HW, 1 paper presentation, 1 project
  - On-chip networks & Off-chip networks
  - HPC Matters ([link](#))
Course Evaluation Reminder

- eSET is open from 5/30 to 6/13
- Very important to me; your participation is greatly appreciated 😊