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**Project:** Inter-stage gain amplifier for a 13-bit 100Msamples/sec two-step ADC

**Due Date:** Jun. 8, 2009 8am PST

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The objective of this project is to design a fully differential feedback amplifier (shown in Fig. 1) used to generate the *residue* for the second stage of a two-step analog-to-digital converter (ADC). The first stage of the ADC resolves 2 bits and the second stage resolves rest of the 11 bits. While a practical residue amplifier is implemented as a switched-capacitor circuit, the main focus of this project is only on the amplifier design. The primary goal is to achieve the specifications given in Table 1 with minimum power consumption.

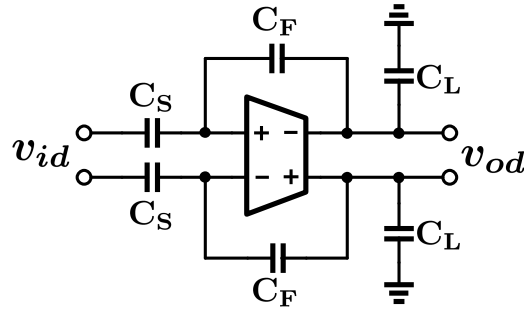


Figure 1: Inter-stage gain amplifier schematic.

Table 1: Amplifier specifications

Technology	ECE520 0.18 $\mu$ m CMOS
Supply voltage	$\leq 1.8$ V
Closed loop gain	4
Settling error (static + dynamic)	$\leq 2.5 \times 10^{-4}$
Load capacitance ( $C_L$ )	2pF
Settling time	$\leq 5$ ns
Peak SNR	$\geq 66$ dB
THD	$\leq -70$ dB
Power consumption	Minimum

$$\text{Peak SNR} = \frac{\text{Maximum signal power}}{\text{Total noise power}}$$

$$\text{Total Harmonic Distortion (THD)} = \frac{\sum_{i=2}^6 \text{i}^{\text{th}} \text{harmonic power}}{\text{Fundamental frequency power}}$$

## Report Guidelines

The report should describe all the design choices you made with justification, present relevant simulation results and should **not exceed 15 pages**. The report should **strictly adhere** to the following outline:

- (1) Overall design approach with emphasis on system level trade-offs and the design choices made to arrive at your amplifier architecture should be presented in the first page. You should explain your design decisions and compare the tradeoffs with alternative choices.
- (2) Clearly drawn complete amplifier schematic (do not cut-and-paste Cadence schematic) along with tabulated device sizes, bias currents,  $g_m$ s, and  $\Delta$ s of all the devices should be shown in the second page. Indicate the transistors operating in triode region separately.
- (3) The simulated performance summary of the amplifier should be given in page 3 (see example performance summary table shown in next page).
- (4) All the relevant calculations to achieve the simulated performance should be provided in pages 4 and 5.
- (5) Clearly annotated simulated results as specified below should be presented in pages 6-11.
  - (page 6) Differential-mode loop-gain AC response (magnitude and phase) with clearly marked DC gain, loop-gain bandwidth, and phase- and gain-margins.
  - (page 7) Differential-mode DC loop gain versus differential output swing.
  - (page 8) Common-mode loop-gain AC response (magnitude and phase) with clearly marked DC gain, loop-gain bandwidth, and phase margin.
  - (page 9) Positive step response with maximum-allowed input step and clearly marked settling time and settling error on a separate zoomed-in plot.
  - (page 10) Negative step response with maximum-allowed input step and clearly marked settling time and settling error on a separate zoomed-in plot.
  - (page 11) Integrated differential output noise versus frequency plot (integrate noise from 100Hz to 100GHz). See slide 42 of handout 5 for an example.
  - (page 12) Output spectrums of  $\sim 1$ MHz and  $\sim 49$ MHz output sine-waves with maximum-allowed output swing. Use 4096 point FFT.
- (6) References and an appendix for additional information in the last couple of pages.
- (7) Use L<sup>A</sup>T<sub>E</sub>X or MS WORD to type-set your report and name the report as lastname1\_lastname2.pdf.
- (8) Submit the tarred and gzipped Cadence directory along with project report by e-mail.

## Grading

Design choices and justification .....	35%
Results presentation (report clarity) .....	30%
Functionality & performance .....	25%
Novelty .....	10%

Table 2: Performance summary

Design parameter/variable	Simulated performance	Specification
Supply voltage		$\leq 1.8V$
Closed loop gain		4
Settling error (static + dynamic)		$2.5 \times \leq 10^{-4}$
Load capacitance ( $C_L$ )		2pF
Settling time		$\leq 5ns$
Peak SNR		$\geq 66dB$
Differential r.m.s noise voltage [ $\mu V$ ]		–
THD ( $F_{in} = 1MHz$ )		$\leq -70dB$
THD ( $F_{in} = 49MHz$ )		$\leq -70dB$
Amplifier core power consumption [mW]		Minimum
Bias power consumption [mW]		Minimum
Total power consumption [mW]		Minimum
Differential DC loop gain ( $v_{od} = 0$ ) [dB]		–
Differential DC loop gain ( $v_{od} = v_{od,max}$ ) [dB]		–
Differential loop-gain unity gain bandwidth [MHz]		–
Differential loop-gain phase margin [deg]		–
Differential loop-gain gain margin [dB]		–
Common-mode loop-gain unity gain bandwidth [MHz]		–
Common-mode loop-gain phase margin [deg]		–