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**Project:** Low power, wide-operating range phase-locked loop

**Due Date:** Mar. 11, 2008 8am PST

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The objective of this project is to design a complete phase-locked loop circuit operating over a wide frequency range with a low-frequency reference clock, while seeking to minimize the overall power consumption. The target specifications are given in Table 1.

Table 1: PLL Specifications

Technology	ECE599 0.18 $\mu$ m CMOS
Supply voltage	< 1.8V
Operating frequency	100MHz – 500MHz
Fixed feedback divider	1024
Absolute jitter	0.1% of the period (rms)
Power consumption	Minimum

## Report Guidelines

The report should describe all the design choices you made with justification and should not exceed 5 pages. The outline of the report should be as follows:

- (1) The first page should give an overall description of the PLL architecture with emphasis on system level trade-offs and the design choices you made to arrive at the presented architecture. You should explain how you chose the PLL bandwidth and phase margin to minimize both power and jitter simultaneously. A plot indicating the noise contribution of all the blocks and the overall noise performance of the PLL can be used to illustrate your design choices. Tabulate all the component values and appropriate simulated gain of each of the blocks and show the total PLL power and jitter. Draw a pie-chart for the power dissipation of each of the blocks. Use L<sup>A</sup>T<sub>E</sub>X or MS WORD to type-set your report.
- (2) Pages 2, 3, and 4 should elaborate on the design of the individual blocks of the PLL. Show clearly drawn schematics, simulated waveforms, transfer functions, and noise analysis of each of the blocks. Emphasize the design tradeoffs and focus on the design choices made.
- (3) On the last page, summarize your work along with conclusions drawn from your experience. Do not forget to have a references section quoting all the work you used from the literature.

## Grading

Design choices and justification	30%
Results presentation (Report clarity)	20%
Functionality & performance	15%
Novelty	10%
Oral presentation	30%
Lowest power (Bonus)	10%