

# ECE520: Analog CMOS Integrated Circuits

T/TR 4:00 - 5:50pm, Room: KEAR 205

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**Instructor:** Pavan Kumar Hanumolu, [hanumolu@eecs.oregonstate.edu](mailto:hanumolu@eecs.oregonstate.edu)  
**Office:** KEC 4097, Ph: 737-2178  
**Office hours:** Walk-in or by appointment  
**Textbook:** No text book required  
**Prerequisites:** ECE423 or equivalent  
**Course website:** <http://web.engr.oregonstate.edu/~hanumolu/ece520.htm>

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**Course Description:** Analysis and design of transistor-level circuits in CMOS technology. Emphasis on fundamental understanding, design intuition, and implementation of transistor-level analog circuits in modern-day CMOS processes. Topics include single-, multi-stage amplifier design, compensation techniques, electronic noise, output stages, and power-management circuits.

## Grading Policy:

Homework .....	25%
Midterm - I ( <b>April 23</b> ) .....	25%
Midterm - II ( <b>May 21</b> ) .....	25%
Project .....	25%

## Reference books:

- P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4<sup>th</sup> Edition, Wiley, 2001.
- B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Science, 2000.
- D. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, 1996.
- R. Gregorian and G. Temes, *Analog MOS Integrated Circuits for Signal Processing*, Wiley, 1986.
- K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994.
- P. Allen and D. Hollberg, *CMOS Analog Circuit Design*, Oxford University Press, 2002.
- Y. Tsvividis, *Operation and Modeling of the MOS Transistor*, Oxford University Press, 2003.
- A. Hastings, *Art of Analog Layout*, Prentice Hall, 2005.

### Tentative course outline

Date	Topic	HW/Projects
Tue. March 31	Course overview	
Thu. April 2	Passives in CMOS technology	
Tue. April 7	MOS transistor	
Thu. April 9	Basic building blocks (review)	HW # 1 due
Tue. April 14	Basic building blocks (review)	
Thu. April 16	$g_m/I_d$ design methodology	HW # 2 due
Tue. April 21	Differential OTAs (CMFB)	
Thu. April 23	Midterm - I	HW # 3 due
Tue. April 28	Noise	
Thu. April 30	Noise	HW # 4 due
Tue. May 5	Transient response	Project out
Thu. May 7	Compensation	HW # 5 due
Tue. May 12	Compensation	
Thu. May 14	Feedback stability	HW # 6 due
Tue. May 19	Noise in feedback circuits	
Thu. May 21	Midterm - II	
Tue. May 26	Power management circuits	
Thu. May 28	Power management circuits	HW # 7 due
Tue. June 2	Power management circuits	
Tue. June 4	Guest Lecture	Project due