ECE599: Phase-locked loops T/TR 4:00 - 5:50pm, Room: KEC 1005

Instructor:	Pavan Kumar Hanumolu, hanumolu@eecs.oregonstate.edu
Office:	KEC 4097, Ph: 737-2178
Office hours:	By appointment
Textbook:	No text book needed
Prerequisites:	ECE599: Phase-Locked Loops – I
Course website:	http://web.engr.oregonstate.edu/∼hanumolu/ece599.htm

Course Description: Analysis and design of advanced phase-locked loop (PLL) architectures and circuits for communication systems. Emphasis on behavioral modelling, system simulation, and circuit implementation of PLLs in modern-day CMOS processes. Topics include supply-regulated PLLs, delay-locked loops, fractional-N PLLs, digital PLLs, and clock and data recovery circuits.

Course Outline:

Week 1 ..... Introduction; Basic charge-pump PLLs
Week 2 ..... Alternate charge-pump PLL architectures
Week 3 ..... Supply-regulated PLLs
Week 4 ..... Self-biased and bandwidth-tracking PLLs
Week 5 ..... Delay-locked loops
Week 6 ..... Fractional-N synthesizers
Week 7 ..... Digital PLLs
Week 8 ..... Clock and data recovery PLLs
Week 9 ..... Clock and data recovery PLLs
Week 10 ..... Miscellaneous topics

Grading Policy:

Project-I 25%
Project-II 25%
Project-III 25%
Project-IV 25%

Reference books:

- F. Gardner, *Phaselock Techniques*, John Wiley & Sons, 2005.
- D. Wolaver, *Phase-Locked Loop Circuit Design*, Prentice-Hall, 1991.
- W. Egan, *Phase-Lock Basics*, John Wiley & Sons, 1998.
- R. Best, *Phase-Locked Loops : Design, Simulation, and Applications*, McGraw Hill, 2003.

Date	Topic	Projects
Tue. Sep. 30	Course overview, Charge-pump PLLs	
Thu. Oct. 2	Proportional-integral control schemes	
Tue. Oct. 7	Split-tuned PLLs	Project-I out
Thu. Oct. 9	Supply-regulated PLLs	
Tue. Oct. 14	Regulator design	
Thu. Oct. 16	Self-biased PLLs	
Tue. Oct. 21	Bandwidth tracking PLLs	Project-I due, Project-II out
Thu. Oct. 23	Delay-locked loops	
Tue. Oct. 28	Multiplying delay-locked loops	
Thu. Oct. 30	Fractional-N synthesizers	
Tue. Nov. 4	Delta-sigma fractional-N synthesizers	Project-II due, Project-III out
Thu. Nov. 6	Digital PLLs	
Tue. Nov. 11	Digital PLL building blocks	
Thu. Nov. 13	Clock and data recovery basics	
Tue. Nov. 18	Clock and data recovery architectures	Project-III due, Project-IV out
Tue. Nov. 20	Clock and data recovery building blocks	
Thu. Nov. 25	Data recovery in source-synchronous interfaces	
Tue. Nov. 27	Thanksgiving	
Tue. Dec. 2	Direct digital frequency synthesis	
Tue. Dec. 4	Course summary	Project-IV due