Zirconium oxide-aluminum oxide nanolamine gate dielectrics for amorphous oxide semiconductor thin-film transistors

T. Waggoner, J. Triska, K. Hoshino, J. F. Wager, and J. F. Conley, Jr.1
Oregon State University, School of EECS, 1148 Kelley Engineering Center, Corvallis, Oregon 97331-5501

(Received 18 February 2011; accepted 1 June 2011; published 10 August 2011)

The dielectric properties of ZrO2–Al2O3 nanolaminates, deposited via atomic layer deposition, and their impact on the performance and stability of indium gallium zinc oxide and zinc tin oxide amorphous oxide semiconductor thin-film transistors (TFTs) are investigated. It is found that nanolaminate dielectrics can combine the advantages of constituent dielectrics and produce TFTs with improved performance and stability compared to single layer gate dielectrics. It is also found that TFT performance and stability are influenced not only by the chemical composition of the gate dielectric/channel interface but also by the thickness and composition of the laminate layers in the dielectric near the interface. © 2011 American Vacuum Society. [DOI: 10.1116/1.3609254]

I. INTRODUCTION

Thin film transistors (TFTs) fabricated using amorphous oxide semiconductors (AOSs) are transparent, exhibit good electron mobility (in the general range of 1–30 cm2/V s), and can be processed at low temperature.1–8 This new class of materials shows promise for application in active-matrix organic light-emitting diode (AMOLED) displays,9–11 large-area, high-performance active-matrix liquid crystal displays12 (AMLCDs), and e-paper.13 Commercialization of these applications will require optimization of TFT performance and reliability.14–22 It is well known that the performance and stability of field-effect devices such as TFTs depends critically on the gate dielectric and its interface with the active channel and it has been shown recently that a thin dielectric interfacial layer can dominate AOS TFT stability.20–22 The use of multilayer or nanolaminate gate dielectrics can allow for independent tuning of the properties of the dielectric/channel interface and bulk dielectric.

Atomic layer deposition (ALD) is a highly conformal and uniform technique with inherent atomic-scale control of thin film composition, making it ideally suited for deposition of nanolaminates.23,24 Previous work has shown that ALD nanolaminates can exhibit superior performance to single layer gate dielectrics in metal/oxide/silicon (MOS) structures25–30 and perform well as passivation and diffusion barriers for AOS TFTs.31 Very little work has been reported on the use of ALD nanolaminates as AOS TFT gate dielectrics. Although ALD nanolaminates of Al2O3–TiO2 (ATO), typically supplied by Planar Systems, have been used as gate dielectrics for AOS TFTs, there is little information reported about the material.31–33 Most ATO work in literature has focused on dielectric characterization for use in MOS technologies.29,34–36

In this work, we use ALD to deposit ZrO2–Al2O3 (ZAO) nanolaminates of various structure, composition, and surface termination at the AOS channel interface and investigate their impact on the performance and stability of TFTs made using two of the most promising AOS materials, zinc tin oxide (ZTO), and indium gallium zinc oxide (IGZO). We find that ZAO nanolaminate dielectrics can be tuned to combine the bulk advantages of the constituent dielectrics—the high dielectric constant of ZrO2 and the low leakage of Al2O3. By using the proper nanolaminate bilayer structure, interfacial material, and thickness/composition of the near-interfacial layers, we were able to improve overall performance compared to TFTs made using single layer films of either Al2O3 or ZrO2.

II. EXPERIMENT

A. Device fabrication

A schematic cross section of the staggered, bottom-gate (SBG) AOS TFTs used in this study is shown in Fig. 1. A heavily doped (0.05 Ω cm) p-type Si substrate served as a bottom-gate contact. 25 × 25 mm2 p-type Si coupons were cleaned with consecutive rinses of acetone, isopropyl alcohol, and 18 M Ω cm de-ionized water, followed by dehydroxylation in an oven at 125 °C for 15 min. Immediately following this procedure, the gate dielectric was deposited via thermal ALD using a Picosun Sunale R-150 reactor. ZrO2 was deposited at 250 °C using alternating pulses of tetrakis(ethylmethylamido)zirconium (TEMAZ) and H2O. Al2O3 was deposited at 250 °C using trimethylaluminum (TMA) and H2O. ZAO nanolaminates were deposited at 250 °C in a single ALD run. ZAO nanolaminates are composed of alternating pairs of ZrO2 and Al2O3 layers, which we refer to as bilayers. Shown in Fig. 2 is a schematic cross section of a ZAO nanolaminate delineating total thickness, bilayer thickness, and individual layer thickness. Nanolaminates were deposited with bilayer thicknesses of 5, 10, and 20 nm. Nanolaminate compositions of roughly 25%, 50%, and 75% overall ZrO2 content were synthesized by varying the thickness ratio of the ZrO2 and Al2O3 layers in each bilayer. For example, a 200 nm thick, 10 nm bilayer, 75% ZrO2 content ZAO laminate film would have a ZrO2 layer thickness of approximately 7.5 nm, and an Al2O3 layer thickness of ap-
approximately 2.5 nm. In order to enhance the initial nucleation of ZrO₂ on the Si substrate for the nanolaminates that would begin with ZrO₂, depositions begin with an initial ten ALD cycles of Al₂O₃. For nanolaminates that begin with Al₂O₃, ten extra cycles of Al₂O₃ are added for consistency. The thickness of single layer ZrO₂ and Al₂O₃ films was measured using a spectroscopic ellipsometer. The thickness of individual layers in nanolaminates was estimated from the experimentally determined ALD deposition rates of Al₂O₃ (~0.089 nm/cycle) and ZrO₂ (~0.079 nm/cycle).

Following deposition of the gate oxide, an approximately 60 nm thick AOS channel layer of either ZTO or IGZO was deposited via rf magnetron sputtering at a pressure of 5 mTorr in a 90/10 Ar/O₂ atmosphere. No additional clean was performed between the gate dielectric deposition and AOS channel deposition. A shadow mask was used to define active regions of 100 μm in length and 1000 μm in width, giving a W/L ratio of 10. ZTO was deposited in an AJA Orion V using a 3 in. ZTO target (AJA) and a rf power of 100 W. IGZO was deposited using a custom-built sputtering system with a 3 in. IGZO target (Cerac) and a rf power of 100 W. Following deposition, IGZO films were annealed at 300 °C for 1 h with a 2 °C/min ramp rate. IGZO films received a postdeposition annealing for 1 h at 400 °C with a 5 °C/min ramp rate. Finally, the SBG TFT structures were completed by thermally evaporating Al through a shadow mask to form source and drain contacts.

In addition to TFTs, metal-insulator-semiconductor (MIS) devices with 40 nm thick dielectrics were prepared on both lightly doped (12–15 Ω cm) and heavily doped (50–80 m Ω cm) p-type Si. Evaporated Al dots with nominal areas of 1.3 × 10⁻⁴, 2.5 × 10⁻⁴, and 5.1 × 10⁻⁴ form the top metal contact for the MIS devices.

B. Electrical characterization

All electrical measurements were performed in a dark box in atmosphere at room temperature. Capacitance versus voltage (C-V) measurements (100 kHz) were performed on MIS structures with lightly doped Si substrates using an Agilent E4980A LCR meter. The relative dielectric constant (κ) of the dielectric stack was extracted from the slope of the accumulation capacitance versus device area. Current density versus field (J-ξ) measurements were performed on MIS structures with heavily doped Si substrates using an Agilent 4155B semiconductor parameter analyzer. Leakage current density and breakdown strength were extracted by grounding the back contact and sweeping the gate voltage in +100 mV increments at a sweep rate of approximately 200 mV/s until irreversible breakdown occurred.

Double-sweep Id-Vgs transfer curves were taken on SBG TFTs using an Agilent 4155B with VDS held at +1 V. One double-sweep consists of an initial hold time of 5 s, followed by ramping VGS from +20 V to −5 V and then back to +20 V in 100 mV steps with a sweep rate of approximately 200 mV/s. To stabilize operation, a total of 5 double sweeps was performed. The fifth transfer curve was analyzed for VON, subthreshold swing (S), the ION/Ioff ratio, hysteresis (∆Vhys), and incremental electron mobility (μinc). VON was empirically defined as the onset of 1 nA of drain current in the log(Id)-Vgs transfer curve.7,37 S was defined as the inverse maximum slope of the positive to negative sweep log(Id)-Vgs trace and is reported in units of mV/decade of current. ION current was measured at 10 V above VON. Ioff was taken at VDS=-5 V; both were extracted from the positive to negative sweep log(Id)-Vgs trace so that Ioff is fairly constant with respect to VGS. ∆Vhys was extracted as the difference in VON between positive and negative sweeps. Following Hoffman,37 μinc was extracted from Id-Vgs curves using

\[
\mu_{inc}(VGS) = \lim_{VDS \to 0} \left[ \frac{\partial G_d(VGS)}{\partial VGS} \frac{W}{C_G \cdot L} \right],
\]

where Gd is the channel conductance, CG is the geometric capacitance of the gate oxide, and W and L are the width and length of the transistor. For each device, μinc is reported at 10 V above VON. To assess device stability, long term bias stressing was performed with VGS=+20 V and VDS=+1 V. Stress was interrupted at approximately logarithmic time intervals to measure Id-Vgs transfer curves.
approximately 3.4 MV/cm for ZrO$_2$. As expected, nanolaminate breakdown strength tended to decrease with increasing ZrO$_2$ content, with the exception of the 25% ZrO$_2$ content film, which showed an increased average breakdown strength over the single layer Al$_2$O$_3$. Bilayer thickness (not shown) did not have a strong impact on the average breakdown strength of the nanolaminates. The shape of the $J$-$\xi$ curve is a function of ZrO$_2$ content, indicating the dominance of different conduction mechanisms for the Al$_2$O$_3$, ZrO$_2$, and ZAO laminate films. For the 25% and 50% laminates, the conductive “knee” (the field at which the leakage slope increases but breakdown does not occur) occurs at higher fields than for the Al$_2$O$_3$ film whereas in the 75% ZrO$_2$ film, this “knee” occurs at a lower field. Because of this, the influence of ZrO$_2$ content on $J$ is a function of $\xi$.

Shown in Fig. 5 are plots of the average current density ($J_{\text{AVG}}$) versus ZrO$_2$ content for the devices shown in Fig. 4, extracted at electric fields of (a) 1 MV/cm and (b) 4 MV/cm. Also included in Fig. 5 are data from ZAO nanolaminates with bilayer thicknesses of 10 and 20 nm. Once again, data points at 0% and 100% ZrO$_2$ content refer to single layer Al$_2$O$_3$ and ZrO$_2$ dielectrics, respectively. At low fields of 1–2 MV/cm, typical of TFT operation, $J_{\text{AVG}}$ increases only weakly with increasing ZrO$_2$ content. Between the single layer Al$_2$O$_3$ films and the 75% ZrO$_2$ laminates, $J_{\text{AVG}}$ increases by less than a factor of 2. Once again, bilayer thickness did not appear to have a strong effect.

At 4 MV/cm [Fig. 5(b)], the relationship between leakage current density and ZrO$_2$ content is more complex. In all cases, the 25% ZrO$_2$ content films exhibited much lower leakage than the single layer Al$_2$O$_3$ films. At 50% ZrO$_2$ content, both the 5 and 10 nm bilayer films still showed lower leakage than the single layer Al$_2$O$_3$ while the 20 nm bilayer films were slightly higher. It is not until the laminate films reach 75% ZrO$_2$ content that they all exhibit higher leakage than the single layer Al$_2$O$_3$ films. At 4 MV/cm, all of the single layer ZrO$_2$ films have experienced breakdown and therefore are not shown. Leakage current density at 4 MV/cm appears to be a weak function of bilayer thickness, trending higher with increasing bilayer thickness. This may
be caused by the larger crystal grains in thicker ZrO₂ layers, which grow until terminated with an Al₂O₃ layer, increasing the roughness of the films.³⁹

B. TFTs

The possibility of increased $C_{ox}$ with little leakage current penalty suggests that these nanolaminates may offer advantages as gate dielectrics for TFTs. The details of the dielectric-channel interface are known to play an important role in determining the performance and stability of field-effect devices. Nanolaminate films can be terminated with a final layer of either Al₂O₃ or ZrO₂ to form the interface with the AOS channel. Shown in Fig. 6 are $I_D-V_{GS}$ transfer curves and $I_D-V_{GS}$ curves for IGZO and ZTO channel TFTs with 200 nm thick, 10 nm bilayer ZAO laminate dielectrics terminating with either Al₂O₃ (5 nm ZrO₂/5 nm Al₂O₃/AOS channel) or ZrO₂ (5 nm Al₂O₃/5 nm ZrO₂/AOS channel) at the AOS channel interface. Since the overall composition is the same, all of these dielectrics have the same dielectric constant. Relevant parameters of these devices are tabulated in Table I. For IGZO channel TFTs with ZAO laminate dielectrics, $\mu_{inc}$, reduced $\Delta V_{thys}$, and reduced $S$. For the ZTO TFTs with nanolaminate dielectrics, the benefits are not as clear. Devices with Al₂O₃/ZTO interfaces showed reduced $\Delta V_{thys}$ and increased $\mu_{inc}$, but increased $S$ as compared to ZrO₂/ZTO devices.

The data from Figs. 3–5 suggest that some laminate compositions may allow improved performance over single layer dielectrics for TFT applications. Shown in Fig. 7 are $I_D-V_{GS}$ transfer curves and $I_D-V_{GS}$ plots for IGZO channel TFTs with 200 nm thick gate dielectrics of either single layer ZrO₂, single layer Al₂O₃, or 10 nm bilayer ZAO nanolaminates of 25%, 50%, and 75% ZrO₂ content. All devices except the single layer ZrO₂ have an Al₂O₃/IGZO interface. Relevant parameters of these devices are tabulated in Table II. While the single layer ZrO₂ dielectric devices have significantly higher $I_G$ than the rest of the devices, there appears to be no significant difference in $I_G$ between devices with ZAO nanolaminates and single layer Al₂O₃ dielectrics. This result is consistent with the weak dependence of 1 MV/cm leakage current density on ZrO₂ content seen for the 40 nm thick nanolaminate MIS devices [Fig. 5(a)]. Looking first at the performance parameters of TFTs with single layer dielectrics, the ZrO₂ gate dielectric devices showed high $I_{ON}$ and the lowest $S$ (both due in part to having the largest capacitance), medium $\Delta V_{thys}$ and $\mu_{inc}$, but the worst $I_{OFF}$ and thus the worst $I_{ON}/I_{OFF}$ ratio. The single layer Al₂O₃ dielectric devices exhibited lower $I_{OFF}$ than the ZrO₂ devices, but also lower $I_{ON}$ and higher $S$ (due in part to the lower capacitance), lower $\mu_{inc}$, and the largest $\Delta V_{thys}$ of any of the devices. For the TFTs with ZAO laminate dielectrics, the 25% ZrO₂ dielectric devices had low $I_{OFF}$, excellent $I_{ON}/I_{OFF}$, and good $I_{ON}$, but also the worst $S$ and worst $\mu_{inc}$ of any of the devices. The 50% ZrO₂ dielectric devices had the lowest $I_{OFF}$, the best $I_{ON}/I_{OFF}$, and the lowest $\Delta V_{thys}$, but only medium $\mu_{inc}$. Finally, the 75% ZrO₂ content dielectric devices had good $I_{ON}/I_{OFF}$, very low $\Delta V_{thys}$, medium subthreshold slope, and the highest $\mu_{inc}$. For the nanolaminate dielectric devices, $V_{ON}$ decreased, $I_{OFF}$ increased, and $\mu_{inc}$ increased with increasing overall ZrO₂ content. Devices with ZAO nanolaminate dielectrics accounted for the best $I_{OFF}$, highest $I_{ON}$, lowest $\Delta V_{thys}$, and highest $\mu_{inc}$. Overall the 75% ZrO₂ content laminate (7.5 nm ZrO₂/2.5 nm Al₂O₃ bilayer structure) was the
TABLE I. Comparison of device parameters for ZTO and IGZO TFTs with 200 nm thick ZAO dielectrics composed of 10 nm bilayers with 50% overall ZrO2 content (5 nm Al2O3/5 nm ZrO2), terminated with either 5 nm Al2O3 or 5 nm ZrO2 at the AOS interface.

<table>
<thead>
<tr>
<th>Nanolamine/AOS interface</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( \mu_{\text{inc}} ) (cm(^2)/V s)</td>
<td>( S ) (mV/dec)</td>
<td>( \Delta V_{\text{GS}} ) (V)</td>
<td>( I_{\text{ON}}/I_{\text{OFF}} )</td>
</tr>
<tr>
<td>ZrO2/Al2O3/IGZO</td>
<td>14.2</td>
<td>131</td>
<td>0.01</td>
<td>( 10^8 )</td>
</tr>
<tr>
<td>Al2O3/ZrO2/IGZO</td>
<td>10.65</td>
<td>158</td>
<td>0.04</td>
<td>( 10^8 )</td>
</tr>
<tr>
<td>ZrO2/Al2O3/ZTO</td>
<td>15.4</td>
<td>260</td>
<td>0.39</td>
<td>( 9 \times 10^5 )</td>
</tr>
<tr>
<td>Al2O3/ZrO2/ZTO</td>
<td>13.6</td>
<td>226</td>
<td>0.85</td>
<td>( 9 \times 10^5 )</td>
</tr>
</tbody>
</table>

best performing dielectric for the IGZO TFTs in this study, indicating that nanolamine films may be able to combine the benefits of both component dielectrics to produce better performance than either of the single layer films.

Note that because of varying composition and \( \kappa \), each of the 200 nm thick dielectrics have different capacitances and thus, for the same applied \( V_{\text{GS}} \), will induce different charge densities in the AOS channel. In order to account for this difference, we use the concept of capacitive equivalent thickness (CET) in which the thickness of each film is normalized to a capacitive equivalent thickness of Al2O3. The CET of a dielectric is defined as CET = \( d_{\text{phys}} \times (k_{\text{Al2O3}}/k_{\text{dielectric}}) \), where \( d_{\text{phys}} \) is the physical thickness of the dielectric (in all cases 200 nm) and \( k_{\text{dielectric}} \) is the \( \kappa \) of the dielectric for which we are calculating the CET. Using the CET for each dielectric, the effective gate electric field, \( \xi_{\text{GS-EFF}} = \xi_{\text{GS}}/\text{CET} \), required to generate a given charge density in the channel can be determined. Shown in Fig. 7(b) are the data from Fig. 7(a) replotted against \( \xi_{\text{GS-EFF}} \). It is seen that when the differences in capacitance are accounted for, the high capacitance dielectrics such as ZrO2 look a bit worse (increased \( S \) and decreased \( I_{\text{ON}} \)) while the single layer Al2O3 device looks a bit better (reduced \( S \) and increased \( I_{\text{ON}} \)). The conclusions drawn from Fig. 7(a) remain the same, however, in that the 50% and 75% content 10 nm bilayer laminates still exhibit the best overall performance.

An important consideration for commercial applications of AOS TFTs is operational stability.\(^{14–18}\) Shown in Fig. 8 are plots of \( \Delta V_{\text{ON}} \) versus dc bias stress time for IGZO TFTs with 200 nm thick gate dielectrics consisting of either single layer Al2O3, ZrO2, or ZAO laminates with a variety of bilayer structures. All devices have an Al2O3/IGZO interface. All devices were stressed using the same conditions: \( V_{\text{GS}} = +20 \) V (\( \xi_{\text{GS}} = +1 \) MV/cm) with \( V_{\text{DS}} = 1 \) V. Stress was inter-

Table II. Comparison of device parameters for IGZO TFTs with 200 nm thick gate dielectrics of Al2O3, ZrO2, or 10 nm bilayer ZAO laminates of 25%, 50%, and 75% overall ZrO2 content.

<table>
<thead>
<tr>
<th>Dielectric or bilayer structure (nm)</th>
<th>( \mu_{\text{inc}} ) (cm(^2)/V s)</th>
<th>( S ) (mV/dec)</th>
<th>( \Delta V_{\text{GS}} ) (V)</th>
<th>( I_{\text{ON}}/I_{\text{OFF}} )</th>
<th>( \kappa )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al2O3</td>
<td>12.0</td>
<td>151</td>
<td>0.45</td>
<td>( 6 \times 10^6 )</td>
<td>8.0</td>
</tr>
<tr>
<td>2.5 ZrO2/7.5 Al2O3</td>
<td>7.2</td>
<td>247</td>
<td>0.24</td>
<td>( 2 \times 10^5 )</td>
<td>9.3</td>
</tr>
<tr>
<td>5.0 ZrO2/5.0 Al2O3</td>
<td>14.2</td>
<td>131</td>
<td>0.01</td>
<td>( 10^8 )</td>
<td>12.4</td>
</tr>
<tr>
<td>7.5 ZrO2/2.5 Al2O3</td>
<td>22.3</td>
<td>152</td>
<td>0.02</td>
<td>( 10^7 )</td>
<td>14.4</td>
</tr>
<tr>
<td>ZrO2</td>
<td>16.1</td>
<td>100</td>
<td>0.19</td>
<td>( 2 \times 10^6 )</td>
<td>25.3</td>
</tr>
</tbody>
</table>
ruptured at regular time intervals to measure \( I_D-V_{GS} \) transfer curves. Because \( I_D-V_{GS} \) transfer curves took about 10^3 s to collect, Fig. 8 begins at an accumulated bias stress time of 10^3 s. Devices with a single layer Al\(_2\)O\(_3\) dielectric showed \( \Delta V_{ON} \) of roughly 0.8 V at 2 × 10^4 s. As seen in Fig. 8(a), \( \Delta V_{ON} \) was the worst in devices with single layer ZrO\(_2\). Shown in the zoomed y-axis scale plot in Fig. 8(b), it is seen that the bias stress performance of the 5 and 20 nm thick bilayer laminates was comparable to single layer Al\(_2\)O\(_3\). All of the 10 nm bilayer ZAO nanolaminate films, regardless of ZrO\(_2\) content, performed as well or better than single layer Al\(_2\)O\(_3\), exhibiting lower \( \Delta V_{ON} \) at long stress times. Once again, the 75% ZrO\(_2\) 10 nm bilayer ZAO performed the best with only a 0.2 V shift after 10^3 s of stress.

As seen in Fig. 8, TFTs with single layer ZrO\(_2\) dielectrics suffer more from \( \Delta V_{ON} \) than TFTs with single layer Al\(_2\)O\(_3\) dielectrics. Much of this is likely due to the different chemical natures of the IGZO/AOS and Al\(_2\)O\(_3\)/AOS interfaces. In addition, the increased susceptibility of ZrO\(_2\) to positive gate bias stress may be due in part to the smaller conduction band offset of ZrO\(_2\) to IGZO, which allows more injection into the ZrO\(_2\) layer (see Figs. 4 and 5), which in turn leads to increased electron trapping and increased \( \Delta V_{ON} \) as compared to single layer Al\(_2\)O\(_3\). The presence of Al\(_2\)O\(_3\) at the interface, which has a larger conduction band offset to IGZO, may help in preventing electrons from being injected into the ZrO\(_2\) layer and thus lead to a reduction in \( \Delta V_{ON} \) as a function of stress time. What is puzzling is the observation in Fig. 7 that TFTs with laminate Al\(_2\)O\(_3\) interfaces can perform better than single layer Al\(_2\)O\(_3\) interfaces. That is, the use of a thin Al\(_2\)O\(_3\) layer at the interface can in some cases perform better than a thick single layer Al\(_2\)O\(_3\) dielectric. Combined with the stability results from Fig. 8, this suggests that there may be an optimal thickness for the near-interfacial bilayer structure to attain the best overall performance and stability. Although there is no clear overall dependence of \( \Delta V_{ON} \) on the Al\(_2\)O\(_3\) interfacial layer thickness, \( \Delta V_{ON} \) for the 10 nm bilayer nanolaminates appears to become larger as the thickness of the Al\(_2\)O\(_3\) layer at the AOS interface increases. During sputter deposition of the AOS channel, the surface of the dielectric is exposed to energetic particle bombardment from the plasma, which could create traps in the dielectric. Al\(_2\)O\(_3\) may be more susceptible to this damage than ZrO\(_2\). As a result, the use of an Al\(_2\)O\(_3\) interfacial layer that is thicker than necessary to impede charge injection (order of a few nanometers) may lead to a larger \( \Delta V_{ON} \) than a thinner Al\(_2\)O\(_3\) interfacial layer, due the creation of additional traps near the dielectric/channel interface. It therefore may be possible to optimize the bilayer structure with the interfacial Al\(_2\)O\(_3\) layer effectively arranged so as to suppress the electron injection into the ZrO\(_2\) layer while at the same time avoiding excessive plasma-induced electron traps. It is likely that the optimum arrangement of the interfacial bilayer will be a function of the AOS material (interface chemistry) as well as the processing details of the AOS deposition. 19

IV. SUMMARY AND CONCLUSIONS

ZrO\(_2\)–Al\(_2\)O\(_3\) nanolaminate dielectrics consisting of a series of ZrO\(_2\)–Al\(_2\)O\(_3\) bilayers were deposited via ALD with various bilayer thicknesses. The percentage of ZrO\(_2\) in the laminates was varied by adjusting the ratio of ZrO\(_2\) layer thickness to Al\(_2\)O\(_3\) layer thickness within each ZrO\(_2\)–Al\(_2\)O\(_3\) bilayer. The relative dielectric constants of ZAO laminate films in MIS devices were found to be between those of single layer ZrO\(_2\) and single layer Al\(_2\)O\(_3\) films, increasing with increasing ZrO\(_2\) content as would be expected from a simple series of Al\(_2\)O\(_3\) and ZrO\(_2\) capacitors. Leakage current density was found to be a function of ZrO\(_2\) content as well as the applied electric field. At low electric fields, in the range suitable for TFT operation (1–2 MV/cm), leakage current density increased only weakly with increasing ZrO\(_2\) content. At higher fields (∼4 MV/cm), nanolaminate films with 25% and 50% ZrO\(_2\) had lower leakage currents than single layer Al\(_2\)O\(_3\) films. Neither the relative dielectric constant nor leakage was found to be a strong function of bilayer thickness.

ZAO nanolaminates were used as gate dielectrics for IGZO and ZTO TFTs. It was found that terminating ZAO laminate dielectrics with a layer of Al\(_2\)O\(_3\), so as to provide an Al\(_2\)O\(_3\)/AOS channel interface rather than a ZrO\(_2\)/AOS channel interface, resulted in improved device characteristics for IGZO channel devices. In addition, it was found that ZAO nanolaminate dielectrics could be engineered to outperform the constituent single layer dielectrics for AOS TFT applications, providing improved TFT performance and stability.

For IGZO TFTs, both 50% and 75% ZrO2 content 10 nm bilayer films showed better performance than single layer Al2O3 films with \( \mu_{\text{inc}} \) as high as 22.3 cm2/V s, low \( \Delta V_{\text{TH}} \), and minimal \( \Delta V_{\text{ON}} \) during extended positive dc bias stressing. For 10 nm bilayer array, \( \Delta V_{\text{ON}} \) appears to decrease as the thickness of the Al2O3 interfacial layer decreases. However, the lack of a universal dependence of device performance on the thickness of the Al2O3 interfacial layer in all laminate films suggests that there may be an optimum thickness that depends not only on the AOS material but also on the trade-off between the effectiveness of Al2O3 as a barrier to electron injection and the susceptibility of Al2O3 to sputter damage, the thickness of the adjacent ZrO2 layer, and/or the deposition details of the AOS material.

ACKNOWLEDGMENTS

This work was supported in part by grants from the National Science Foundation (through Grant No. DMR-0805372 and an REU supplement) and matching funds from the Oregon Nanoscience and Microtechnologies Institute (ONAMI). The authors thank Professor Greg Herman (OSU ChE) for the ZTO used in this study.