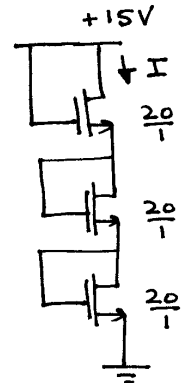


Homework #2 (Due Oct. 16)

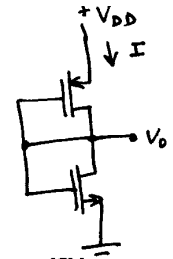
Note that the bulk is tied to the lowest voltage for NMOS transistors and the highest voltage for PMOS transistors.

1. n-ch: $V_{TO} = 1.0 \text{ V}$, $k' = 25 \mu\text{A}/\text{V}^2$ p-ch: $V_{TO} = -1.0 \text{ V}$, $k' = 10 \mu\text{A}/\text{V}^2$.

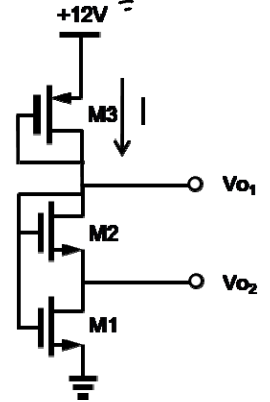
- (a) Assume $\gamma = 0 \text{ V}^{1/2}$. Determine the current I.
- (b) Take $\gamma = 0.5 \text{ V}^{1/2}$, $\phi = 0.6 \text{ V}$. Determine the current I.
- (c) Replace the NMOS transistors with PMOS transistors with the gate and drain tied together (similar to the NMOS circuit). Draw the circuit schematic.
- (d) For the circuit in (c) assume $\gamma = 0 \text{ V}^{1/2}$ and $W/L = 40/1$. Determine I.
- (e) For the circuit in (c) assume $\gamma = 0.5 \text{ V}^{1/2}$, $\phi = 0.6 \text{ V}$, and $W/L = 40/1$. Determine I.
- (f) Verify the results for (a), (b), (d), and (e) using SPICE.



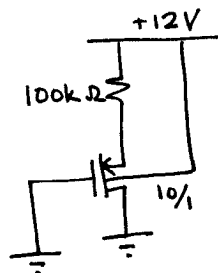
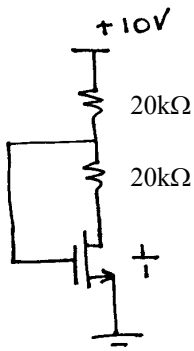
2. a) Find the current I and voltage V_o for the circuit shown with $W/L = 20/1$ for both transistors. n-ch: $V_{TO} = 1.0 \text{ V}$, $k' = 25 \mu\text{A}/\text{V}^2$, p-ch: $V_{TO} = -1.0 \text{ V}$, $k' = 10 \mu\text{A}/\text{V}^2$. Verify your results with SPICE.



b) Find the current I and voltages V_{o1} and V_{o2} for the circuit shown with $(W/L)_1 = 2 \mu\text{m}/1 \mu\text{m}$, $(W/L)_2 = 8 \mu\text{m}/1 \mu\text{m}$ and $(W/L)_3 = 18 \mu\text{m}/1 \mu\text{m}$. n-ch: $V_{TO} = 1.0 \text{ V}$, $k' = 100 \mu\text{A}/\text{V}^2$, $V_{SB} = 0\text{V}$, p-ch: $V_{TO} = -1.0 \text{ V}$, $k' = 50 \mu\text{A}/\text{V}^2$, $V_{SB} = 0\text{V}$. Verify your results with SPICE using the Level-1 MOSFET model.



3. Calculate I_D , V_{GS} and V_{DS} for the transistors shown in the circuit. Use the transistor parameters from Problem 2 (a). Verify your results with SPICE.



4. a) Use SPICE to generate the I_D - V_{DS} characteristics for an n-channel MOSFET. Take $V_{GS}=1, 1.5,$ and $2V$ and $V_{DS}=0$ to $2V$ in steps of $0.2V$. Compare the results using the BSIM3 model parameters ($0.18\mu m$ CMOS process) on the class web page for three device geometries $\frac{W}{L} = \frac{100\mu}{100\mu}$, $\frac{W}{L} = \frac{1\mu}{1\mu}$, and $\frac{W}{L} = \frac{0.2\mu}{0.2\mu}$. Comment on your results.

b) Let $\frac{W}{L} = \frac{1\mu}{1\mu}$, $V_{GS} = 1.5V$, $V_{TO} = .417$, and assume the transistor is biased in saturation, find λ and k_n' using results from (a).

5. An n-channel MOSFET has $V_{TO}=0.7V$, $\phi = 0.7V$, $K' = 100 \mu A/V^2$, $\gamma = 0.6V^{1/2}$, $\frac{1}{\lambda L} = \frac{20V}{\mu m}$. This device is biased in saturation with $I_D=100 \mu A$ and $V_{SB}=1V$. Find the $\frac{W}{L}$ to provide a g_m of $200 \mu A/V$ and a g_{ds} of $2 \mu A/V$. What is the value of g_{mbs} ? Verify results with the SPICE Level 1 model.

6. a) Derive the expressions for the small-signal resistance as shown in the following circuits. Do not ignore the transistor r_o .

- b) Calculate the value of R for each of the cases assuming $k'=100 \mu A/V^2$, $V_{TO}=0.7V$, $\lambda=0.05$, $\phi = 0.7V$, $\gamma = 0.6V^{1/2}$, $\frac{W}{L} = \frac{10\mu}{0.5\mu}$ and all transistors are biased in saturation with a current of $100 \mu A$.
- c) Verify your results using .TF and .AC analyses in SPICE and the MOSFET level-1 model.

