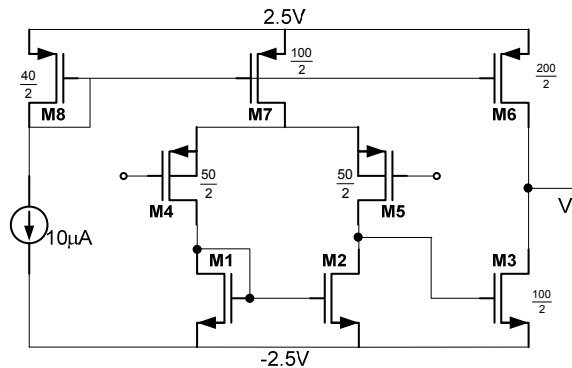


Homework #5 (Due Nov. 10)

- For the 2-stage opamp shown below determine the sizes of M1 and M2 to avoid a systematic offset voltage. Calculate the dc operating point, the input common mode range, the output voltage swing, the small-signal voltage gain, and the output resistance. $V_{TON}=0.7V$, $V_{TOP}=-0.9V$ $k_N' = 100 \mu A/V^2$, $k_P' = 50 \mu A/V^2$, and $\frac{1}{\lambda L} = \frac{20V}{\mu m}$. Compare your results with SPICE Level-1 MOSFET model.



- Design a two-stage opamp given the following constraints: $W(\max) = 50\mu m$, $L(\min) = 2\mu m$, $V_{DD} = 2.5V$, $V_{SS} = -2.5V$, $P_{diss} = 1mW$. Choose the bias current for the first stage (I_{SS}) and the second stage to be $80\mu A$ and design for the largest possible G_m for the first stage. Determine the small-signal gain, output resistance, the input common mode range, and the output voltage swing. $V_{TON}=0.7V$, $V_{TOP}=-0.9V$ $k_N' = 100 \mu A/V^2$, $k_P' = 50 \mu A/V^2$, and $\frac{1}{\lambda L} = \frac{20V}{\mu m}$. Verify your results using SPICE with the Level-1 MOSFET model. Also simulate the systematic input offset voltage with SPICE.

- The layout and biasing of a MOSFET are shown below.
 - Sketch the complete small-signal model for this transistor at the given operating point and calculate the values of all small-signal parameters. $V_{TO}=0.7V$, $k' = 100 \mu A/V^2$, $\lambda=0.05/V$, $\gamma=0.5V^{1/2}$, $\phi=0.7V$, $T_{ox}=100 \text{ \AA}$, $C_{JO}=0.5fF/\mu m^2$, $C_{JSWO}=0.3fF/\mu m$, $C_{GSO}=C_{GD0}=0.4fF/\mu m$, $M_J=0.6$, $M_{JSW}=0.1$, $P_B=P_{BSW} = 1.0V$.
 - Calculate the unity-gain frequency.
 - Verify your results of (a) and (b) using SPICE with the Level-1 MOSFET model.

