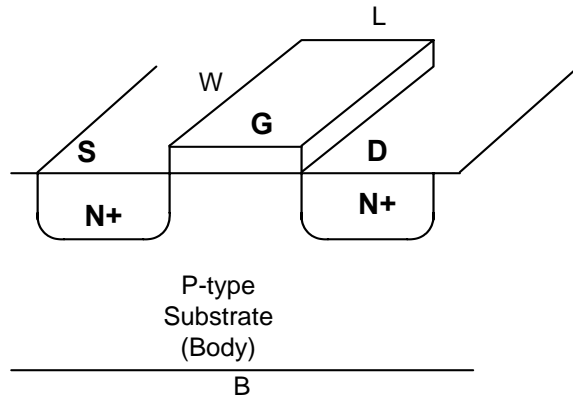


# MOSFET

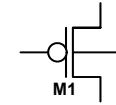
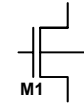
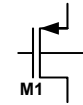
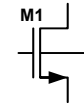
## Enhancement mode N-channel MOSFET (NMOSFET)



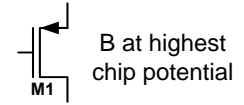
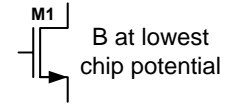
# MOSFET Symbols

N-channel FETs

P-channel FETs



If bulk is connected to proper power supply:

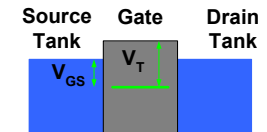
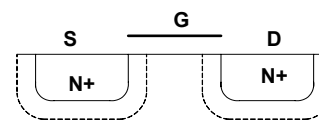


## PMOSFET in a P-type Substrate?

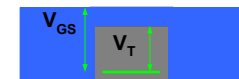
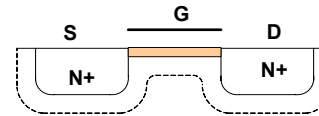
## MOSFET Operation Simplified (Fluid Dynamics Analog)

$V_T$  = turn-on Voltage (threshold voltage)

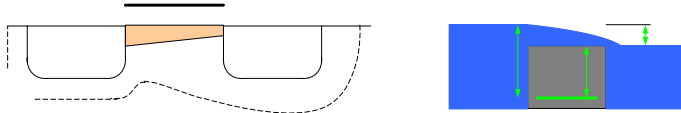
1) Cut off:  $V_{GS} < V_T$ ,  $V_{DS} = 0$



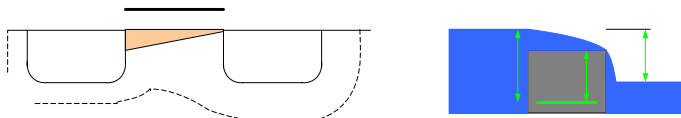
2) Strong Inversion:  $V_{GS} > V_T$ ,  $V_{DS} = 0$



3) Non-saturation:  $V_{GS} > V_T$ ,  $0 < V_{DS} < V_{GS} - V_T$



4) Saturation:  $V_{GS} > V_T$ ,  $V_{DS} > V_{GS} - V_T$



Flow becomes independent of VDS

## Simple MOSFET Model (Level = 1)

$$I_{DS} = 0 \quad V_{GS} < V_T \quad \text{Cutoff}$$

$$I_{DS} = K' \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] (1 + \lambda V_{DS}) \quad V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T$$

Linear, triode, non-saturation

$$I_{DS} = \frac{K'}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T$$

Saturation

$$V_T = V_{T0} + \gamma (\sqrt{|\Phi + V_{SB}|} - \sqrt{|\Phi|})$$

$K', V_{T0}, \gamma, \lambda, \phi$  are process parameters

$W, L$  are device geometry parameters

G

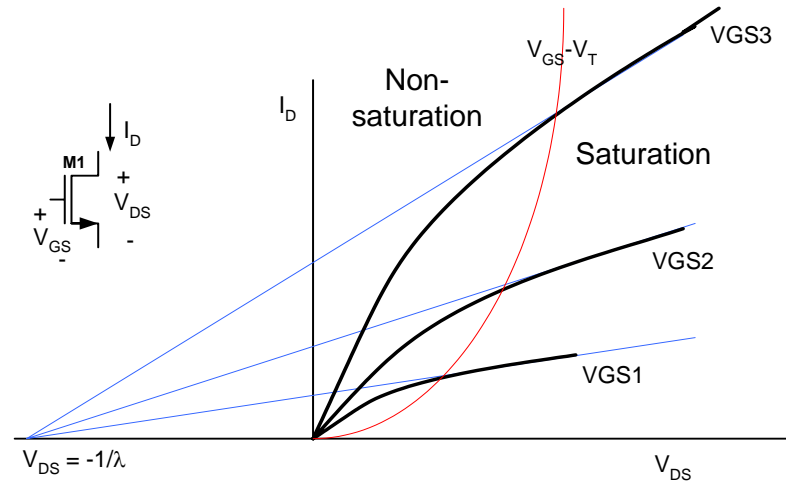
S

## Model Parameter Names in SPICE

Parameter	SPICE Param	Units
$K'$	KP	$A/V^2$
$V_{T0}$	VTO	V
$\gamma$	GAMMA	$V^{1/2}$
$\lambda$	LAMBDA	$V^{-1}$
$\phi$	PHI	V

D

## N-channel device I-V Characteristics

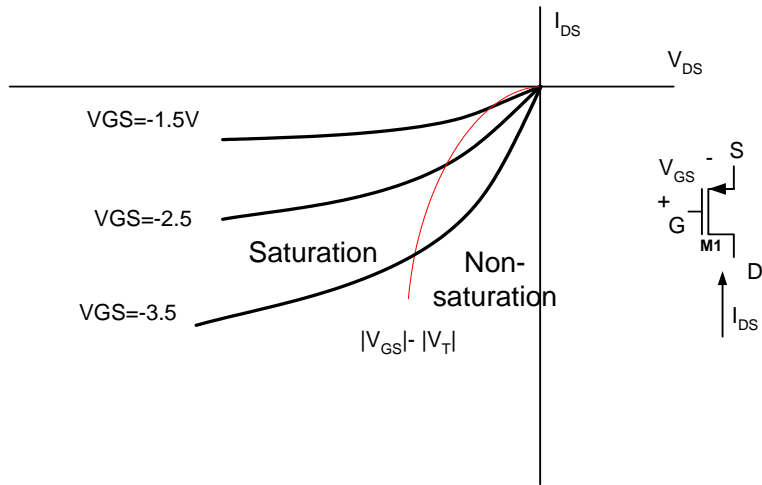


G

S

D

## P-channel device I-V Characteristics



## Parameter Extraction

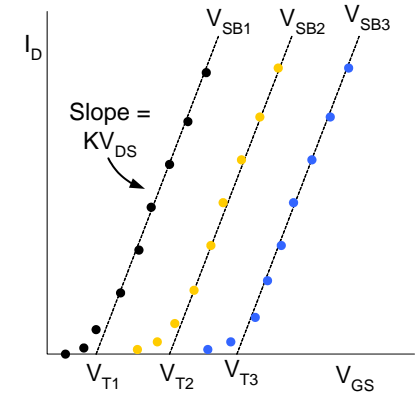
- Determination of  $K$  and  $V_T$  ( $K = K'W/L$ )

– At very small  $V_{DS}$

$$I_{DS} \cong K(V_{GS} - V_T)V_{DS}$$

– Slope =  $K V_{DS}$ , extrapolated intercept is  $V_T$

– If slope is not the same for all curves, use an average value

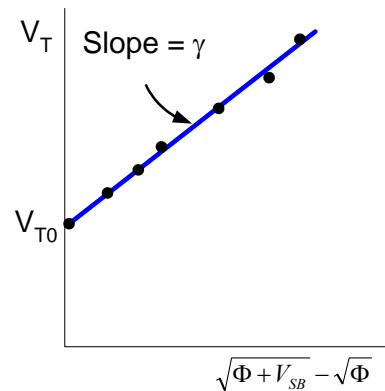


## Parameter Extraction

- Determination of  $\gamma$  and  $V_{T0}$

$$V_T = V_{T0} + \gamma(\sqrt{\Phi + V_{SB}} - \sqrt{\Phi})$$

- Plot  $V_T$  vs  $\sqrt{\Phi + V_{SB}} - \sqrt{\Phi}$
- Assume  $\Phi = 0.6 V$
- Slope =  $\gamma$ , intercept =  $V_{T0}$



## Parameter Extraction

- Calculation of  $\lambda$

$$I_{DS} = \frac{1}{2}K' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

– For a fixed  $V_{GS}$  and  $V_{SB}$

$$I_{DS} = I_0 (1 + \lambda V_{DS}) \quad \text{where} \quad I_0 = \frac{K' W}{2 L} (V_{GS} - V_T)^2$$

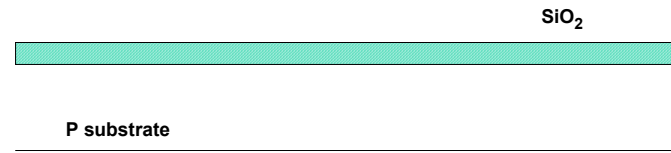
$$\frac{I_{D1}}{I_{D2}} = \frac{(1 + \lambda V_{DS1})}{(1 + \lambda V_{DS2})}$$

– Solve for  $\lambda$

# CMOS Integrated Circuit Technology

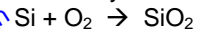
## Starting Material

Start with a single-crystal Silicon wafer – up to 12" diameter (300 mm)



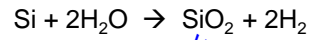
Grow oxide layer

*Dry Oxidation*



Temperature raised between 850°C to 1100°C

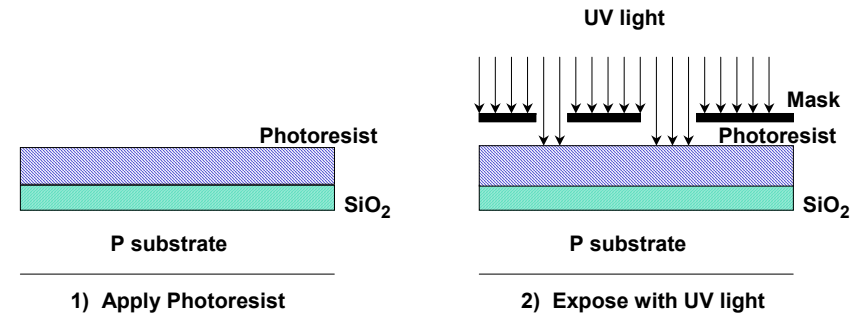
Consumes Si at rate of 0.44 times SiO<sub>2</sub> thickness



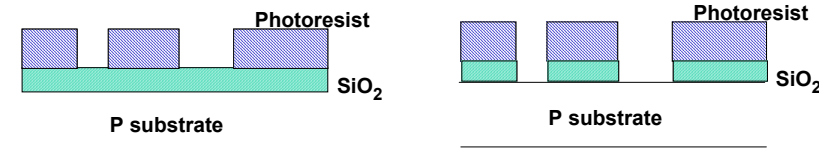
*Wet Oxidation*

A unique property of Si is that the SiO<sub>2</sub> oxide layer thickness can be controlled very uniformly

# Photolithography



## Creating N and P-Type Regions

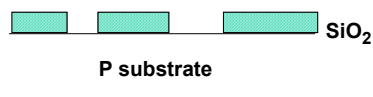


3) Develop Photoresist

Positive resist : exposed resist is removed  
 Negative resist : non-exposed resist is removed

4) Etch SiO<sub>2</sub>

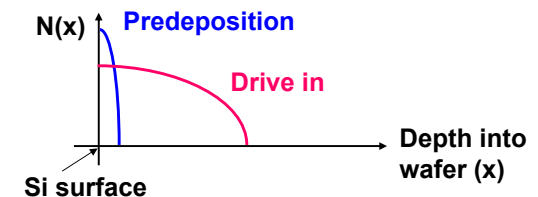
SiO<sub>2</sub> can then be removed with hydrofluoric acid



5) Strip resist leaving patterned SiO<sub>2</sub>

## Diffusion

- Deposit a layer of material on silicon surface (**Predeposition**)
- Boron for P-type; Arsenic or Phosphorus for N-type
- Raise temperature to ~ 1000° C to allow impurities to diffuse into substrate and replace Si atoms (**Drive in**)
- Highest impurity concentration at surface



## Ion Implantation

- Atoms are inserted at high energy into substrate
- Must be annealed at  $\sim 800^\circ\text{C}$  for approx 10 min to activate and reduce damage to substrate
- Most common method because
  - Small amounts of impurities can be reproducibly deposited
  - Amount of impurity deposited can be precisely controlled
  - Very uniform across wafer
  - Peak of impurity profile can be below surface

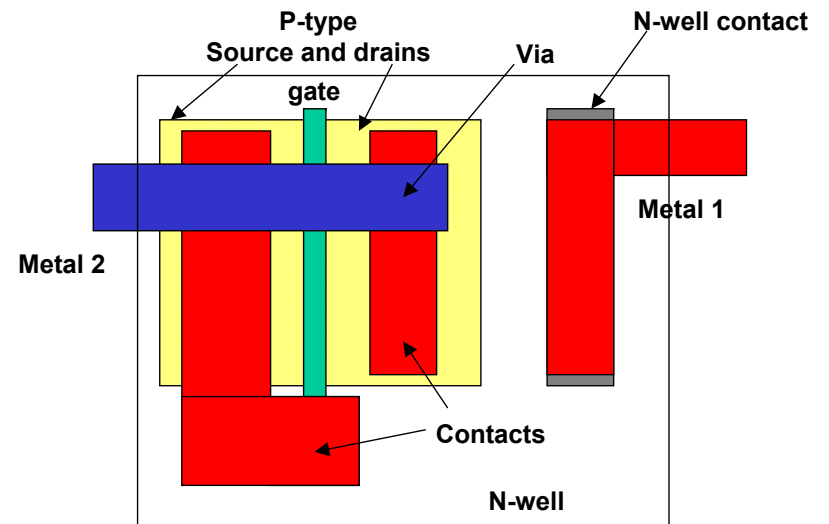
## Deposition

- Various materials need to be deposited on the wafers to fabricate circuits
- Chemical vapor deposition (CVD) is a common method to apply polysilicon, silicon nitride ( $\text{Si}_3\text{N}_4$ ) and other dielectrics
- Metals are typically evaporated onto the wafers (sputtering)

## Etching

- Used to remove materials with high precision
- Wet etching
- Plasma etching
- Reactive ion etching (RIE)

## Layout Example of PMOS Transistor



# Process Flow

