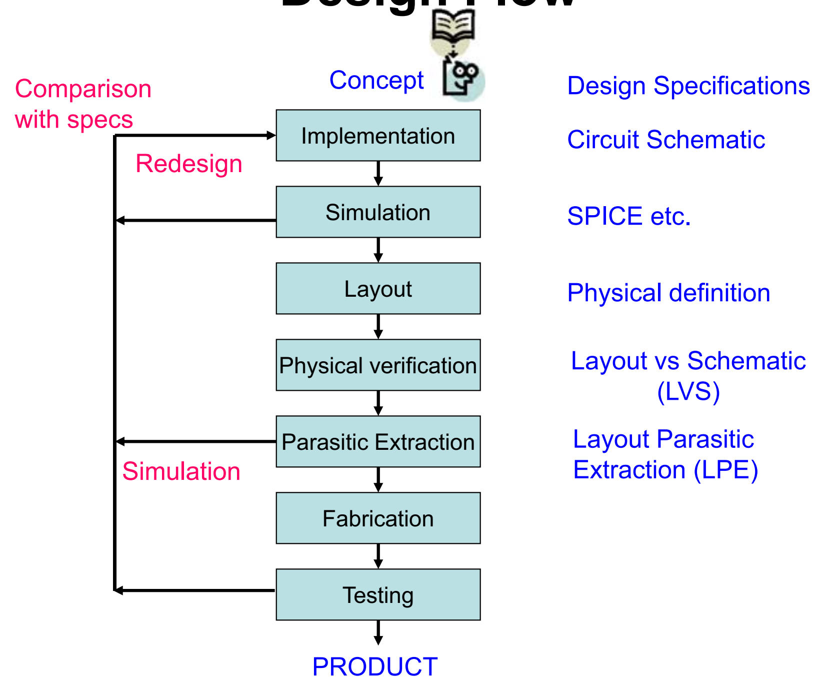
ECE 521

Fall 2016

Design Flow



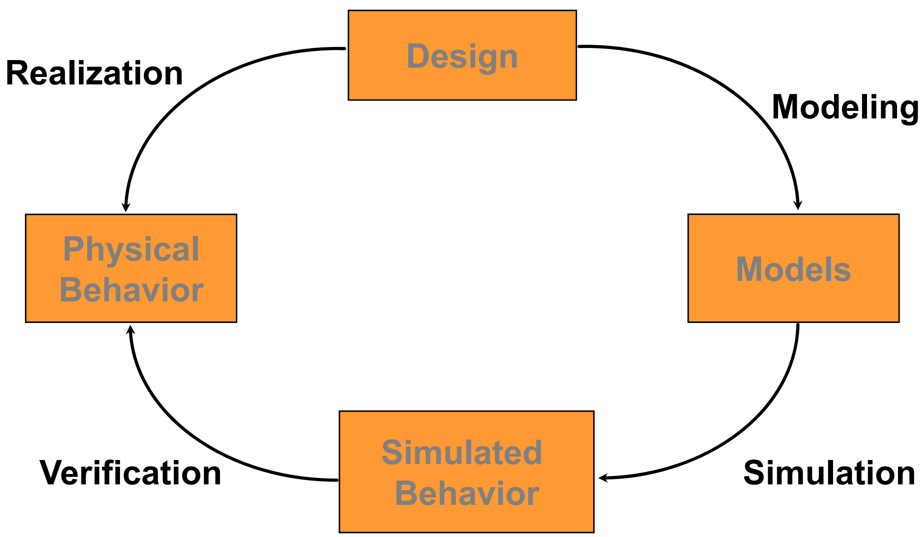
Design Verification

- **Prototyping or bread boarding**
  - Implement and see if design works
  - Tweak component values for proper operation
- **Simulation**
  - Start from mathematical descriptions of components (Models)
  - Formulate equations based on physical laws (KCL, KVL)
  - Specify input test patterns and find output
  - Equations solved by use of a computer

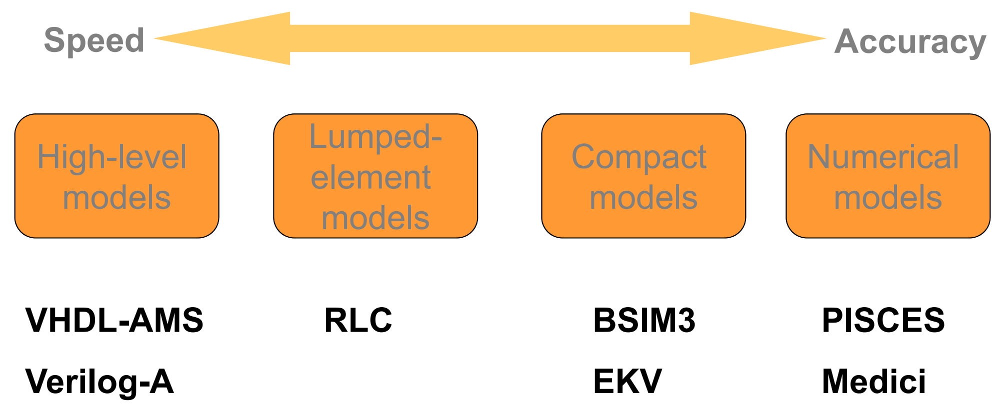
Why Solve Equations on a Computer?

- **Problem has no closed-form solution**
  - Have to use numerical techniques
- **Problems typically very large so cannot be solved by hand**
- **In IC world simulation is a necessity**
  - Cannot bread board ICs
  - Fabrication for design iterations is an expensive alternative
  - First step to ensuring first-pass silicon
  - Can do early design even before complete process exists

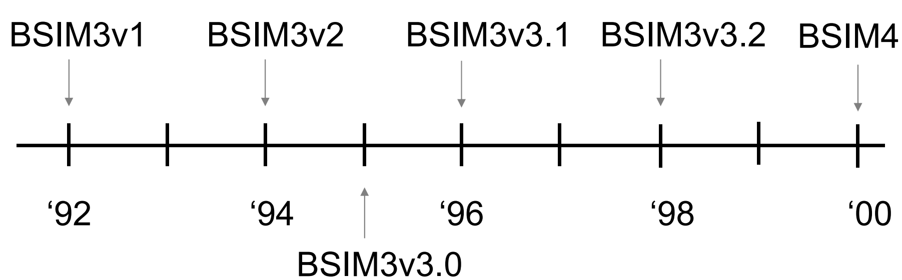
Role of Modeling in Design



The Modeling Hierarchy

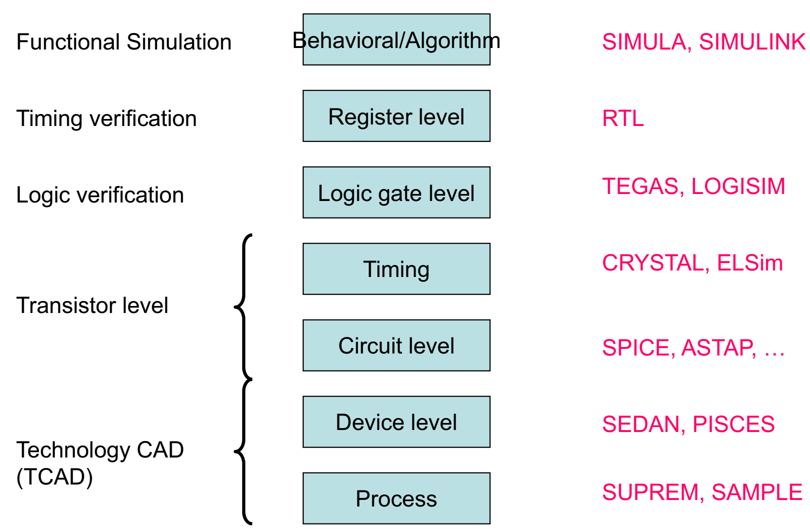


A Case Study - BSIM3 MOSFET Model

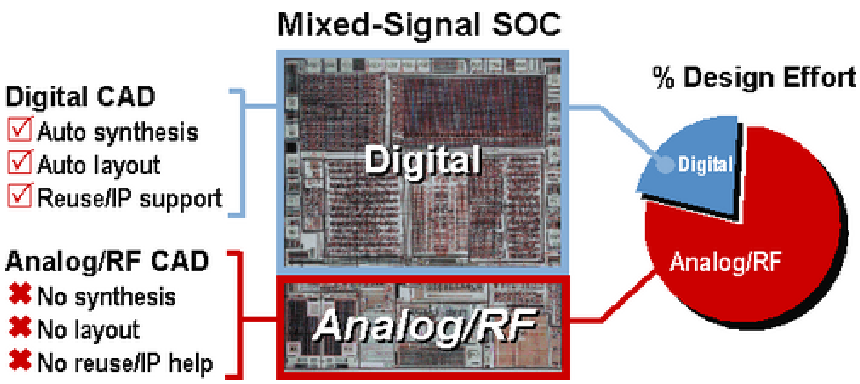


- **Compact model development, implementation and validation takes several years**

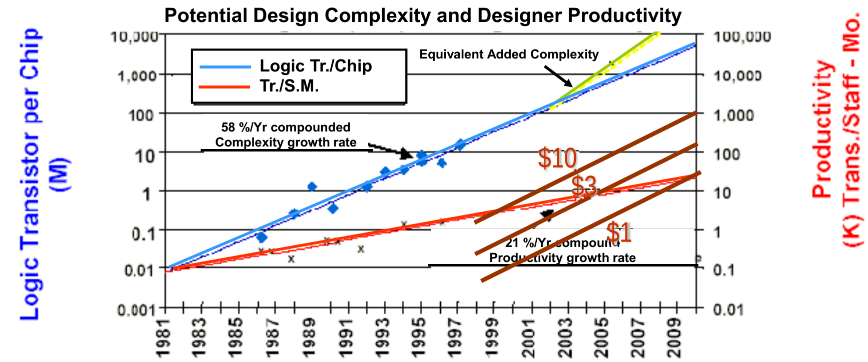
Simulation Levels



Digital vs Analog CAD



"The Design Productivity Gap"



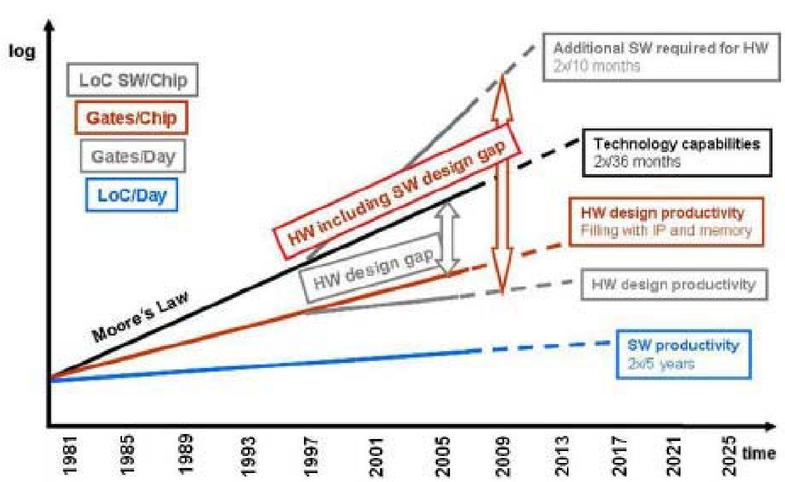
Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400 MHz	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $ 150 k / Staff Yr. (In 1997 Dollars)

Source: SEMATECH

Hardware and Software Design Gaps versus Time (2011 ITRS Roadmap)

http://www.semiconductors.org/clientuploads/Research_Technology/ITRS/2011/2011Design.pdf



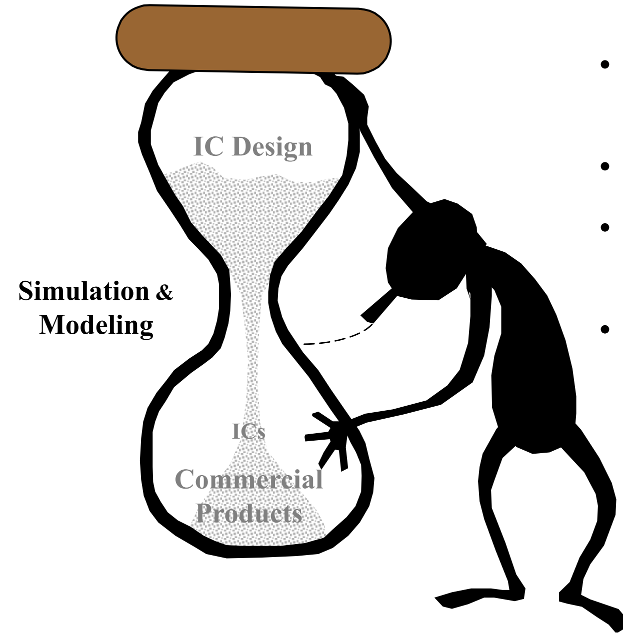
Why Analog Circuit Simulation?

- Difficult and challenging
- Analog behavior specified in terms of complex functions
  - Time-domain waveforms (settling time, slew)
  - Frequency response (mag, phase, spectra)
  - Distortion (HD, IMD)
  - Noise
  - Device matching
- Require very accurate component models

Challenges in Analog Circuit Simulation

- **Accurate models**
  - Low frequency, high frequency
  - Noise
  - Distortion
  - Statistical variations
- **Faster simulation techniques**
  - Power supplies
  - $\Delta\Sigma$ modulators
  - RF oscillators, mixers, phase noise, mixing
  - Phase-locked loops
  - Accurate distortion calculation

Simulation & Modeling are Design Bottlenecks



- **Reduced simulation times**
- **Accurate models**
- **Modeling of high frequency effects**
- **Simulation of RF ICs**

ITRS Modeling and Simulation Challenges

http://www.semiconductors.org/clientuploads/Research_Technology/ITRS/2013/2013 Modeling_Summary.pdf

Nanoscale device modeling for novel devices	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra Coupling traditional electronic models for memories with new state variables (e.g. spin, polarization, local material composition, phase state, mass density/mechanical stress, bonding arrangement, …) Models for gate stacks with ultra-thin/high-k dielectrics for relevant channel materials (e.g. Ge, SiGe, InGaAs, ...) w.r.t. electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure , dopant and material variations in order to assess the impact of variations on statistics of device performance, including non-Gaussian distributions
Hierarchical simulation	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modelling and simulation levels as well as different simulation domains '- including manufacturability
Multiphysics simulation	Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers Combined EM and drift diffusion simulation to include inductance effects in substrate caused by interconnects and bond wires

What is This Course About?

Input

```
R1 1 0 1K
C1 1 0 1pF
M1 1 2 0 0 MOD1 W=1U L=1U
…
```

Input processor

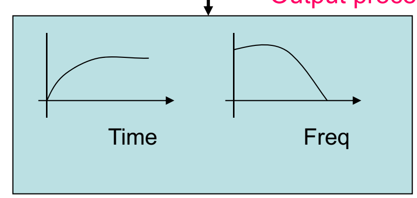
Simulation Engine and Models

Numerical Solution

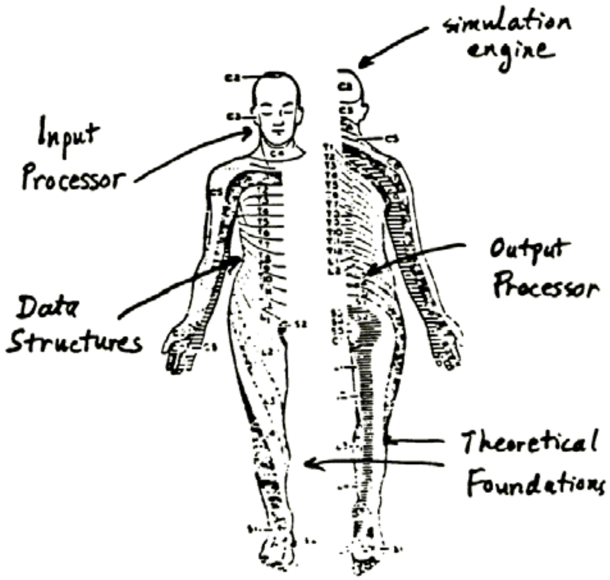
Output processor

Theoretical foundation, modeling, software

Output



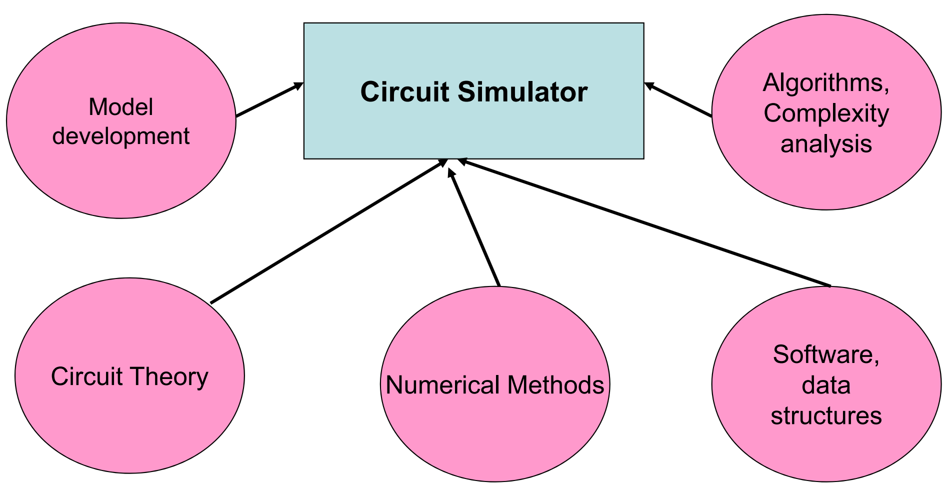
The Anatomy of a Circuit Simulator (From Dr. Res Saleh)



Who Can Benefit from This Course

- **Circuit designers**
  - Be an informed consumer of simulation tools
  - Simulator knowledge helps identify problems
- **Model developers**
  - Models implemented in simulators
  - Tight coupling between models & algorithms
- **Computer-aided design (CAD) tool developer**
  - Simulators are the most important IC-CAD tool

Basic Skills Required



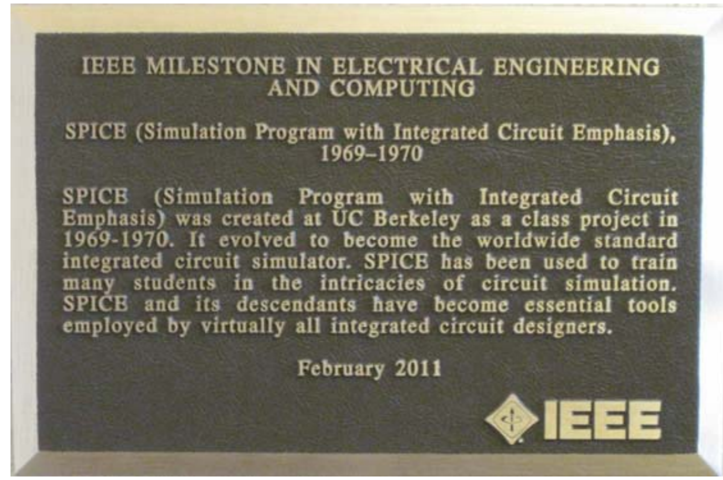
Brief Overview of SPICE

1969-70	**CANCER project (Computer Analysis of Nonlinear Circuits Excluding Radiation)** **Ron Rohrer's class project**
1970-72	**CANCER program (Rohrer and Nagel)**
1972	**SPICE1 released as public-domain tool (Nagel and Pederson)**
1975	**SPICE 2A, 2C**
1976	**SPICE 2D – New MOS models**
1979	**SPICE 2E – Device levels**
1980	**SPICE 2F – Portable SPICE, MOSFET charge models**
1982	**SPICE 2G**
1985	**SPICE 3C (Quarles, Newton, and Pederson)**
1993	**SPICE 3F**
1999	**NGSPICE (SPICE 3F + enhancements)**
2014	**NGSPICE (Release 26)** CUSPICE - NGSPICE on CUDA platforms

SPICE – The Present

- **The “alphabet” SPICE(s)**
  - HSPICE, GSPICE, QSPICE, PSPICE, …
- **Internal SPICE**
  - TI-SPICE (TINA), TekSPICE, ADICE, LTSPICE, …
- **Others**
  - Qucs, Gnucap, iFreeda, DoCircuits, EveryCircuit, CircuitLab, Circuit-cloud, …
- **Open source parallel SPICE**
  - XYCE (https://xyce.sandia.gov/)
- **Commercial**
  - Spectre, Eldo, AFS, ADS, SmartSpice, …
- **Recognized as an IEEE milestone (significant technical achievement) in 2011**

IEEE Milestone Plaque (From Dr. Larry Nagel)



Reasons for Success

- **Proper choice of algorithms and software system**
- **Friendly (intuitive) input description language**
- **Public domain software**
- **Developed by circuit designers**
- **Useful tool for teaching and understanding circuits**

SPICE – The Future

- **New functionality**
  - Algorithms
  - Device models
  - Chip, package, electrothermal simulation
  - Coupled simulation domains
  - Analog behavioral modeling languages
- **Robust simulation of extremely large circuits – Full-chip circuit simulation**
- **Faster simulation**
  - Fast SPICE(s)
- **Hardware accelerated simulation**
  - GPU
  - Multi-core

Course Outline (DC Analysis)

- **Solution of linear resistive circuits**
  - R, independent (dc) current/voltage sources
  - Linear dependent (controlled) sources
  - Equation formulation methods
  - Equation solution methods
  - Software implementation
- **Solution of nonlinear resistive circuits**
  - Diodes, Transistors, all linear components
  - Equation formulation methods
  - Equation solution methods
  - Software implementation

Course Outline (Transient Analysis)

- **Solution of linear dynamic circuits**
  - R, independent (dc, time-varying) current/voltage sources
  - Linear dependent (controlled) sources
  - C, L
  - Diodes, Transistors
  - Equation formulation methods
  - Equation solution methods
  - Software implementation
- **Solution of nonlinear dynamic circuits**
  - Nonlinear capacitors

Course Outline (Other Analyses)

- **Small-signal AC analysis**
- **Pole-zero analysis**
- **Sensitivity analysis**
- **Fourier analysis**
- **Small-signal noise analysis**
- **Analysis methods for RF circuits**

Other Information and Assignments

- **Class webpage:**
  http://web.engr.oregonstate.edu/~karti/ece521.html
- **Lecture notes posted on class webpage**
- **Anonymous feedback available on webpage**
- **Read background papers posted on webpage**
- **Familiarize/review C programming language**
- **HW#1 posted (Due Oct 12)**
  - More on it next week
  - C-code templates provided