SPICE - The Third Decade

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ABSTRACT

This paper is a review of the evolution of SPICE from the initial research project at the University of California at Berkeley in the late 1960s, through the 1970s and 1980s, and into the 1990s.

A general description of the SPICE techniques, analysis modes, and intended areas of application is provided first. The relation between solution algorithms, semiconductor device models, and circuits to be characterized is explored in order to clarify the merits and limits of this program. The current trends in electrical circuit simulation and the role of SPICE in its third decade are presented in the last part of this review.

1. Introduction

SPICE in its different versions has been the main Computer-Aided Analysis program used in analog design for over twenty years. SPICE is the result of the work of a number of talented graduate students in the Electrical Engineering and Computer Science Department at the University of California at Berkeley, under the mandate that they produce the best available computer program for the simulation of practical integrated circuits, ICs, under the guidance of D. Pederson and R. Rohrer. This program has been written by engineering students for engineers which explains the simpler and computationally more efficient approach chosen for the network equations and the built-in semiconductor device models.

The program known as SPICE today was first released under the name CANCER [1] in 1970 and acquired the name SPICE1 [2] in 1972. SPICE2 [3], [4], which in its various versions enjoys the largest use worldwide today, was released in 1975. The universal acceptance is due not only to its robustness and ease of use but also to its free distribution by UC Berkeley.

It is important to note that the early years of the SPICE development have been dedicated to the investigation of the most accurate and efficient numerical methods for circuit representation, input language, nonlinear equation solution, integration algorithms, sparse-matrix solutions, and nonlinear semiconductor device modeling. The main goal of the SPICE project has been to provide an efficient computer tool for the design of the emerging ICs in the late 1960s and early 1970s. The choice of the Nodal Admittance representation is based on the relative ease of setting up the circuit matrix, and the quick access to the DC operating point. In the design of linear ICs such as the μA741 checking the bias point and performing a small-signal analysis were essential. A number of related programs originated from this research; First, BIAS-3 [5], a program for the nonlinear DC solution of bipolar circuits was developed which was later included into SLIC [6] to address the analysis of linear bipolar ICs. The need for accurate large-signal time-domain simulation for the characterization of highly nonlinear circuits such as oscillators fueled the research for numerical integration and the development of program TRAC [7] at Autonetics, a division of Rockwell Corporation, and CIRPAC [8] at Bell Labs. The algorithms of TRAC evolved into programs TIME [9] at Motorola, and SINC [Sinc] at Berkeley. These efforts have been continued through the 1970s with the MSINC program at Stanford, and MTIME which is still in use at Motorola.

The algorithmic research carried out during the development of these programs converged to the use of the Newton-Raphson solution of nonlinear equations, limiting techniques, implicit integration methods using fixed time step, and reordering schemes for sparse matrices.

The emphasis on linear IC design using bipolar technology explains the priority given the implementation of bipolar device models, diodes and transistors. CANCER [1] implemented the Ebers-Moll [10] model for the bipolar transistor described by 18 parameters. The circuit size was limited to 400 components, with only 100 transistors and diodes, and up to 100 nodes. The circuit decks were submitted on punched cards and the program was developed and initially used on a CDC 6400.

An excellent review of the algorithms, techniques, and milestones in circuit simulation evolution can be found in a paper by D. Pederson [11].

2. SPICE in the 1970s

It is actually in the early 1970s that L. Nagel continuing to develop the CANCER-type of program called the new version SPICE, Simulation Program with Integrated Circuit Emphasis. In May 1972 SPICE1 [2] has been distributed for the first time in the public domain.

The most important addition to this program has been in the area of semiconductor device models. A better model for bipolar transistors has been introduced in 1970, the integral charge-control model of H. Gummel and C. Poon [12]. This model, available in SPICE1, included second-order effects such as high-level injection and low-level recombination, and represented a major advancement over the Ebers-Moll model.

Models for two other semiconductor devices have been added to SPICE1: the Junction-Field-Effect Transistor (JFET), and the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). In this first implementation the two models were very similar and were based on the first-order quadratic model of H. Shichman and D. Hodges [13].

A new approach to IC modeling, known as macromodeling [14] was introduced at this time to overcome the long run-times

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required by the use of detailed transistor-level schematics. The first macro-models have been developed for operational amplifiers by replacing many transistors through functionally equivalent controlled sources which are simulated much faster. Macro-models are to this day the main approach to represent SPICE equivalent circuits for a variety of complex ICs.

A novel circuit-theoretical concept, the adjoint network [15], introduced by Rohrer and Director in the late 1960s was used to add very efficient computation for sensitivity, noise and distortion in SPICE.

The next major release of the program, SPICE2 [3], was completed in 1975 and offered significant improvements over SPICE1. A new circuit representation known as Modified Nodal Analysis (MNA) [16], [6], replaced the old nodal analysis. This new representation added support for voltage-defined elements such as voltage sources and inductors.

A memory management package was developed in SPICE2 [4] which allowed the program to allocate dynamically the entire available memory to the solution of the circuit. This capability addressed the need to design larger ICs which by the mid 1970s had grown in complexity and the component limit of SPICE1 had become a serious limitation.

The accuracy and speed of the analysis have been improved by adding a time-step control mechanism and the stiffly stable multiple-order integration method of Gear [17].

Independent research on circuit simulation conducted at IBM led to the ASTAP program [18]. ASTAP used a different circuit representation, known as Sparse Tableau which allowed access to all desired circuit state variables at the cost of run time and memory. Similar to SPICE2 it used implicit, variable-order integration and Newton-Raphson nonlinear solution which led to their classification as third-generation circuit simulators [19].

A noteworthy event took place in the second half of the 1970s with the introduction by NCSS of ISPICE, Interactive SPICE, the first commercially supported version. This trend of commercial SPICE derivatives grows considerably in the 1980s.

In the late 1970s all semiconductor companies used circuit simulation, and most had adhered to SPICE. IC technology had advanced the complexity of circuits to Large-Scale Integration, LSI, and these circuits used mostly N-channel MOS devices. A new push has been given by industry to improve the SPICE2 device models to keep up with technology.

The representation of MOSFETs in SPICE2 was significantly overhauled at this time. It was important to add device geometry information such as Drain- and Source Areas, Perimeters, and Number of Squares. In addition to the simple square-law MOSFET model available in 1976 two more complex models have been added which described such effects as subthreshold conduction, carrier velocity-limited saturation, short- and narrow-channel effects [20]. The need to measure sub-pC charges in memory cells has also led to the implementation of a charge-based MOS model [21] in addition to the existing piece-wise-linear Meyer capacitance model [22].

Bipolar transistor geometries were also shrinking and the frequency of operation rising. Improvements such as Base Pushout, split Base-Collector capacitance, substrate capacitance, and transit time modeling have been added to the Gummel-Poon model.

The increase in circuit size has also brought about the need of increasing the accuracy of the sparse matrix solution by allowing for run-time pivoting to correct any singularity which may occur during a long transient simulation.

3. SPICE in the 1980s

At the beginning of the 1980s the introduction of the minicomputer has given engineering groups easier access to computer resources and SPICE has seen a tremendous increase in use. The VAX 11/780 quickly became the platform of choice for running SPICE and engineers were able to view the results of the simulation on their terminals as soon as the analysis had been completed.

With the proliferation of the number of users it has become obvious that support for SPICE users was lacking. Large companies had internal CAD groups dedicated to support and enhance software packages for their engineers. Small engineering firms however had little help when using public domain programs like SPICE. This need has been the driving force of new businesses with the charter to upgrade and support the public domain SPICE2. Examples include HSPICE from Meta Software [23].

LSI complexity chips required electrical simulation speeds in excess of an order of magnitude faster than SPICE. A number of approaches for speeding up electrical simulation by relaxing the accuracy and/or limiting the class of circuits to which it can be applied have been used in several programs. Timing simulators such as MOTIS, MOS TIming Simulator [24], which was first introduced in the mid 1970s, led the way to a number of programs which took advantage of MOSFET characteristics, time sparsity of events in digital circuits and the absence of feedback. Although fast, timing simulators did not have the accuracy needed in the design of sophisticated microprocessor and memory chips. Algorithmic innovation in timing simulation [25] led to the Waveform Relaxation technique, exemplified by the RELAX2 program [26], and Iterated Timing Analysis used in the SPLICE simulators [27], [28], [29]. This class of electrical simulators achieved speedups in excess of an order of magnitude compared to SPICE for MOS digital circuits. The attempt to use these programs to characterize analog circuits required the implementation of the more accurate and time-consuming SPICE device models, and often resulted in longer run-times than SPICE.

A different approach to faster simulation of complex ICs is the Mixed-Mode or Hybrid simulation, where individual blocks can be evaluated depending on the performed function, e.g., only analog blocks need electrical characterization, while digital blocks can be evaluated using logic simulation. Early efforts in this category include SPLICE from UC Berkeley, DIANA form University of Leuven [30], and SAMSON from Carnegie-Mellon University [31]. In spite of these first programs good commercial mixed-mode simulators are lacking. One possible explanation is the need of customization of mixed-mode simulators to specific applications which goes against the desire of software tools companies to develop universal tools.

Another approach to speed up electrical simulation has been to tailor the direct method algorithms of SPICE2 to various parallel computer architectures. Examples include CLASSIE [32] which was developed at UC Berkeley for CRAY vector computers, Single-Instruction Multiple-Data (SIMD) machines, and PACSIM [33] of SIMUCAD Corp. for Multiple-Instruction Multiple-Data (MIMD) computers, like Sequent or Alliant machines based on the MSPLICE project at UC Berkeley. Program SLATE [34] which emerged from research at University of Illinois, Urbana, decoupled the analysis of circuit blocks and took advantage of latency to speed up the time-domain simulation. A different way to more speed has been to build dedicated hardware accelerators for circuit simulation algorithms [35], [36].

These accelerators did not make it beyond a prototype due to either insufficient performance or inflexibility.

Speed-ups of up to an order of magnitude have been achieved for circuits with a regular structure and described in a hierarchical fashion. Flat circuit netlists often the result of layout extractors could be simulated only a few times faster. The lack of impressive speed returns and the customization needed for the various parallel architectures, as well as the emergence of RISC workstations with ever increasing processing speeds, doomed these efforts in the late 1980s.

Another major development by mid 1980s was the proliferation of the Personal Computer in the engineering field. By early 1984 PSPICE [37], the first PC version of SPICE, has become available on the IBM PC-XT. Although 8 times slower than on a VAX 11/780, the de facto reference for SPICE throughput, PC-based SPICE programs have contributed to attract many new users and considerably expand the popularity of this electric simulator.

SPICE received an additional boost from three companies, Daisy, Mentor, and Valid, a.k.a. DMV, which in 1981-1982 introduced integrated software packages for electronic design using microprocessor-powered engineering workstations. The business they developed has been called Computer-Aided Engineering. All three addressed the most lucrative business of digital design first. The need for an integrated analog simulation tool which covers design entry, simulation, and graphic display of results on the same screen/workstation had become obvious.

DMV realized this need and linked their schematic capture to a SPICE version and developed waveform display tools. Daisy took the lead in electrical simulation development by supporting an improved SPICE2 version, DSPICE, as part of its analog Virtual Lab software, while the other two offered an user interface with SPICE2 or deferred the choice of the simulator to the end user. A new company, Analog Design Tools, emerged in 1985 with a well-integrated analog CAE product, the Analog Workbench, an Apple Macintosh-like user interface, which extended the realm of electric simulation to board-level analog engineers and power supply designers, who historically had been reluctant to use computers. Both ADT and Daisy developed analog component libraries needed by analog system designers.

The major achievement of these CAE companies has been to extend the use of SPICE to the system/board-level analog designer and to add new functionality and models to the program to serve the needs of those applications.

The SPICE technology has also been advanced by the contributions of talented CAD groups at Bell Labs, Analog Devices, Texas Instruments, Hewlett Packard, Tektronix, Harris Semiconductor, and National Semiconductor. Most of these groups had provided output display tools on graphic terminals in the second half of the 1970s. During the 1980 decade the effort was directed towards robust convergence, e.g., ADICE from Analog Devices and TekSPICE from Tektronix, accurate semiconductor device modeling, e.g., TI SPICE, ADVICE at Bell Labs, and HP SPICE, and additional functionality and user-friendly features. Although these proprietary developments have not been available to the user at large ideas and results of this parallel research work eventually found their way in public-domain or commercial software.

University research made new contributions to the SPICE technology during this decade. At the beginning of the 1980s the wide-spread use of UNIX in the university research environment offered the potential for increased interactivity between user and program. SPICE2 however was a Fortran batch program which was difficult to modify and limited in its potential use of C-shell utilities. This realization led to the SPICE3 project [38] at UC Berkeley which had as goals to rewrite and improve SPICE2 version 2G6 [39] using the C language to produce an interactive, modular, easy to understand, structured program with a graphic tool for result display. SPICE3 [40] was released in the public domain in March 1985.

An important achievement of the concurrent SPICE work in this decade has been the elimination to a large degree of convergence problems. The use of continuation methods and education of users have contributed towards reliable DC analysis. Improved models as well as techniques to handle discontinuities have resulted in a robust time-domain simulation as well.

An interesting concept which gained support towards the end of the 1980s was to provide the user the capability of describing the functions which govern the operation of devices used in the simulation. This feature was first available in ASTAP and then expanded in the SABER simulator [41] from Analogy. SABER, initially developed as a piece-wise linear electrical simulator addressed at the simulation of analog systems, promoted the behavioral representation of entire circuit blocks by time-domain or frequency-domain equations. Modeling entire circuit blocks at a functional level rather than transistor level speeds up the simulation and enables a designer to evaluate an entire analog board or system.

4. Where to SPICE in the 1990s?

In 1990 SPICE is synonymous to analog computer-aided simulation. Any major supplier of analog CAD/CAE software offers a well supported and enhanced version of SPICE2 or SPICE3. The major CAE companies, Mentor, Valid and Cadence, offer a proprietary SPICE version as part of their analog CAE products, Accusim, Analog Workbench, or Analog Artist, respectively. The main emphasis for the near future is on increased functionality, higher-level modeling, and integration with schematic capture, display tools, and component libraries, as well as with physical design tools, such as Printed-Circuit Board and Integrated Circuit Layout.

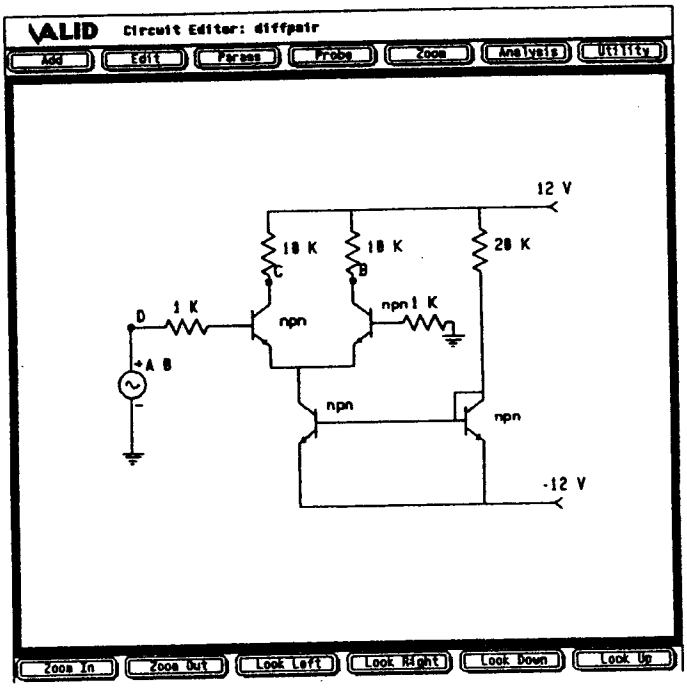

Figure 1: Scematic of Differential Amplifier

An example of a state-of-the-art analog CAE product is the Analog Workbench II [42] from Valid. All information needed for simulation is entered in graphical form and through menus. The circuit is entered as an electric schematic. In order to simulate a differential amplifier a schematic as shown Fig. 1 replaces the old SPICE netlist. Input signals are defined and checked in a Function Generator tool shown in Fig. 2. The time-domain simulation is controlled by pop-up menus and the resulting waveforms can be viewed and measured in an oscilloscope tool as seen in Fig. 3; a similar setup with a Frequency Sweeper and a Network Analyzer tool is used to control and view the results of an AC small-signal analysis of the differential pair as shown in Fig. 4.

Significant research will be dedicated in extending the functionality of electrical simulation beyond the established analysis modes of SPICE, i.e., nonlinear DC and time-domain, and small-signal frequency-domain. A number of interesting developments have started in this direction at the end of the 1980 decade.

One extension is exemplified by SPECTRE [43], a nonlinear frequency-domain analysis program, which has been developed at UC Berkeley. Solution in frequency domain is especially useful for finding the steady-state response of circuits with distributed elements and high-Q resonators. This approach is not very efficient for nonlinear transistor circuits.

Another direction of research is steady-state analysis which solves the above problem in time domain. This mode is particularly important for circuits with long settling times, such as switching power supplies. Although research on this topic took place in the 1970s, [44], there is no reliable program available today. Current research is underway at MIT and UC Berkeley; an envelope-following method is used in NITSWIT [45] while S-SPICE [46] is a vehicle to study various shooting techniques for the steady-state solution.

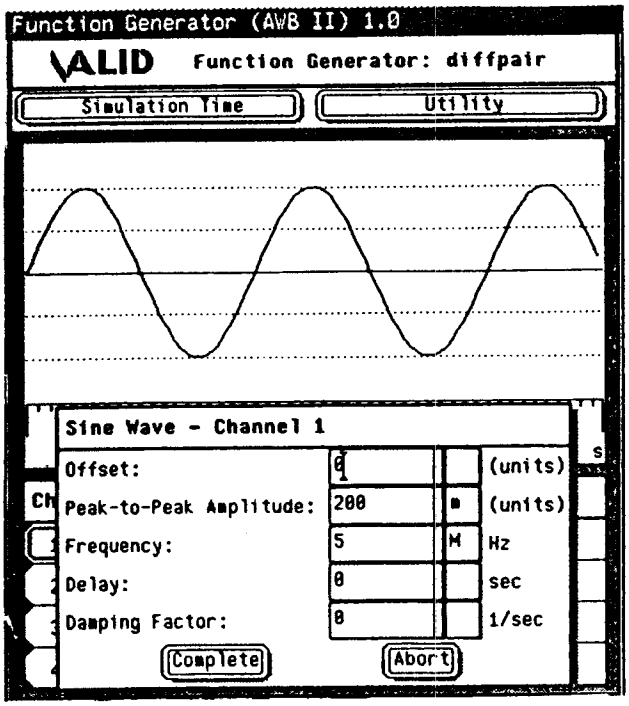

Figure 2: Function Generator Tool for Input Signals

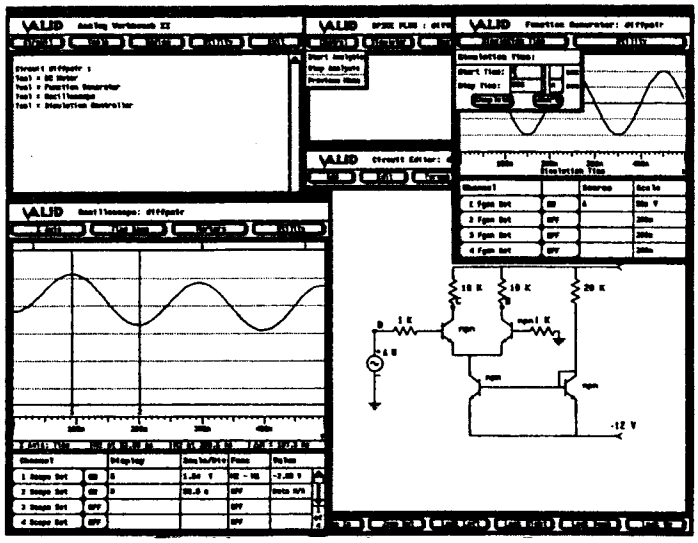

Figure 3: Screen Plot of Time-Domain Analysis Tools

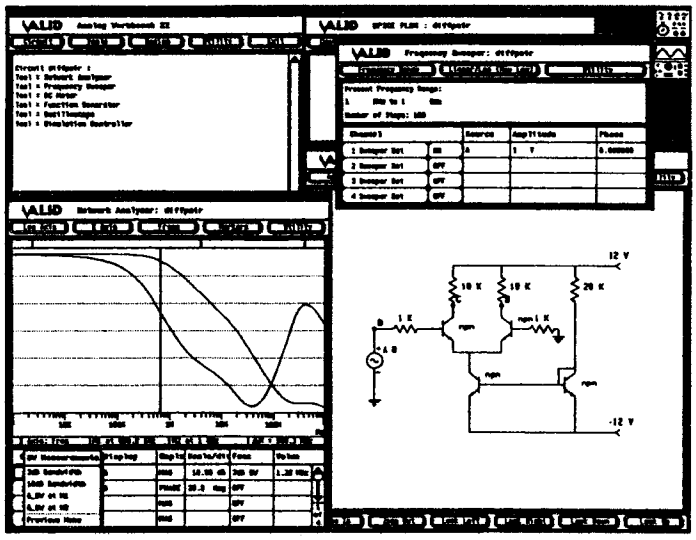

Figure 4: Screen Plot of Frequency-Domain Analysis Tools

SPICE also lacks capabilities for specific applications such as filter design in general and switched capacitor filters in particular. Specialized programs such as SWITCAP [47] have been developed to fill this need. This trend of developing specific functionality for given applications which are not well suited for traditional SPICE analysis will continue in this decade.

Modeling technology is an important aspect of circuit simulation and is instrumental in defining capabilities and accuracy of a program.

At the top level of circuit representation more support will be developed for behavioral/structural description of entire circuit blocks. The ability to represent entire circuit blocks by one or a set of equations will make it possible to simulate complete analog systems. Such functionality creates the need for powerful model generation software capable of automating the process. Also a description language for analog behavior is under development under the guidance of the IEEE Standards Coordinating Committee 30, Analog Hardware Descriptive Language [48].

At the transistor level representation in order to keep up with ever shrinking semiconductor devices SPICE will probably evolve to an open architecture which enables CAD groups of IC manufacturers to implement better device models or to upgrade the default ones. Improved transistor models have been reported in technical journals during the last decade with little impact on the various SPICE releases. Examples include the MEXTRAM model [49] for bipolar transistors which is reported to describe quasi-saturation and high-frequency effects better than the current Gummel-Poon model and which could be an useful addition to SPICE.

While for the last two decades circuit simulation has been used mostly for analyzing fully-specified circuits, this decade more emphasis will be put on the design aspect. Research work in the area of analog synthesis has been reported by groups at Carnegie-Mellon University, Centre Suisse d'Electronique et de Microelectronique (CSEM), and University of California, Berkeley; the synthesis tools these groups have developed, OASYS [50], IDAC [51], and OPASYN [52], respectively, can be used to design well-defined circuit blocks, e.g., operational amplifiers, from a collection of analog cells available in the knowledge base. During the next decade analog synthesis tools will evolve to facilitate the design of complex analog and mixed analog-digital systems. In conjunction with other software modules SPICE will form the analysis core of analog optimization and synthesis software tools.

5. Conclusion

The new developments in circuit simulation do not obsolete SPICE but rather complement it. SPICE will continue to be the main electrical simulator because it solves the fundamental equations of an electrical system. In a recent report on PC-based analog simulation [53] published in EDN magazine, the author concludes that "for the foreseeable future nothing will supplant SPICE as the industry standard for analog simulation." SPICE will probably add a number of analysis modes, e.g., nonlinear frequency-domain, and higher-level modeling capabilities by supporting blocks described by integro-differential or algebraic equations.

Advances in computer technology will also increase the applicability of circuit simulation. Over the next few years the power of engineering workstations will increase to 1000 Mips, 1000 MBytes memory and 1000 GBytes disk storage according to Bill Joy's forecast at the 1990 Design Automation Conference [54]. This translates into a 50,000 transistor circuit simulation capability. One important upgrade needed in SPICE to make such a large simulation a reality is the decoupling of the analysis of circuit blocks at the differential or nonlinear equation level.

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