

Homework #5 (Due Date: Feb 22 by 5pm/Extension allowed to: Feb 25 in class)

1. Read the following paper: D. Shaeffer and T. Lee, "A 1.5V, 1.5GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, pp. 745-759, May 1997. Note that some of the equations are not correct – use class notes for these and the corrections: "Corrections to 'A 1.5V, 1.5GHz CMOS low noise amplifier,'" *IEEE J. Solid-State Circuits*, pp. 1397-1398, June 2005 (Note that the term κ (Eq. (23)) is incorrect even in this correction), "Comment on Corrections to 'A 1.5-V, 1.5-GHz CMOS low noise amplifier'," *IEEE J. Solid-State Circuits*, p. 2359, Oct 2006. Assume R_1 and R_g in Fig. 7 are zero and derive the following expression for the noise figure of the amplifier. Note: this is the correct equation corresponding to Eq. (28) in the original paper.

$$F = 1 + \frac{\gamma}{\alpha} \frac{X}{Q_L} \left(\frac{\omega_0}{\omega_T} \right) \quad \text{where } X = 1 - 2|c| \sqrt{\frac{\delta\alpha^2}{5\gamma} + \frac{\delta\alpha^2}{5\gamma} (1 + Q_L^2)}$$

2. a) Design an inductively degenerated narrowband CMOS LNA for the following specifications using the 0.18 μm TSMC process. $V_{DD} = 1\text{V}$, $f_0 = 2.4\text{ GHz}$, $\text{NF} = 2.5\text{ dB}$, $s_{21} = 10\text{ dB}$, $s_{11} \leq -12\text{ dB}$, $s_{12} \leq -15\text{ dB}$, $s_{22} \leq -12\text{ dB}$. Both the input and output have to be matched to 50 ohms. The bias current should not exceed 2mA. Simulate and verify your design. The transistor model files (BSIM3) are available on the class web page. Recall that the Spice/Spectre/ADS MOSFET models do not account for the induced gate noise. The BSIM3 channel thermal noise model does not account for the excess short-channel noise (γ) that could be important for the shortest channel lengths. Assume that you have ideal inductors but include all transistor parasitic capacitances.
 - b) What are the simulated s-parameters, IIP3, and NF for your design? Show the frequency spectrum for an input signal of -12dBm.
 - c) For the calculated source inductor value, design an on-chip spiral. Use the technology file on the class web page to design the on-chip spiral. You can choose to use a bondwire or external inductor for the gate.
 - d) Redesign the LNA using appropriate equivalent circuit models for all the inductors. Simulate and verify your design.
 - e) Redesign the LNA taking into account the package pin parasitics. Assume that the bond pad can be modeled as a capacitor of value 0.1 pF. Assume the package has an inductance of 6nH (for each pin and the bondwire) and use as many pins as you need. Simulate and verify your design. What are the simulated s-parameters, IIP3, NF, and the Stern stability factor for your design? Show the frequency spectrum for an input signal of -12dBm.
 - f) Repeat part (e) assuming the package has a pin and bondwire inductance of 3nH for all pins and bondwire. Compare the performance of this design with that of (e).

Notes:

- You may use HSPICE, SpectreRF or Agilent/EEsof- ADS for circuit simulations.
- It may be difficult to meet the specifications for NF with parasitics included. In that case, you need to get the best possible NF and provide an explanation for why you could not meet the NF specifications.
- The L_{min} for this process is $0.18\mu\text{m}$. If you use minimum channel length transistors you need to include the excess drain noise (γ). Use a value of $\gamma = 2$.
- For including the transistor junction capacitances use the following rules $AD = AS = 0.6e-12*W$, $PD = PS = 2e-6*(W+0.6)$, where W is the transistor width in μm .
- For ASITIC/COILS the minimum spacing between metal traces is $0.8\mu\text{m}$. Also the minimum metal trace width is $0.6\mu\text{m}$ and the maximum metal trace width is $30\mu\text{m}$.
- Assume a bond wire inductance of 1nH/mm .
- You may find the following paper useful for inductor design. "Simple accurate expressions for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1419-1424, October 1999.
- The design and simulations for parts (b), (d), (e), and (f) should include gate noise and excess drain noise ($\gamma=2$, $\delta=4$). Note that the excess drain noise is required if you use transistors with $L = L_{min}$. For transistors sized with $L \geq 2*L_{min}$, you can ignore the effect of excess drain noise i.e., use $\gamma=2/3$ and $\delta=4/3$.
- For including excess drain noise using a subcircuit model, refer to the paper in *IEEE J. Solid-State Circuits*, Dec. 2000, pp. 1909-1910.
- Since you have not been asked to design a bias circuit - use the simplest possible biasing for your LNA.
- You may want to refer to Ken Kundert's article on simulation of IP_3 on the class webpage.