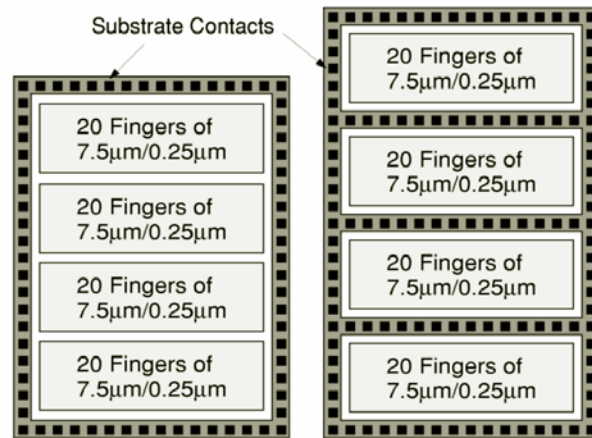


## Layout for Reducing Epi-Noise



Q.Huang et al., IEEE JSSC, March 1999

## MOSFET Noise Models in SPICE

- Gate noise model available only in BSIM4
- Channel thermal noise is typically based on long-channel model

$$\text{SPICE 2} \quad \overline{i_d^2} = 4kT \left( \frac{2}{3} g_m \right) \Delta f$$

$$\text{BSIM3 implementation of SPICE 2} \quad \overline{i_d^2} = 4kT \frac{2}{3} (g_m + g_{ds} + g_{mb}) \Delta f$$

- Short-channel factor  $\gamma$  not included
- BSIM3 thermal noise model related to inversion layer charge  $Q_i$

$$\overline{i_d^2} = 4kT \frac{\mu}{L^2} |Q_i| \Delta f$$

## MOSFET at High Frequencies

- Distributed effects that must be modeled
  - Distributed channel: Nonquasistatic (NQS) modeling
  - Distributed gate: Gate resistance modeling
  - Distributed substrate: Substrate network modeling

## Non-Quasistatic Operation Modeled As Gate Resistance

- From Tsividis's book

$$Y_{11} \approx j\omega C_{gs} \frac{1}{1 + j \frac{2\omega}{15\omega_0}} \quad \omega_0 = \frac{\mu(V_{gs} - V_T)}{L^2}$$

$$R_G = \frac{1}{5g_{d0}} \quad g_{d0} = \frac{\mu C_{ox} W (V_{gs} - V_T)}{L}$$

$$R_G = \frac{1}{5g_{m,sat}}$$

Y. Tsividis., Operation and Modeling of The MOS Transistor, 1999.

## Gate Resistance Modeling

- A distributed analysis for a wide gate MOSFET

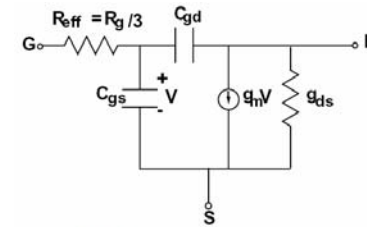
$$\eta_{\text{exact}} = \frac{\tanh \sqrt{sR_g C_g}}{\sqrt{sR_g C_g}}$$

- Two approximations

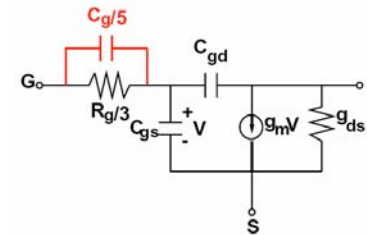
$$\frac{\tanh \sqrt{sR_g C_g}}{\sqrt{sR_g C_g}} \approx 1 - \frac{1}{3} sR_g C_g \approx \frac{1}{1 + \frac{1}{3} sR_g C_g}$$

$$\frac{\tanh \sqrt{sR_g C_g}}{\sqrt{sR_g C_g}} \approx 1 - \frac{1}{3} sR_g C_g + \frac{2}{15} (sR_g C_g)^2 \approx \frac{1 + \frac{1}{15} sR_g C_g}{1 + \frac{6}{15} sR_g C_g}$$

## Razavi's and Improved Circuit Models



Razavi's Circuit Model

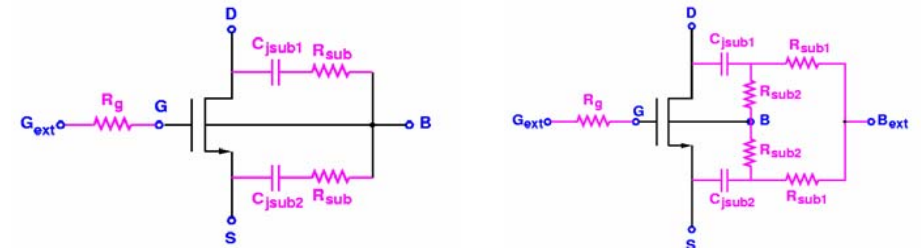


Improved Circuit Model

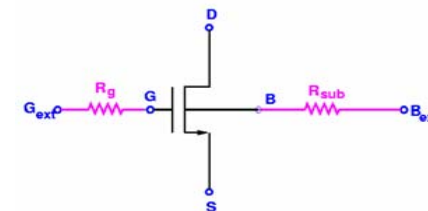
## Substrate Modeling

- Substrate parasitics important at high frequencies (GHz range)
- Parasitics can be incorporated as an external substrate network
- Several circuits proposed
  - Resistive network
  - External capacitance: C<sub>bd</sub> and C<sub>bs</sub>

## Various Substrate Networks



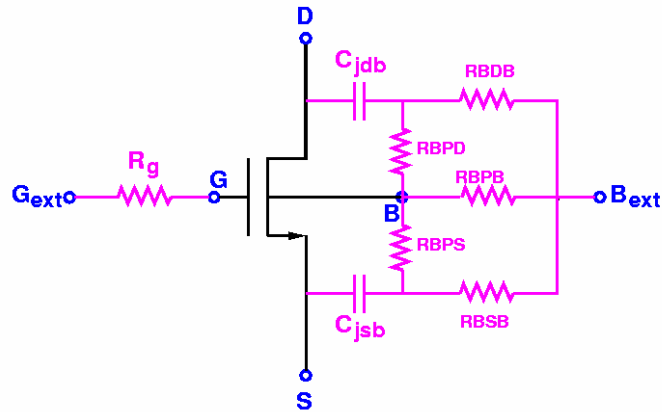
J. J. Ou et. al., UC Berkeley, 1998      W. Liu et. al., Texas Instruments, 1997



S.F.Tin, et. al., 2000

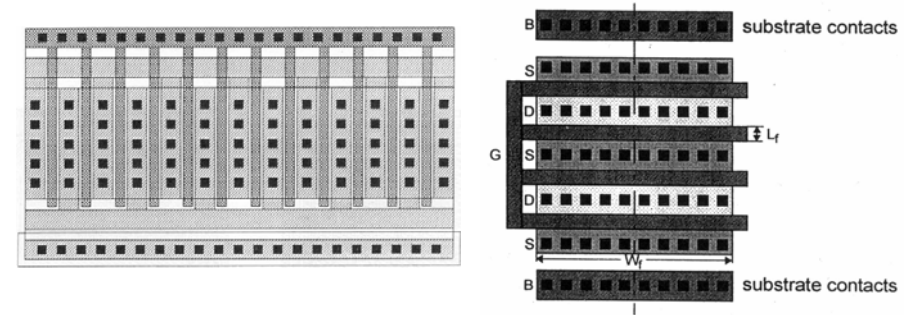
## BSIM4 Substrate Network

- Flexible substrate network with 5 external resistances



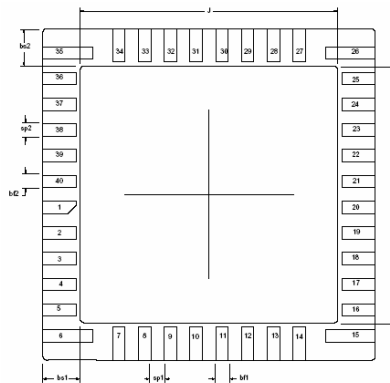
## Substrate Resistances

- The values of the substrate resistances depend on the transistor layout and the placement of substrate of contacts

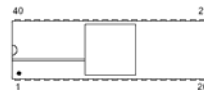


- Substrate network must reflect this dependence on layout

## DIP40 Package

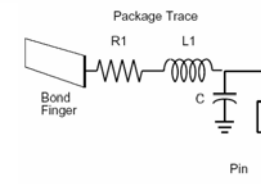


Dimension	Designation	Nominal	Units/Material
J, K	Cavity length	0.310	sq. in.
bs1	Bond shelf width	0.045	in.
bs2	Bond shelf width	0.045	in.
bf1	Bond finger width	0.015	in.
bf2	Bond finger width	0.015	in.
sp1	Finger spacing	0.016	in.
sp2	Finger spacing	0.016	in.

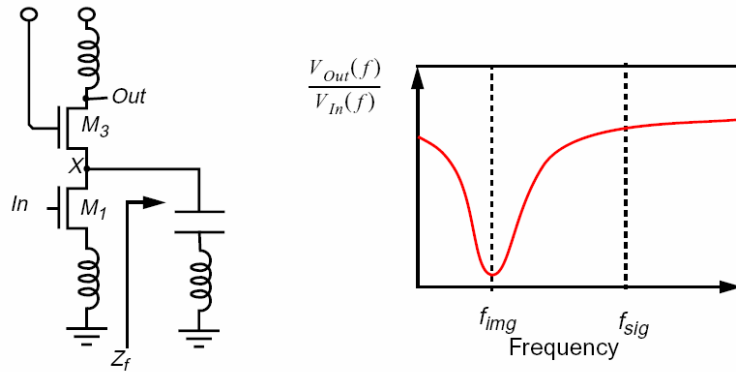


## DIP40 Electrical Characteristics

Pin	R ( $\Omega$ )	L (nH)	C (pF)	$t_{or}$ (ps)
1,20,21,40	0.217	8.18	5.32	209
2,19,22,39	0.177	7.92	4.39	187
3,18,23,38	0.154	7.34	3.37	157
4,17,24,37	0.110	6.48	2.34	123
5,16,25,36	0.103	5.69	2.16	111
6,15,26,35	0.0661	4.37	1.43	79.0
7,14,27,34	0.0646	4.54	1.48	81.9
8,13,28,33	0.0498	3.69	1.05	62.3
9,12,29,32	0.0378	3.54	0.863	55.3
10,11,30,31	0.0247	3.15	0.660	45.6



## Noise Rejection with Series Tuned Circuit

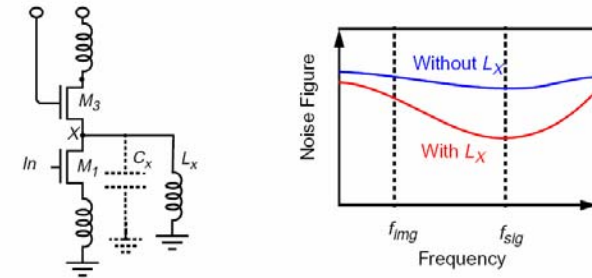


- Series resonance @  $f_{img}$  → improves image rejection

Samavati et al. IEEE JSSC, May 2000.

## Effect of Parasitic Capacitance

Parasitic capacitance  $C_x$  degrades the noise performance.



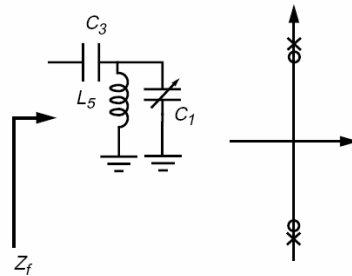
- Parallel resonance @  $f_{sig}$  → improves noise figure

## Use Third-Order Filter

$$Z_f(s) = \frac{L_5 \cdot (C_3 + C_1) \cdot s^2 + 1}{C_1 \cdot C_3 \cdot L_5 \cdot s^3 + C_3 \cdot s}$$

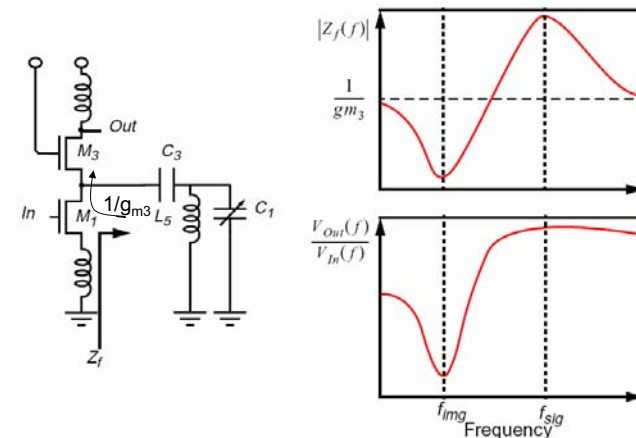
$$\omega_z = \pm \frac{1}{\sqrt{L_5 \cdot (C_3 + C_1)}}$$

$$\omega_p = \pm \frac{1}{\sqrt{L_5 \cdot C_1}}$$



Varactor controls the location of the pole-zero pair

## Final Circuit and Transfer Function



- Third-order filter rejects the image and also diminishes the effect of parasitic capacitance
- 12 dB image rejection