

Comments and Corrections

Corrections to “A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier”

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The authors of the above paper [1] would like to report an error concerning expression (23) in the original paper that was brought to their attention by some alert readers. In that expression, the term Q_L should be deleted. In the process of reviewing the mathematical treatment, the authors also identified an additional, unrelated error concerning expression (20) in the paper. Namely, the sign of the drain and gate noise correlation coefficient, c , should be reversed for the noise source reference polarities indicated in the original Fig. 7. Doing so will make the correlation consistent with that derived by van der Ziel [2]. Note that he adopts the opposite (and unconventional) reference polarity for the drain current noise while also indicating a positive sign for the correlation coefficient. The correct correlation coefficient and related noise source polarities are shown in Fig. 1.

Accounting for these two errors, the following expressions appearing in Section III of the original paper require minor revisions:

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{i_g^2 i_d^2}} \approx -0.395j \quad (20)$$

$$\kappa = \frac{\delta\alpha^2}{5\gamma} |c|^2 + \left[1 - |c| \sqrt{\frac{\delta\alpha^2}{5\gamma}} \right]^2 \quad (23)$$

$$\chi = \kappa + \xi = 1 - 2|c| \sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma} (1 + Q_L^2). \quad (28)$$

These revised expressions are identical to the originals, except for the removal of the extra factor of Q_L from the last term in (23) and from the middle term in (28) and the reversal of the sign of the correlation coefficient, c , in all three expressions.

The remaining corrections indicated here follow directly from the revisions noted above. In particular, the derivations presented in Section IV of the original paper should be revised to reflect these changes. Expression (41), which is the basis of subsequent derivations, should read

$$P(\rho, P_D) = \frac{P_D P_1(\rho) + \frac{P_0}{P_D} P_2(\rho)}{\rho^3 \left(1 + \frac{\rho}{2}\right)^2 (1 + \rho)} \quad (41)$$

where

$$\begin{aligned} P_1(\rho) &= (1 + \rho)^6 - 2|c| \sqrt{\frac{\delta}{5\gamma}} \left(1 + \frac{\rho}{2}\right) (1 + \rho)^4 \\ &\quad + \frac{\delta}{5\gamma} (1 + \rho)^2 \left(1 + \frac{\rho}{2}\right)^2 \\ P_2(\rho) &= \frac{\delta}{5\gamma} \left(1 + \frac{\rho}{2}\right)^2 \rho^4. \end{aligned}$$

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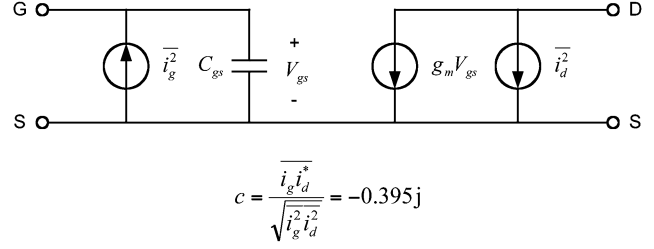


Fig. 1. Simplified MOSFET small-signal equivalent circuit model showing gate and drain noise generators. For the polarity shown, the noise correlation coefficient is as indicated in the long-channel limit.

The following expressions in the *Fixed G_m Optimization* subsection should be revised:

$$P_{D,opt,G_m} = P_0 \frac{\rho^2}{1 + \rho} \left[1 - 2|c| \sqrt{\frac{5\gamma}{\delta\alpha^2}} + \frac{5\gamma}{\delta\alpha^2} \right]^{-1/2} \quad (44)$$

$$Q_{L,opt,G_m} = \left\{ 1 - 2|c| \sqrt{\frac{5\gamma}{\delta\alpha^2}} + \frac{5\gamma}{\delta\alpha^2} \right\}^{1/2} \geq 1.500 \quad (45)$$

$$\begin{aligned} F_{min,G_m} &= 1 + \sqrt{\frac{4}{5}} \delta\gamma \left(\frac{\omega_0}{\omega_T} \right) \\ &\quad \times \left\{ 1 - 2|c| \sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma} \right\}^{1/2} \\ &= 1 + 0.849 \sqrt{\delta\gamma} \left(\frac{\omega_0}{\omega_T} \right) \\ &\geq 1 + 0.800 \left(\frac{\omega_0}{\omega_T} \right) \end{aligned} \quad (46)$$

where the numerical results are strictly valid only in the long-channel limit.

The following expressions in the *Fixed P_D Optimization* subsection should also be revised:

$$P(\rho, P_D) \approx \frac{P_D}{P_0} \left(1 - 2|c| \sqrt{\frac{\delta}{5\gamma}} + \frac{\delta}{5\gamma} \right) + \frac{P_0}{P_D} \frac{\delta}{5\gamma} \rho^4 \quad (47)$$

$$\rho_{opt,P_D}^2 = \frac{P_D}{P_0} \sqrt{3} \left\{ 1 - 2|c| \sqrt{\frac{5\gamma}{\delta\alpha^2}} + \frac{5\gamma}{\delta\alpha^2} \right\}^{1/2} \quad (49)$$

$$\begin{aligned} Q_{L,opt,P_D} &= \sqrt{3} \left\{ 1 - 2|c| \sqrt{\frac{5\gamma}{\delta\alpha^2}} + \frac{5\gamma}{\delta\alpha^2} \right\}^{1/2} \\ &\geq 2.598 \end{aligned} \quad (50)$$

$$\begin{aligned} F_{min,P_D} &= 1 + \sqrt{\frac{16}{15}} \delta\gamma \left(\frac{\omega_0}{\omega_T} \right) \\ &\quad \times \left\{ 1 - 2|c| \sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma} \right\}^{1/2} \\ &= 1 + 0.980 \sqrt{\delta\gamma} \left(\frac{\omega_0}{\omega_T} \right) \\ &\geq 1 + 0.924 \left(\frac{\omega_0}{\omega_T} \right) \end{aligned} \quad (51)$$

where the numerical results are strictly valid only in the long-channel limit. From these revisions, it is clear that the optimum Q and minimum noise figure are both slightly lower than indicated in the original paper.

Expression (52) in the subsection entitled *Discussion of F_{\min}* should be revised as well to reverse the sign of the correlation coefficient:

$$B_{cor} = \omega C_{gs} \left[1 - |c| \sqrt{\frac{\delta \alpha^2}{5\gamma}} \right] \geq 0.75 \omega C_{gs}. \quad (52)$$

Once again, the numerical result is only indicative of the long-channel limit.

Finally, expression (53) in Section V would also be revised in light of the new value for optimum Q :

$$W_{M1,opt,PD} = \left[\frac{2}{3} \omega_0 L C_{ox} R_s Q_{L,opt,PD} \right]^{-1} \approx 860 \mu\text{m}. \quad (53)$$

However, it should be noted that the optimum width indicated by (53) is pessimistically large in light of the overlap capacitance, which is neglected in the original analysis. Subsequent work using a complete device model with induced gate noise indicated that the optimum Q is relatively insensitive to the value of the overlap capacitance [3]. Accordingly, the optimum device width is somewhat lower than that given in (53). An improved (though still approximate) expression for optimum

device width accounting for the above-noted revision to optimum Q and assuming 2fF total gate capacitance (including overlap) per micron of gate width is

$$W_{opt} \approx \frac{600 \mu\text{m-GHz}}{f_0} \quad (1)$$

where f_0 is given in GHz.

Apart from the above-noted revisions, the remaining expressions in the original paper are correct. These revisions do not affect the general conclusions of the paper, though some of the numerical results are modified (particularly, the values for optimum Q_L and the achievable noise figures, as indicated).

The authors sincerely regret any confusion that these errors may have caused. They are also grateful to the readers of the original paper who alerted them to the first error, thereby prompting these revisions.

REFERENCES

- [1] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.
- [2] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York, NY: Wiley, 1986, pp. 88–90.
- [3] D. K. Shaeffer and T. H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*. Boston, MA: Kluwer, 1999.