January 6, 2020

class web page material
(Syllabus/reference sheet/exam examples/hw)

Calendar, quiz...

next lecture

http://eecs.oregonstate.edu/~mooon/ece323/lectures

This notes/scrivble are mode available.
Microelectronic Circuits by Sedra & Smith (& Carusone & Gaudet)

HW  Homework will not be graded based on right or wrong answers, but on the level of effort shown in what you submit each week. Each assignment is to be submitted on the due date at the **beginning** of class. No late homework will be accepted. Homework grading will be done using one of three scores: 10, 5, or 0. A complete/good effort and understanding demonstrated will receive a 10; insufficient work will receive a 0; and a 5 for something in between.

Exams  Exams are **closed** book, **closed** notes, and no calculator. I will provide a “reference sheet” for the exam. This sheet will be made available well before the exam so that you’d know what to expect.

OH  Please ask specific questions at office hours, referring to a copy of my own writing (e.g. posted lecture notes, homework solutions...). Bring printed notes/solutions that I posted or show it on your laptop (not on your phone).

Grade  **Homework**

<table>
<thead>
<tr>
<th>Grade</th>
<th>Percentage</th>
<th>Date</th>
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<tbody>
<tr>
<td>Midterm-1</td>
<td>25%</td>
<td>(Monday Feb-3 in class)</td>
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<td>Midterm-2</td>
<td>25%</td>
<td>(Monday Mar-2 in class)</td>
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<tr>
<td>Final</td>
<td>35%</td>
<td>(Tuesday Mar-17 9:30-11:20am)</td>
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**Academic Dishonesty** (cheating) is defined as an act of deception in which a student seeks to claim credit for the work or effort of another person, or uses unauthorized materials or fabricated information in any academic work or research, either through the student's own efforts or the efforts of another. [See Code of Student Conduct document at http://studentlife.oregonstate.edu/studentconduct]. **Exams:** Talking, looking at another student’s exam, using prohibited items like cellphone, notes, calculator... **Homework:** Copying (whole or partial) solutions, copying (whole or partial) another student’s work... What will be the penalty? You will receive 0% for that and potentially for the entire course. You will also be reported to the university.
Your reading guide for the course...
Section numbers are from the eighth edition, but you can find the same topic in older editions.

Course overview; ECE 322 review
5.1 Device structure and physical operation (MOSFET)
5.2 Current-voltage characteristics (MOSFET)
5.3 MOSFET circuits at DC
6.1 Device structure and physical operation (BJT)
6.2 Current-voltage characteristics (BJT)
6.3 BJT circuits at DC
7.1 Basic principles (transistor amplifiers)
7.2 Small-signal operation and models (transistor amplifiers)

Single stage amplifiers
7.3 Basic configuration (transistor amplifiers)
7.4 Biasing (transistor amplifiers)
7.5 Discrete-circuit amplifiers (transistor amplifiers)

Multi stages & building blocks
8.2 IC biasing: current sources and current mirrors
8.3 The basic gain cell
8.4 The common-gate and common-base amplifiers as current buffers
Parts of 9.* (differential and multistage amplifiers)

Frequency response
10.1 High-frequency transistor models
10.2 High-frequency response of CS and CE amplifiers
10.3 The method of open-circuit time constants
10.8 Low-frequency response of discrete-circuits CS and CE amplifiers

Feedback
11.*

Oscillators/feedback & stability
15.1 Basic principles of sinusoidal oscillators
15.2 Opamp-RC oscillator circuits
15.4 Nonlinear oscillators or function generators

Digital logic
16.1 CMOS logic-gate circuits
16.2 Digital logic inverters
16.3 The CMOS inverter
17.2 Transistor sizing (Digital design: power, speed, and area)
This is a tentative schedule/calendar, except those in bold are permanent

<table>
<thead>
<tr>
<th>Dates</th>
<th>Course overview; ECE 322 review</th>
<th>Single stage amplifiers</th>
<th>Multi stages &amp; building blocks</th>
<th>Multi stages &amp; building blocks continued</th>
<th>MIDTERM-1</th>
<th>Frequency response</th>
<th>Feedback</th>
<th>Frequency response continued</th>
<th>Oscillators/feedback &amp; stability</th>
<th>Oscillator/feedback continued</th>
<th>Digital logic</th>
<th>HW1 due</th>
<th>HW2 due</th>
<th>HW3 due</th>
<th>HW4 due</th>
<th>HW5 due</th>
<th>HW6 due</th>
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<td><strong>MLK Jr. Holiday</strong></td>
<td>Multi stages &amp; building blocks</td>
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<td>Oscillators/feedback &amp; stability</td>
<td>HW5 due</td>
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<td>Mar. 2, 4, 6</td>
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<td>Mar. 9, 11, 13</td>
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**FINAL EXAM at 9:30-11:20am on Tuesday 3/17**
MOSFET:
\[ I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 \quad \text{or} \quad I_D = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_{TN})V_D - \frac{V_D^2}{2} \right] \]
\[ g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TN}) = \sqrt{2 \mu C_{ox} \frac{W}{L} I_D} \]

BJT:
\[ I_C = I_S \exp \left\{ \frac{V_{BE}}{V_T} \right\} ; \quad V_T = kT/q \approx 25mV (@\text{RoomTemp}) ; \quad I_S = \text{Device Parameter} \]
\[ g_m = \frac{I_C}{V_T} ; \quad r_\pi = \frac{\beta}{g_m} ; \quad \frac{I_c}{I_b} = \beta \]