http://eecs.oregonstate.edu/~moon/ece423

Prof. Un-Ku Moon <moon@oregonstate.edu> / KEC-4093 / OH: as shown below & by appointment
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Reference texts: Analysis and Design of Analog Integrated Circuits, Gray/Hurst/Lewis/Meyer
Analog Integrated Circuit Design, Carusone/Johns/Martin
Design of analog CMOS integrated circuits, Razavi

I do not follow any textbook outline for this course, but these are excellent books. I presume you already have the Gray/Hurst/Lewis/Meyer book from ECE 422/522.

Course content: This class is a continuation of ECE 422/522 and a prerequisite to ECE 520. This course is geared towards learning commonly practiced CMOS IC design and analysis. We will do some IC layout work to expose you to tools commonly used today (this portion will be taught by the TA). At the end of the course, you will have learned a circuit designer’s approach (less mathematical and more intuition driven) to transistor-level design. The final class project will be a design of a fully differential opamp, which will involve schematic capture, transistor-level simulation, IC layout, layout versus schematic (LVS) verification, layout design rule check (DRC),...

Computer tools: SPICE, MATLAB, and Cadence Design Environment (for layout, schematic capture, physical design checking tools, etc.).

Grading: The course grading will be weighted as follows.

Homework * 25%
Midterm exam 25% (Wed Feb-12 in class)
Circuit design project † 25% (Due Fri Mar-13 midnight)
Final exam 25% (Mon Mar-16 at 6-7:50pm)

* All assignments must be done in pairs (submit one), and no more than twice with the same people/pair during the term. Only the one last person without a partner does it alone (i.e. everyone else must be paired). You may use the class mailing list to find a partner. The homework assignments are essentially the same each year. The homework is intended for your learning/benefit. They will be handed back with a “✓” (3 pts) for good work or “✓−” (2 pts) for lacking work. The “best” among the submitted homework will be scanned and posted on the class web page as “solutions.”

† Each turn in his/her own project (i.e. no partners).