In the bias circuit shown below...

Find \( g_m \) (transistor M1).

Find the proper sizing of M2 transistor for optimum biasing.

Find the equivalent resistance at node Vx.
Find the output-referred noise and the input-referred noise.
In the amplifier shown below...

Design the bias BP and specify transistor sizing for zero systematic offset.

Design the bias BZ for right-half-plane zero cancellation.

Find the input to output small-signal gain expression.
In the circuit shown below, find the output-referred noise. Assume that the circuit is balanced (i.e. $M_1a=M_1b$, $M_2a=M_2b$).
Using one ideal reference current source to ground, design the bias and CMFB for the amplifier shown below. Find the differential gain and CM loop gain.
In the current source shown below, appropriately specify the three transistor sizes for optimum biasing.
Find the output resistance.
For the amplifier shown below, find the input-referred noise (expression).
Design optimum bias and CMFB circuits for the amplifier shown below. Use one ideal current source to ground and one ideal CM voltage reference. Specify device sizes as needed – 1x device size is assumed unless specified. Then find the input to output small-signal gain (expression) and CMFB loopgain (expression).
In the bias circuit shown below, find the resulting current ratio $I_1$ to $I_2$ and $I_2$ to $I_3$. Also find the resulting $gm_1$, $gm_2$, and $gm_3$ of transistors M1/M2/M3 (expression).
Find the equivalent small-signal output resistance (expression). Assume 1X devices unless specified otherwise (e.g. 2X). Also assume input common-mode voltage is large enough (and not too large) to keep all transistors in saturation.
For the amplifier shown below, find the output-referred noise (expression) and input-referred noise (expression).
Design optimum bias and CMFB circuits for the amplifier shown below. Find the small signal input to output gain (expression) and CMFB loopgain (expression). Specify device sizes as needed. A “1X” device size will be assumed if a device size is not specified.
Specify transistor sizes so that $\text{UGBW} \approx 1/(RC)$. A “1X” device size will be assumed if a device size is not specified.
Find $I_{out}$. Specify W/L ratios of M1 and M2 for optimum biasing.
Find the output-referred noise and the input-referred noise. Assume all transistors are in saturation.
Using an ideal reference current source and an ideal 2.5-V common-mode reference voltage source, design the optimum bias BP and common-mode feedback which feeds CMFB node. Specify all transistor sizes.
Find the small-signal gain (expression) of the amplifier shown below. Be sure to take care of multiple signal paths.
First ignore the branch in the dotted circle (i.e. assume gate of M1 is properly biased with a fixed DC voltage), and find the output resistance (expression). Now consider the branch in the dotted circle which controls the gate of M1, and find the output resistance (expression). Finally, find the resulting numerical value of the bias current $I_b$.

![Circuit Diagram]