Assuming that the dashed lines are not connected, design the bias circuit for BP1/BP2/BP3, and specify all transistor sizes in the bias circuit and the top two PMOS transistors currently unspecified [15pts]. Now, considering the dashed line connection, specify which transistor dimensions must change (and to what W/L ratio) to maintain optimal biasing [10pts].
Assuming that the dashed lines are not connected, design the bias circuit for BP1/BP2/BP3, and specify all transistor sizes in the bias circuit and the two PMOS transistors currently unspecified. Now, considering the dashed line connection, specify which transistor dimensions must change (and to what W/L ratio) to maintain optimal biasing.
Design the bias circuit for BP1/BP2/BP3/BN1/BN2 and specify appropriate transistor sizes. Make sure no systematic offset results from transistor sizing. Assuming $W/L$ of MZ is half that of M3, design the bias for BZ such that RHP is canceled. Find the approximate input to output small-signal gain (expression only).

![Schematic Diagram]

$V_{DD} = 5V$
Design the bias circuit for BN1/BN2/BP1 and specify W/L of M7. Find the input to output small-signal gain (expression only).

![Circuit Diagram](image)

$V_{DD} = 5V$
Design the bias circuit for BP1/BP2/BN1/BN2/BN3/BN4. They are 1X devices unless specified otherwise (e.g. 2X). Find the approximate input to output small-signal gain (expression).
Specify W/L dimensions for the five biasing transistors for optimum biasing.
Find the equivalent small-signal output resistance (expression). They are all 1X devices.
All transistors are labeled, so be sure to be precise with parameter names. {e.g. $g_{m2}$, $r_{o5}$} What is the Norton-equivalent $G_m$ and $R_{out}$?
For the opamp shown below, specify W/L of PMOS bias circuit made of M7, M8, and M9. Specify W/L for M5 and M6 such that there is no systematic offset. Design the bias circuit for BN. Find the small-signal gain expression.
Find the Norton equivalent “Gm” and “Rout”.

[Diagram of the circuit with the values 200 µA, 50 µA, 50/1, 100/1, M1, M2]
 Appropriately size transistors M1 to M6 for optimum biasing.
What is the resulting output current $I_{\text{OUT}}$? Find (expressions with $V_T$’s and $\Delta$’s) all node voltages, and the output resistance (expression - label transistors as needed) of the current source. Assume $1X$ devices unless specified otherwise (e.g. $2X$).
Design the optimum bias and specify transistor sizes. Find the small signal gain (expression) from input to output.
First, ignore the dotted current source, and appropriately size the transistors. Now include the dotted current source, and re-size the transistors as needed. Device sizes already specified must be kept as is.
Find the Norton equivalent small-signal $G_m$ and $R_{out}$ (expression). Assume $1X$ devices unless specified otherwise (e.g. $2X$). Assume $V_{DC}$ is large enough (and not too large) to keep all transistors in saturation.