Opamp Design

I. Introduction
In this homework the goal is to design a two-stage single ended CMOS op-amp with Miller compensation. The paper is organized as follows: in section II, the design procedure about how to determine the topology and parameters is presented; In section III, a table comparing simulated results with the specifications is provided; Finally, all simulations results are given in section IV.

II. Design Procedure
1. Circuit Structure
The design circuit is shown in Figure1. M1-M5 is the first stage to provide large gain; M6-M7 is the second stage to provide high output swing; C_o is the Miller capacitor to split the two poles; R_a is the resistor to move the zero frequency.

![Design Circuit](image)

Figure 1 Design circuit

2. Find gm and current
Assume parasitic capacitors are much smaller than C_o and C_i, so parasitic capacitors are ignored. Set C_o=2pF, so

Assume p=1.5ω, so

The zero compensates the p. Then,

By setting V_o=0.2mV,

3. Find W and L

From the above equation, the requirements for Lambda is set. The Lambda is calculated for different L. To satisfy the gain requirements, the minimum length is 400μm. Because the error between manual calculation
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and simulation, the final values for netlist are a little different and are shown as below.

<table>
<thead>
<tr>
<th>MOSFETS</th>
<th>W/L VALUES um</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>20.48/0.4</td>
</tr>
<tr>
<td>M3, M4</td>
<td>53/0.4</td>
</tr>
<tr>
<td>M5</td>
<td>320/1</td>
</tr>
<tr>
<td>M6</td>
<td>159/0.4</td>
</tr>
<tr>
<td>M7</td>
<td>480/1</td>
</tr>
<tr>
<td>M8</td>
<td>160/1</td>
</tr>
</tbody>
</table>

Table 1 Values for transistors

III. Simulated Results and Conclusion

The simulated results are shown in Appendix. The design completely meets the design specifications.

Table 2 Comparison between specifications and simulated results

<table>
<thead>
<tr>
<th>Specification</th>
<th>Specification</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open loop gain</td>
<td>≥ 60dB</td>
<td>60.78dB</td>
</tr>
<tr>
<td>Phase margin</td>
<td>≥ 60°</td>
<td>63°</td>
</tr>
<tr>
<td>Unity gain frequency</td>
<td>≥ 160MHz</td>
<td>165MHz</td>
</tr>
<tr>
<td>Output Swing</td>
<td>1Vpp</td>
<td>(0.186V, 2.2V)</td>
</tr>
<tr>
<td>Power consumption</td>
<td>10mW</td>
<td>3mW</td>
</tr>
</tbody>
</table>

IV. Appendices

Appendix I Netlist of the Opamp

* # FILE NAME: /NFS/STAK/STUDENT/SCHEMATIC/NETLIST/OP.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON JAN 13 15:24:31 2017
* GLOBAL NET DEFINITIONS
  .GLOBAL VDD!
* FILE NAME: TEST.OP.SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: OP.
* GENERATED FOR: HSPICES.
I7 VDD! VB DC=200E-6
C1 VOUT 0 4E-12 M=1.0
C0 NET023 VOUT 2E-12 M=1.0
R0 NET13 NET023 1080 M=1.0
V0 VDD! 0 2.5
V1 2 0 1.0
V2 1 0 1.0 AC=1
MP6 VOUT NET13 VDD! VDD! TSMC25DP L=400E-9 W=159E-6 ad=104.94p as=104.94p
pd=319.32u ps=319.32u
MP4 NET13 NET17 VDD! VDD! TSMC25DP L=400E-9 W=53E-6  ad=34.96p as=34.96p
pd=107.32u ps=107.32u
MP3 NET17 NET17 VDD! VDD! TSMC25DP L=400E-9 W=53E-6  ad=34.96p as=34.96p
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INCLUDE FILES

END OF NETLIST

.include

AC DEC 10 1 10G

OPTION POST

.save

.END

Appendix II Simulated Results
Figure 2  DC output voltage range
Figure 3: AC analysis results