1. \[ \text{req} = \infty \]

\[ V_i = -V_{gs} \]

\[ -g_m V_i + I = \frac{V_i}{r_0} + V - I R_s \]

\[ -g_m (V - I R_s) + I = \frac{V - I R_s}{r_0} \]

\[ g_m V + I R_s + I = \frac{V - I R_s}{r_0} \]

\[ I \left( \frac{g_m R_s}{r_0} + \frac{1}{r_0} \right) = \frac{V}{r_0} \left( 1 + g_m \right) \]

\[ \text{req} = \frac{V}{I} = \frac{g_m R_s + \frac{1}{r_0}}{1 + g_m \frac{r_0}{r_0} + g_m} \]

\[ = \frac{r_0 + R_s (1 + g_m \frac{r_0}{r_0})}{r_0 + g_m} \]

\[ \text{req} = r_0 \]

\[ V_i = -V_{gs} \]

\[ V_2 = I R_0 \]

\[ I = g_m V_i = \frac{V_i - V_2}{r_0} \]

\[ I = g_m V_i = V_1 - I R_0 \]

\[ \frac{I}{1 - \frac{R_0}{r_0}} = \frac{V_1}{1 + g_m \frac{r_0}{r_0}} \]

\[ \text{req} = \frac{V}{I} = \frac{1 + \frac{R_0}{r_0}}{1 + g_m \frac{r_0}{r_0}} \]

\[ V_x = -g_m V_x + \frac{V - V_x}{r_0} \]

\[ V_x = I R_3 \]

\[ I \left( 1 + g_m \frac{R_3}{r_0} \right) = \frac{V}{r_0} \]

\[ \text{req} = \frac{V}{I} = \frac{r_0 + R_0 + g_m R_3 r_0}{r_0 + g_m R_3} \]
\[ R_{eq} = [R_S + r_{o1} + r_{o1} g_m R_S] + r_{o2} + r_{o2} g_m R_S \]

\[ R_{eq} = \frac{r_{o1} + [r_{o3} + r_{o2} + g_{m2} r_{o2} r_{o3}]}{1 + g_{m2} r_{o3}} \]

\[ R_{eq} = r_{o1} + r_{o2} \frac{r_{o3}}{1 + g_{m2} r_{o3}} \]
**Circuit 1:** Figure 1.1 shows the first circuit, which is biased such that $V_{out} = 1.602V$ and $I = 51uA$. The netlist is also included to show that proper device sizing was met.

![Figure 1.1: Circuit with DC biases shown](image)

```
M1 N006 Vin N007 0 CMOSN l=0.5u w=20u
R1 N007 0 1k
V1 N001 0 2.5
V3 N008 0 0.6286
M2 Vout N005 N006 0 CMOSN l=0.24u w=10u
M3 N003 Vout N001 CMOSP l=0.24u w=20u
M4 N001 N002 N003 N001 CMOSP l=0.5u w=40u
V4 N005 0 1.1
V5 N004 0 1.4
V6 N002 0 1.8
V2 Vin N008 AC 1 0
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\wilso\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc25
.ac dec 10 1 1G
.op
.backanno
.end
```
Figure 1.2 shows the circuit modifications that were made to find Gm and Rout. For Gm, a large capacitor was connected to the output, and Gm was calculated as the current through the capacitor divided by the input voltage. Figure 1.3 shows Gm.

\[ Gm = \frac{I(C1)}{V(Vin)} = 385.37 \mu S \]

For Rout, the ac source on vin was removed, and a current source was added at the output, with Rout calculated as the voltage across the current source divided by its current. Figure 1.4 shows Rout.

\[ Rout = \frac{V(Vout)}{I(I1)} = 3.51 \text{Mohms} \]

These values were used to calculate Gain.

\[ Gain = Gm * Rout = 385.37 \mu * 3.51 M = 1.35 k \]

Figure 1.5 shows the simulated gain, which was identical to the gain calculated from Gm*Rout

\[ Gain = \frac{V(Vout)}{V(Vin)} = 1.35 k \]
Figure 1.3: Simulation of Gm

Figure 1.4: Simulation of Rout
Figure 1.5: Simulation of Gain
Circuit 2: Figure 2.1 shows the second circuit, which is biased such that $V_{\text{out}} = 1.258\,\text{V}$ and $I = 200.4\,\mu\text{A}$. The netlist is also included to show that proper device sizing was met.

![Circuit diagram](image)

**Figure 2.1: Circuit with DC biases shown**

```
M1 N001 N002 N001 CMOSP l=0.24u w=30u
M2 N001 N002 Vout N001 CMOSP l=0.24u w=45u
V1 N001 0 2.5
M3 N002 Vin N003 N003 CMOSN l=0.24u w=20u
M4 Vout N004 N003 N003 CMOSN l=0.24u w=20u
M5 N003 N005 N006 0 CMOSN l=0.24u w=30u
M6 N006 N007 N008 0 CMOSN l=0.5u w=60u
V2 Vin N004 AC 1 0
V3 N004 0 1.4
V4 N005 0 1.2
V5 N007 0 0.831
I1 Vout 0 110\mu
R1 N008 0 1k
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\wilso\Documents\LTspiceXVII\lib\cmp\standard.mos
.include tsmc25
* .step param Io 10u 500u 10u
* .ac dec 10 1 10G
.op
.backanno
.end
```
Figure 2.2 shows the circuit modifications that were made to find Gm and Rout. For Gm, a large capacitor was connected to the output, and Gm was calculated as the current through the capacitor divided by the input voltage. Figure 2.3 shows Gm.

\[ G_m = \frac{I(C1)}{V(V_{in})} = 1.87\text{mS} \]

For Rout, the ac source on vin was removed, and a current source was added at the output, with Rout calculated as the voltage across the current source divided by its current. Figure 2.4 shows Rout.

\[ Rout = \frac{V(V_{out})}{I(I2)} = 9.25\text{kOhm} \]

These values were used to calculate Gain.

\[ Gain = G_m \times Rout = 17.3 \]

Figure 2.5 shows the simulated gain, which was identical to the gain calculated from Gm*Rout

\[ Gain = \frac{V(V_{out})}{V(V_{in})} = 17.3 \]
Figure 2.3: Simulation of $G_m$

Figure 2.4: Simulation of $R_{out}$
Figure 2.5: Simulation of Gain