Opamp transistors and sizes shown.

Schematic - Folded Cascode Opamp
Biasing transistors and sizes shown.
Opamp transistors and operating points shown.
Biasing transistors and operating points shown.

OP - Folded Cascode Opamp Bias
Simulation

Schematic (Testbench sources shown)

Power = 7.8 mW
Schematic

DC Gain = 55 dB
UGBW = 283 MHz
PM = 78 deg
Schematic

Input swing = 1.026 mVp-p
Output swing = 0.543 V p-p
Offset = 513 uV
Complete layout shown with 6 pF load capacitor
Layout - Folded Cascode Opamp

Layout shown without load capacitor
Clean DRC
LVS
Testbench
Simulation

Layout

Power = 7.51 mW
DC Gain = 50.13 dB
UGBW = 256 MHz
PM = 82 deg
3dB Output swing = 0.8 Vp-p

Symmetric
Input swing = 204.6 uVp-p
Output swing = 66 mVp-p
Offset = 956 uV