Design a fully differential operational amplifier meeting the following specifications. And also complete the IC layout of the opamp that passes DRC and LVS. Everything is to be done in the Cadence environment using the TSMC 0.18um setup. Use an ideal power supply (1.8±0.1V), an ideal common-mode voltage reference of your choosing (fixed for all cases), and an ideal reference current source to ground (fixed for all cases). If you use resistors, the nominal value must be less than or equal to 25kΩ. Finally, you are not allowed to use RHP zero cancellation in this project.

Simulations are to be completed for three process corners: TT (with temp=27°C & V_DD=1.8V), SS (with temp=85°C & V_DD=1.7V), and FF (with temp=−40°C & V_DD=1.9V).

Specifications (for all three cases):

- Power supply: V_DD=1.8V, 1.7V, 1.9V (TT, SS, FF)
- Load at each output: C_load=3pF (to be affected by TT, SS, FF)
- Loop gain: > 70 dB
- Loop UGBW: > 70 MHz
- Loop Phase Margin: > 60°
- CMFB Phase Margin: > 60°
- CM accuracy (with no differential signal): < ±0.05V
- Output swing (6dB/50% compression): > 1V peak-to-peak differential
- Power consumption (including bias): < 9 mW

Differential Loop characteristics are to be obtained with 1pF input and feedback capacitors (fixed 1pF value for all cases). Use 1GΩ resistors as needed for simulation purposes. Eliminate the 1pF input/feedback capacitors when doing CMFB evaluation. About a 2/3 of your project grade will depend on this design and simulation portion.

The second part of the project is IC layout. Grading depends on whether you pass LVS and DRC, and the quality of your layout (ask yourself if the layout “looks” good). About a 1/3 of project grading will depend on this layout portion.

ECE 523 (graduate class): Using the opamp that you have designed, design a second-order Butterworth lowpass filter with a 200 kHz (at TT) corner frequency. Provide simulation results for all three cases (TT/SS/FF). No IC layout is required for this filter design. You may write a few sentences for this section to explain what/why/how you did your design.

Write-up tips (these tips come from those who will grade your project)

- Every specification needs evidence it passed - reporting it passed without evidence doesn't hold up.
- Performance on all specifications should be reported/shown.
- Both (+ and −) of output nodes should be shown for output swing.
- Make sure all plots have enough points to clearly show the achieved results.
- Include opamp and testbench schematics.
- Schematics need to be clear - this usually means drawing them separately outside of Cadence.
- Sizing (W/L) should be on the schematic and clearly readable.
- Make sure your graphs and reported findings (e.g. table of results) match.