

Error Canceling Low Voltage SAR-ADC

by

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ERROR CANCELING LOW VOLTAGE SAR-ADC

Chapter 1

Introduction

1.1 Motivation

Signal processing is one of the major incentives to the fast development of electronic circuits. With the tremendous advancement of modern VLSI technology, people are able to build more and more complex digital circuits on a single chip to realize signal processing that is conventionally achieved by analog circuits, because digital circuit has advantages over its analog counterpart in several aspects such as much lower noise sensitivity, excellent signal regenerating capability. and it is easier to realize design and test automation as well. However, the object of signal processing - physical signals of the real world are always in analog form. Therefore, to facilitate the extensive DSP functions in the digital domain, interfaces between analog and digital blocks are omnipresent in all modern mixed signal processing integrated circuits. Analog to digital data converters are among the major components in the interfaces.

There are three conceptually distinct operations that are performed sequentially by an A/D converter [17]: (1) It samples a continuous-valued, continuous-time analog signal; (2) it quantizes the sampled signal to a finite number of levels; (3) it assign a digital code to the related quantized level. With this sequence of operations, any physical signal, no matter if it is mechanical, thermal, optical, acoustical, or magnetical, once it has been transformed into electrical signal by a proper sensor, it can be

converted into digital signal by an A/D converter and processed conveniently with powerful digital signal processing components, out of which various useful information can be extracted.

There are many approaches to realizing the analog-to-digital conversion. Some of these techniques, such as flash and pipeline [10] A/D converters trade off accuracy for speed. On the other end of the scale the highest accuracy is realized by oversampling A/D converters [13, 15], which have high tolerance to technological imperfections and component parameter variations but low conversion speed and high power consumption. The compromise between conversion speed and accuracy is achieved by Nyquist rate A/D converters such as algorithmic [9, 11] and successive approximate A/D converters, which have moderate speed and moderate precision.

Switched capacitor circuits have become popular because of their good linearity and dynamic range. Naturally, switched capacitor techniques are also applied to Nyquist rate A/D converters. However, if the conversions are realized by simple charge transfer between ratio-matched capacitors, as it did in the work of McCharles, et al. [11] as an early algorithmic A/D converter, the conversion accuracy will be fundamentally limited by the ratio accuracy. To overcome this problem, several circuit configurations have been proposed which perform the cyclic conversion in a capacitor ratio independent manner [8, 9, 20, 23]. In those approaches the conversion speed was sacrificed for ratio-independent property substantially. For instance, 6 clock cycles were needed for each bit's conversion in the design of Li, et al. [9] compared to 2 clocks in [11]. The approach proposed by Onodera, et al. [14] was able to decrease the number of clocks down to 3 for each bit. A further improvement for conversion speed without losing the ratio-independent feature was realized by Zheng, et al. [26], where a fully differential circuit structure was used and only 2 clocks were needed for each bit's conversion, which has the same conversion speed

as that of the ratio-dependent structure proposed by McCharles, et al. [11].

Similar to switched-capacitor algorithmic ADC, another type of Nyquist rate ADC – switched- capacitor successive approximation ADC also suffers from capacitor mismatch errors. Apart from developing a ratio-independent circuit structure, mismatch-shaping techniques ([1, 3, 19]) can be used to decrease the error. The approach proposed by Rombouts, et al. [18] realized the first order error cancellation, where a nearly distortion-free converter is obtained by employing additional signal processing with the cost of two fold increase of conversion time. To further improve the switched capacitor successive approximation ADC, a novel mismatch error canceling algorithm was proposed by Zheng, et al. [27], where only 50% of conversion time is needed to eliminate the first order mismatch error. As the continuation of this research, this thesis aims to improve the proposed algorithm and realize the circuit on a chip, which will be the test vehicle for the proposed circuitry for further improvement.

1.2 Thesis Structure

Chapter 2 describes the principle of successive approximate A/D converters, and general considerations of circuit non-ideality in realizing a switched capacitor successive A/D converter. Based on the detailed charge domain analysis of the ADC operations, an improvement of the algorithm proposed by Zheng, et al. [27] is provided by tracing the error charge free capacitor. To summarize the complete algorithm, 4 tables

representing the detailed operational sequences of the ADC to be designed are provided at the end of this chapter.

Chapter 3 studies the characteristics of the predictive correlated double sampling technique in switched capacitor successive approximation ADC. A detailed theoretical analyze of the operations of the proposed SC SAR–ADC is given. MATLAB simulations based on the theoretical results show that the conventional predictive CDS is not adequate to achieve high resolution SC SAR–ADC. The subtle difference in signal processing manners between predictive CDS in SC SAR-ADC and other applications is discussed. Further more, the predictive correlated triple sampling (CTS) technique is proposed to improve the inadequacy of predictive CDS in SAR–ADC, and this improvement is verified by SWITCAP simulations.

Chapter 4 gives the detailed design of the proposed SC SAR–ADC with National Semiconductor low voltage technology. Transistor level full chip simulation is given at the end of this chapter.

Chapter 5 summarizes the work of this thesis and the plan of future work.

Chapter 2

Mismatch Error Cancellation Algorithm

2.1 Conceptual Operation of a Successive Approximation ADC

Because of its reasonably high conversion speed with moderate circuit complexity and converting accuracy, successive approximation A/D converters (SAR – ADCs) are among those of the most popular Nyquist rate ADCs. The terms “Divided Reference Algorithm” or “Binary Search Algorithm” can be used to best describe the basic principle of a SAR – ADC.

Figure 2.1 depicts a possible scenario of the operation for a SAR – ADC to an input signal v_{in} , which is sampled at the beginning of each conversion cycle. Conversion starts with the comparison between input signal v_{in} and the half reference voltage $\frac{v_{ref}}{2}$, which determines the MSB of v_{in} and also determines the search region for the second MSB. In order to allow the binary search algorithm to approximate the actual v_{in} , the reference voltage used for MSB will be divided by 2 and the result will be added to or subtracted from the previous reference voltage, which delimitates the new binary search regions. As such, each comparison between v_{in} and updated reference voltage generates one bit of v_{in} , and N bits SAR-ADC will need N comparisons.

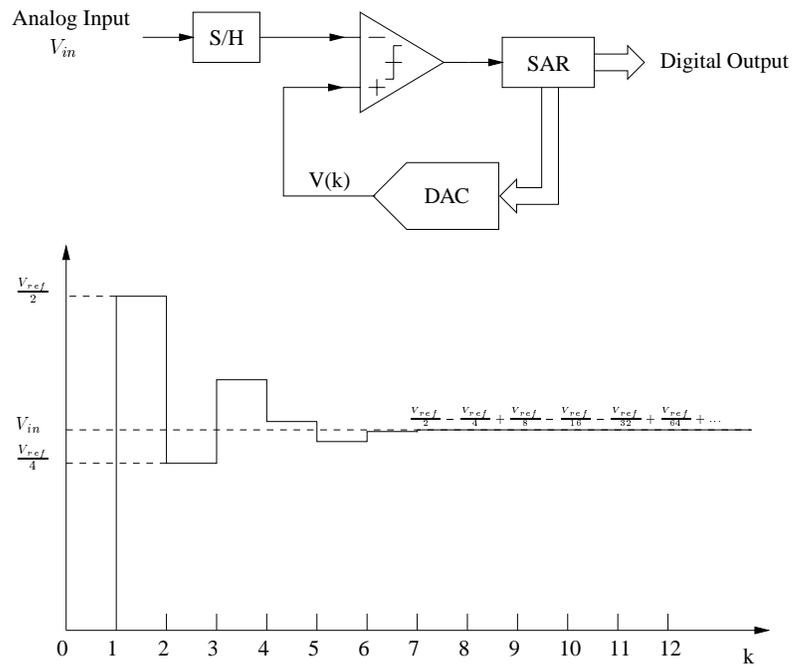


FIGURE 2.1: General successive approximation ADC

2.2 Circuit Non-idealities

Obviously, the above description is based on the ideal operation of a general SAR ADC. In real circuits, the “divided by two” operation to the reference voltage can be realized in various ways. In case of a switched capacitor circuit, it is normally implemented by sharing reference charge with two matched capacitors, as described in the paper by Zheng et al. [27]. Therefore any mismatch error between the two capacitors used to share charge will have a direct impact on the linearity of the overall converter.

Besides the capacitor mismatch error, there are other circuit non-idealities. In the low voltage design context, it is difficult to obtain high op-amp gain, thus circuit imperfection caused by op-amp finite gain is inevitable. Other non-avoidable circuit

non idealities include op-amp offset voltage, parasitic capacitances, charge injection and clock feedthrough, etc. The following is a brief description of a novel technique proposed by Zheng [25] to cope with above circuit imperfection.

2.3 A Novel Capacitor Mismatch Error Cancellation Technique for Switched Capacitor SAR – ADC

A novel capacitor mismatch error cancellation technique for switched capacitor SAR – ADC has been proposed by Zheng [25]. With this technique, the first order capacitor mismatch error is virtually eliminated at the cost of increasing by 50% the data conversion time. This is less than that required in a capacitance ratio independent cyclic A/D converter, where typically 100% additional conversion time is needed compared to the ideal operation. With this technique, not only the capacitance mismatch error has been cancelled, op-amp finite gain and offset voltage are also compensated by the application of the correlated double sampling (CDS) technique. Through the proper path arrangement of charge transfer in a fully differential structure, the influence of top plate parasitic capacitances are also suppressed.

Since there are 16 capacitors in the ADC core, in order to describe the operation more clearly, it is convenient to have a method for the systematic identification of each capacitor. The following convention will be used for the identifying subscripts of the capacitors:

First subscript:

- i or int — denotes an integrating capacitor;
- r or ref — denotes a capacitor which stores a reference charge;
- s or sig — denotes a signal capacitor, which shares charge with reference ca-

pacitor;

- e or err — denotes an error charge capacitor for CDS compensation.

Second subscript:

- 1 — denotes capacitors connected to the inverting input side of the fully differential op-amp;
- 2 — denotes capacitors connected to the non-inverting input side of the fully differential op-amp.

Third subscript:

- D or DAC — denotes CDS error charge capacitors of the op-amp;
- C or Comp — denotes CDS error charge capacitors of the comparator;
- p(predicting) — denotes capacitors used in predicting phase (of CDS operation);
- c(converting) — denotes capacitors used in converting phase (of CDS operation).

Then, the 16 capacitors in the circuit are

C_{int}	C_{ref}	C_{sig}	C_{err}
C_{i1p}	C_{r1p}	C_{s1p}	C_{e1D}
C_{i1c}	C_{r1c}	C_{s1c}	C_{e2D}
C_{i2p}	C_{r2p}	C_{s2p}	C_{e1C}
C_{i2c}	C_{r2c}	C_{s2c}	C_{e2C}

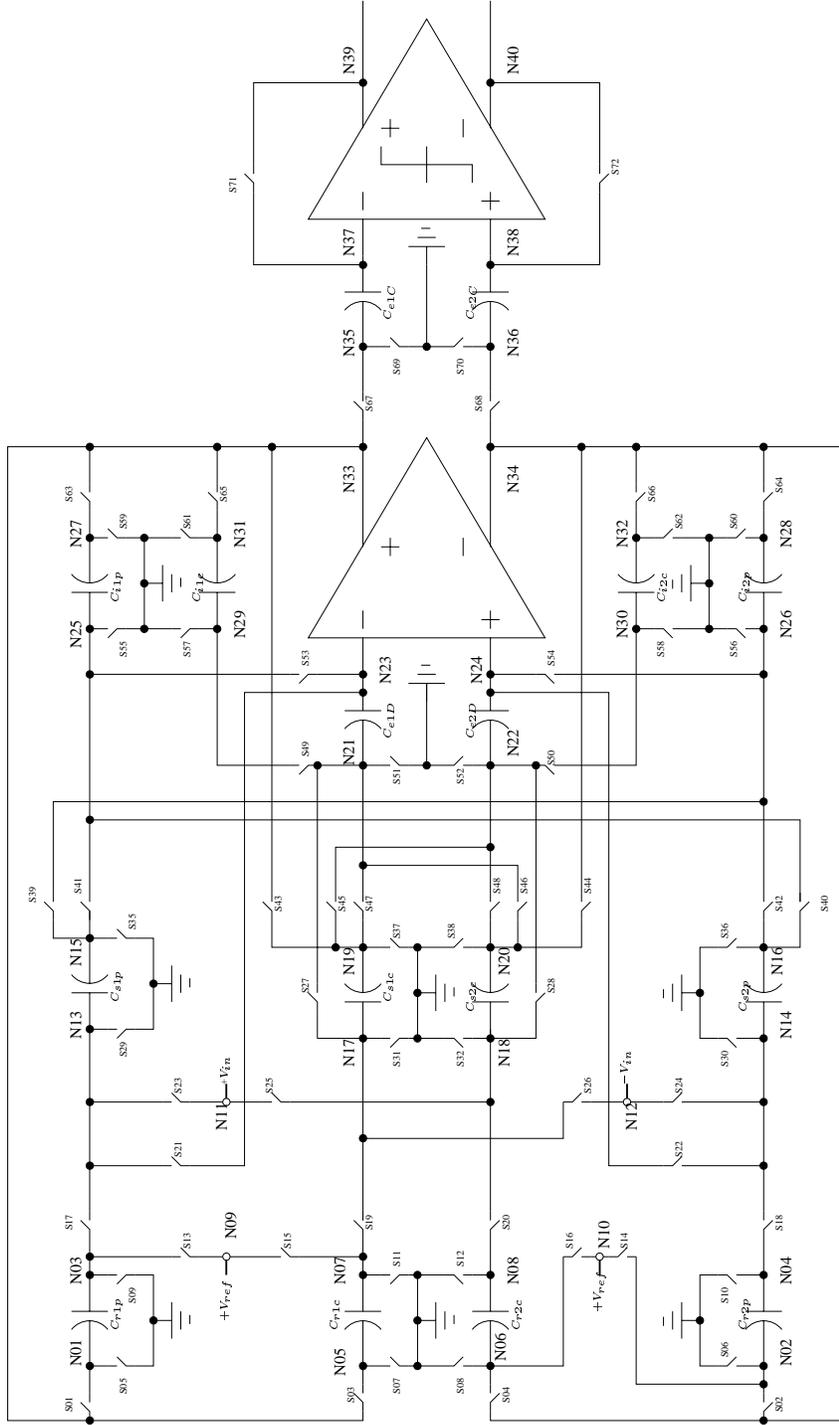


FIGURE 2.2: Circuit of 16 - bit switched-capacitor SAR - A/D converter

The complete circuit diagram of the switched-capacitor SAR A/D converter implementing the capacitor mismatch error cancellation algorithm is shown in Fig. 2.2. Drawing the connection of the crucial elements switched in each of the 6 phases needed to derive two bits in the digital output results in 14 different circuit configurations shown in Fig. 2.3 through Fig. 2.6.

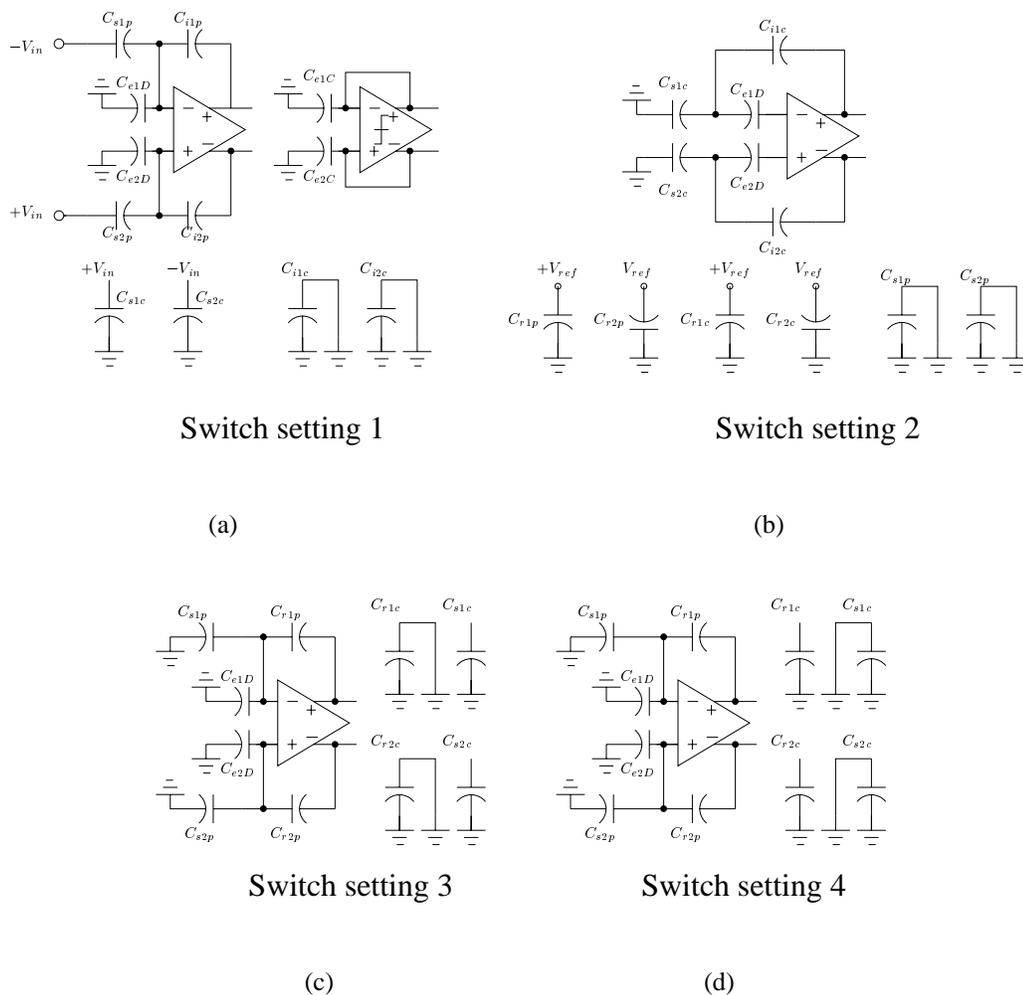


FIGURE 2.3: Circuits of switch setting 1 through switch setting 4

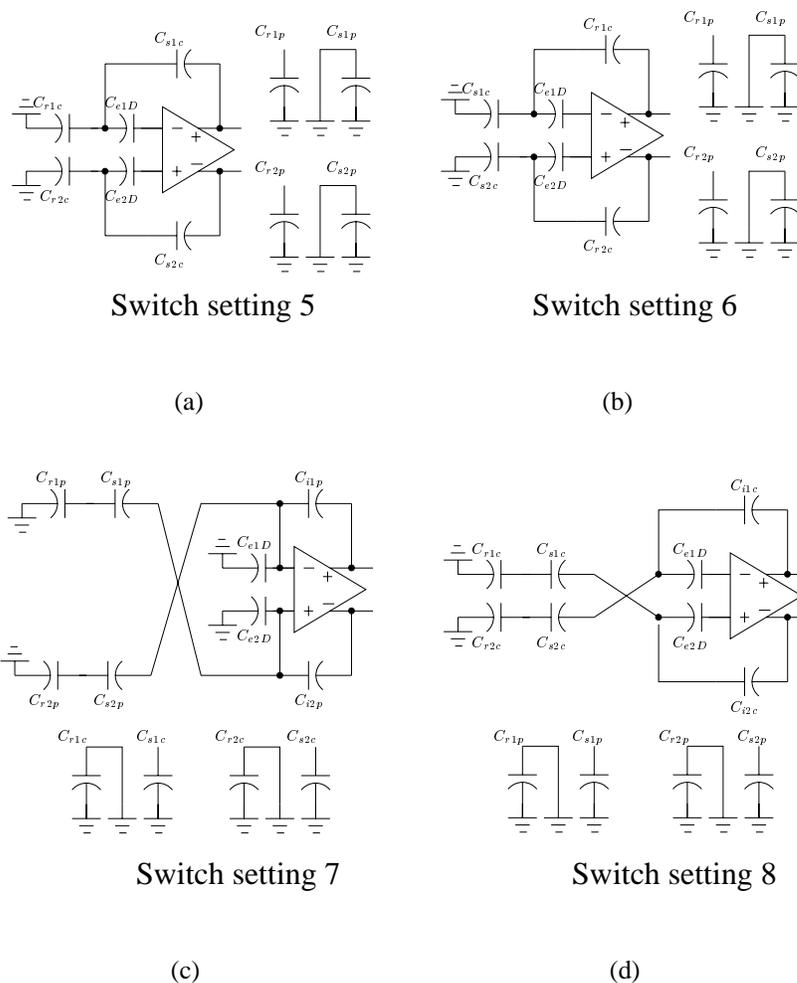


FIGURE 2.4: Circuits of switch setting 5 through switch setting 8

Each conversion starts with the sampling of input signal, which stores the input signal v_{in} in integrating capacitor C_{int} by charge of $C_{int}v_{in}$. For purpose of comparison with reference charge, sampling charge $C_{int}v_{in}$ can be stored as its opposite value $-C_{int}v_{in}$ conveniently through cross coupling of the differential branches. This sampling process is implemented by the two switch configurations (switch setting 1 and

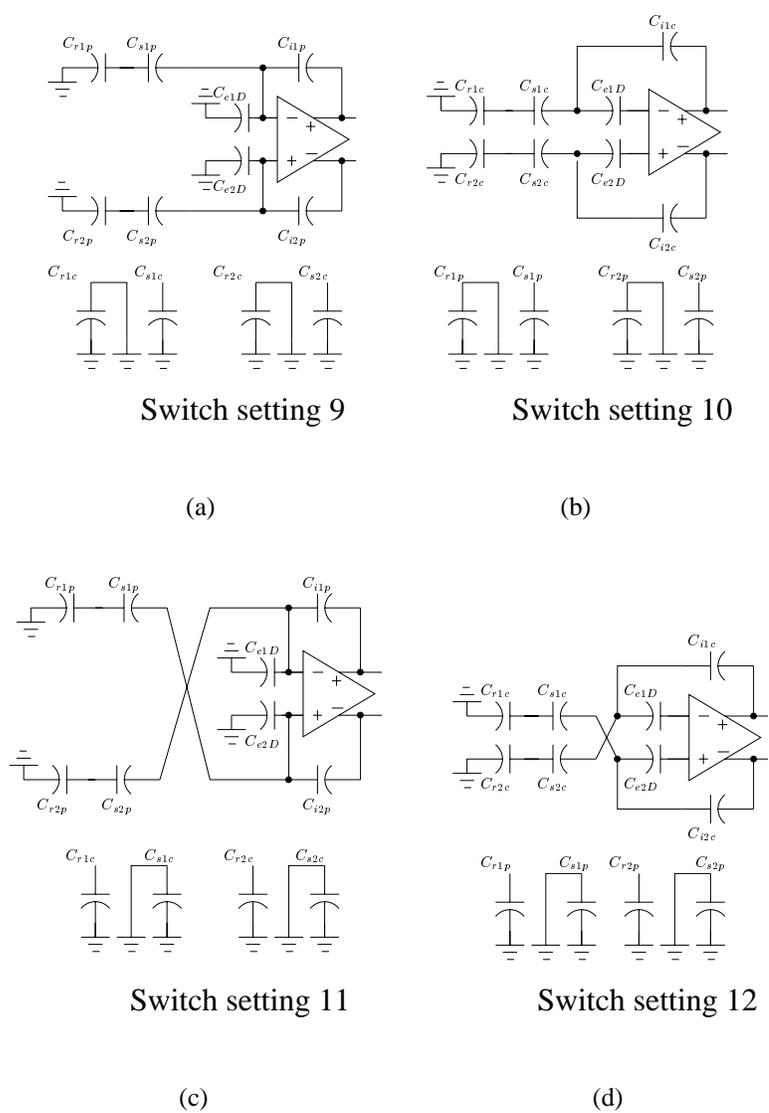


FIGURE 2.5: Circuits of switch setting 9 through switch setting 12

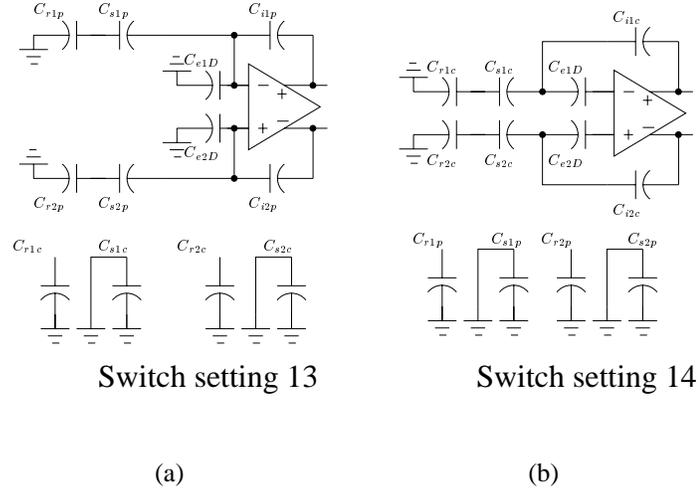


FIGURE 2.6: Circuits of switch setting 13 and switch setting 14

switch setting 2) in Fig. 2.3. Then the normal conversion cycle will be implemented by adding positive (ADD) or negative (SUB) reference charge to the integrating capacitor according to the value of previous bit resulting from last comparison.

As discussed in [25], the addition of reference charge to the integrating capacitor should follow the principle of “the Same Charge Path Flow” to suppress the additional error due to top plate parasitic capacitance mismatches. In actual implementation, this could be realized by the arrangement that any charge flow towards integrating capacitor C_{int} should be from signal capacitor C_{sig} , which means that when sharing the reference charge between reference capacitor C_{ref} and signal capacitor C_{sig} the bottom plate of C_{sig} should always be connected to virtual ground, therefore the charge dumped into C_{int} is always from C_{sig} . In order to suppress the error due to bottom plate parasitic capacitance, it is also necessary to connect the bottom plate of C_{sig} to analog ground before sharing reference charge with C_{ref} and dumping charge into C_{int} . Because of the 2-phase feature of CDS technique, the above additional

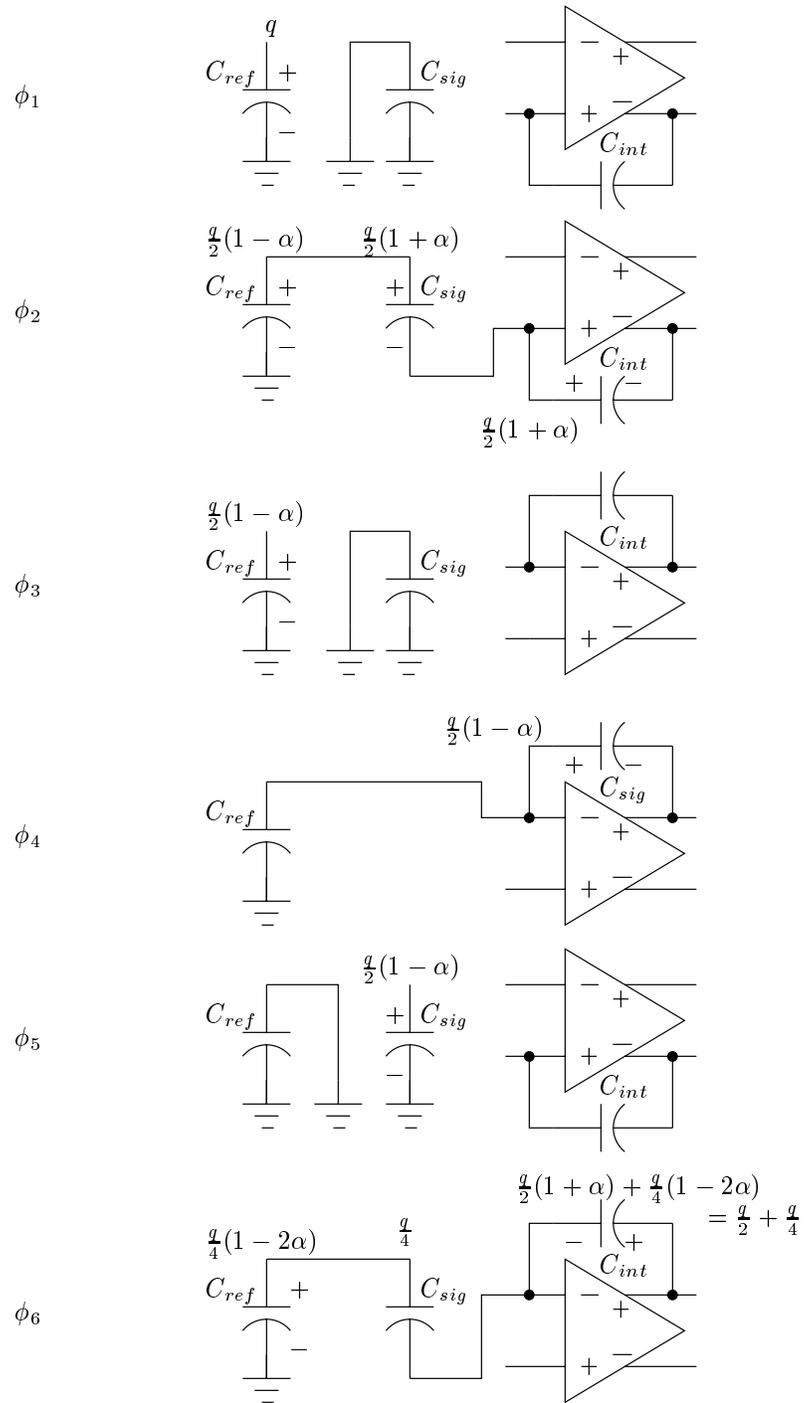


FIGURE 2.7: Mismatch error cancellation for ADD/ADD operation

treatment can be imbedded into normal operations without increasing clock phases.

First order mismatch error cancellation is briefly described as follows. Assume that the mismatch coefficient between reference capacitor C_{ref} and signal capacitor C_{sig} is defined as $\alpha = \frac{C_{sig}-C_{ref}}{C_{sig}+C_{ref}}$ (alternatively $\frac{C_{sig}}{C_{ref}} = \frac{1+\alpha}{1-\alpha}$), and two consecutive charge dumping (into C_{int}) is an ADD/ADD sequence. Further more, the initial error-free reference charge is assumed to be on C_{ref} . Then Fig. 2.7 will be the switch setting sequence for these two bits' conversion. After predictive phase ϕ_1 , the higher bit is obtained by conversion phase ϕ_2 . As it can be seen, this bit has a first order error $\frac{\alpha}{2}q$, which exists both on the reference capacitor C_{ref} and integrating capacitor C_{int} . By virtue of the differential structure, it is possible to manipulate these two error charge and let them cancel each other at the next bit, as shown from phase ϕ_3 through ϕ_6 in fig. 2.7. The purpose of ϕ_3 and ϕ_4 is to swap the reference charge from C_{ref} to C_{sig} , which is necessary to guarantee the principle of “the Same Charge Path Flow” for the low bit conversion in phase ϕ_6 . Obviously, conversion of the low bit in phase ϕ_6 is error free if only the first order mismatch error is concerned. Other possible operation combinations ADD/SUB, SUB/ADD and SUB/SUB have the same mismatch error cancellation fashion: the higher bit has the first order mismatch error while the lower bit is error free. Thus the accumulation of mismatch error during the whole conversion cycle is effectively suppressed. This was clearly demonstrated in Figure 4 of [27], where 24 circuit configuration table were proposed for the complete conversion of any input signal, since there are 4 possible operation sequences (ADD/ADD, ADD/SUB, SUB/ADD and SUB/SUB) and each sequence requires 6 phases.

2.4 Improvement of Mismatch Error Cancellation Algorithm

Further examination of the above discussion reveals that an approximation has been made in the mismatch error cancellation algorithm represented by the 24 circuit configuration table in [27]: the initial error charge of each sequence (consisting of 6 clock phases) is assumed to be always on the signal capacitor (C_2 in [27], which corresponds to 4 C_{sig} — C_{s1p} , C_{s1c} , C_{s2p} and C_{s2c} — in Fig. 2.2), so the signal capacitor C_{sig} is discharged at the beginning of each sequence, while the charge on reference capacitor C_{ref} is kept.

However, detailed charge domain analysis shows that the error charge at the beginning of each sequence could be either on the signal capacitor C_{sig} or on the reference capacitor C_{ref} . Specifically, if the initial error charge is on the signal capacitor C_{sig} (or reference capacitor C_{ref}), then after ADD/SUB or SUB/ADD operations, the error charge will still be on C_{sig} (or C_{ref}) for the next 6-phase sequence, but after ADD/ADD or SUB/SUB operations, the error charge will be on C_{ref} (or C_{sig}) for the next sequence. If the error charge capacitor is not tracked and the charge on C_{ref} is always kept regardless of the type of the last sequence, this error charge on C_{ref} accumulates during the rest operations of each sample. This means that for higher linearity requirement the above approximation could be improved by tracking the error charge capacitor at the beginning of each 6 clock phase operation. This improvement will extend the Table in Figure 4 of [27] from 24 switch configurations to the number of 48 – as

mentioned before, among them only 14 switch configurations are different from each other. Charge domain analysis are shown in Table 2.1 through Table 2.4. Each Table contains two columns: configurations in the left column apply if the error free charge is initially on C_{ref} , while configurations in the right column are to be used in the

TABLE 2.1: ADD/ADD Sequence

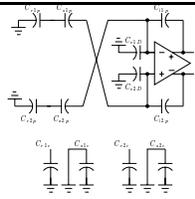
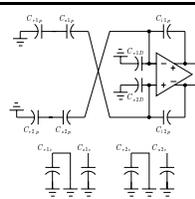
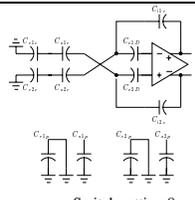
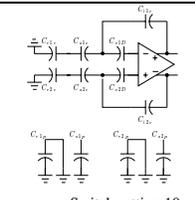
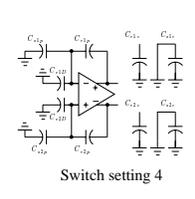
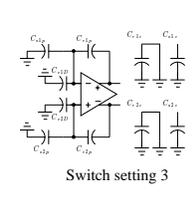
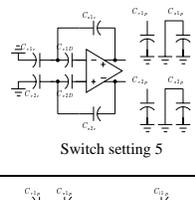
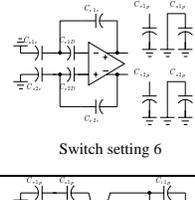
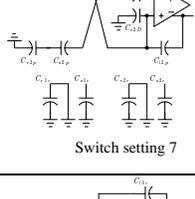
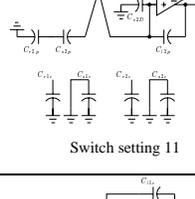
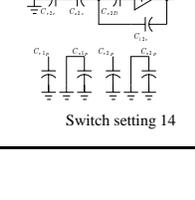
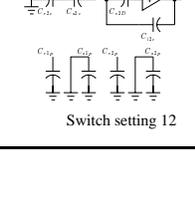
	ADD/ADD(R)	Charge	ADD/ADD (S)	Charge
ϕ_1	 <p>Switch setting 11</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1-\beta}{2}q & \frac{1+\beta}{2}q & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ q & 0 & 0 \end{matrix}$	 <p>Switch setting 7</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1-\beta}{2}q & \frac{1+\beta}{2}q & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & q & 0 \end{matrix}$
ϕ_2	 <p>Switch setting 8</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ 0 & \frac{1+\beta}{2}q & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-\alpha}{2}q & \frac{1+\alpha}{2}q & \frac{1+\alpha}{2}q \end{matrix}$	 <p>Switch setting 10</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ 0 & \frac{1+\beta}{2}q & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-\alpha}{2}q & \frac{1+\alpha}{2}q & \frac{1-\alpha}{2}q \end{matrix}$
ϕ_3	 <p>Switch setting 4</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-\alpha}{2}q & 0 & \frac{1+\alpha}{2}q \end{matrix}$	 <p>Switch setting 3</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & \frac{1+\alpha}{2}q & \frac{1-\alpha}{2}q \end{matrix}$
ϕ_4	 <p>Switch setting 5</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & \frac{1-\alpha}{2}q & \frac{1+\alpha}{2}q \end{matrix}$	 <p>Switch setting 6</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & \frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1+\alpha}{2}q & 0 & \frac{1-\alpha}{2}q \end{matrix}$
ϕ_5	 <p>Switch setting 7</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & \frac{1+2\beta}{4}q & \frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & \frac{1-\alpha}{2}q & \frac{1+\alpha}{2}q \end{matrix}$	 <p>Switch setting 11</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & \frac{1+2\beta}{4}q & \frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1+\alpha}{2}q & 0 & \frac{1-\alpha}{2}q \end{matrix}$
ϕ_6	 <p>Switch setting 14</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & 0 & \frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-2\alpha}{4}q & \frac{1}{4}q & \frac{3}{4}q \end{matrix}$	 <p>Switch setting 12</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & 0 & \frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1}{4}q & \frac{1+2\alpha}{4}q & \frac{3}{4}q \end{matrix}$

TABLE 2.2: ADD/SUB Sequence

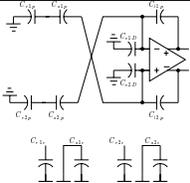
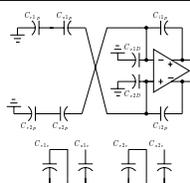
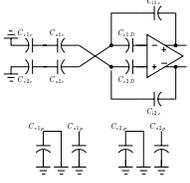
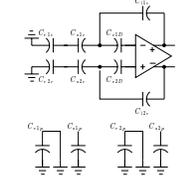
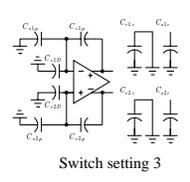
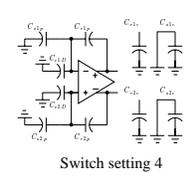
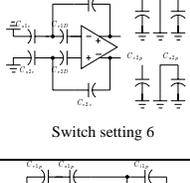
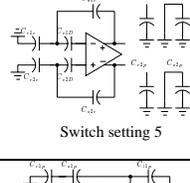
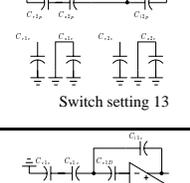
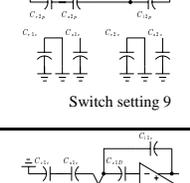
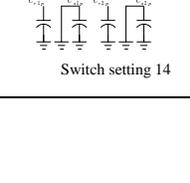
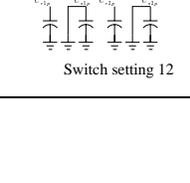
	ADD/SUB(R)	Charge	ADD/SUB (S)	Charge
ϕ_1	 <p>Switch setting 11</p>	C_{rp} C_{sp} C_{ip} $\frac{1-\beta}{2}q$ $\frac{1+\beta}{2}q$ $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} q 0 0	 <p>Switch setting 7</p>	C_{rp} C_{sp} C_{ip} $\frac{1-\beta}{2}q$ $\frac{1+\beta}{2}q$ $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} 0 q 0
ϕ_2	 <p>Switch setting 8</p>	C_{rp} C_{sp} C_{ip} 0 $\frac{1+\beta}{2}q$ $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} $\frac{1-\alpha}{2}q$ $\frac{1+\alpha}{2}q$ $\frac{1+\alpha}{2}q$	 <p>Switch setting 10</p>	C_{rp} C_{sp} C_{ip} 0 $\frac{1+\beta}{2}q$ $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} $\frac{1-\alpha}{2}q$ $\frac{1+\alpha}{2}q$ $\frac{1-\alpha}{2}q$
ϕ_3	 <p>Switch setting 3</p>	C_{rp} C_{sp} C_{ip} $\frac{1+\beta}{2}q$ 0 $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} 0 $\frac{1+\alpha}{2}q$ $\frac{1+\alpha}{2}q$	 <p>Switch setting 4</p>	C_{rp} C_{sp} C_{ip} $\frac{1+\beta}{2}q$ 0 $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} $\frac{1-\alpha}{2}q$ 0 $\frac{1-\alpha}{2}q$
ϕ_4	 <p>Switch setting 6</p>	C_{rp} C_{sp} C_{ip} $\frac{1+\beta}{2}q$ 0 $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} $\frac{1+\alpha}{2}q$ 0 $\frac{1+\alpha}{2}q$	 <p>Switch setting 5</p>	C_{rp} C_{sp} C_{ip} $\frac{1+\beta}{2}q$ 0 $\frac{1+\beta}{2}q$ C_{rc} C_{sc} C_{ic} 0 $\frac{1-\alpha}{2}q$ $\frac{1-\alpha}{2}q$
ϕ_5	 <p>Switch setting 13</p>	C_{rp} C_{sp} C_{ip} $\frac{1}{4}q$ $\frac{1+2\beta}{4}q$ $\frac{1}{4}q$ C_{rc} C_{sc} C_{ic} $\frac{1+\alpha}{2}q$ 0 $\frac{1+\alpha}{2}q$	 <p>Switch setting 9</p>	C_{rp} C_{sp} C_{ip} $\frac{1}{4}q$ $\frac{1+2\beta}{4}q$ $\frac{1}{4}q$ C_{rc} C_{sc} C_{ic} 0 $\frac{1-\alpha}{2}q$ $\frac{1-\alpha}{2}q$
ϕ_6	 <p>Switch setting 14</p>	C_{rp} C_{sp} C_{ip} $\frac{1}{4}q$ 0 $\frac{1}{4}q$ C_{rc} C_{sc} C_{ic} $\frac{1}{4}q$ $\frac{1+2\alpha}{4}q$ $\frac{1}{4}q$	 <p>Switch setting 12</p>	C_{rp} C_{sp} C_{ip} $\frac{1}{4}q$ 0 $\frac{1}{4}q$ C_{rc} C_{sc} C_{ic} $\frac{1-\alpha}{4}q$ $\frac{1}{4}q$ $\frac{1}{4}q$

TABLE 2.3: SUB/ADD Sequence

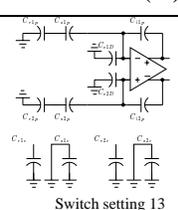
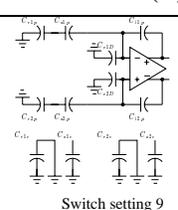
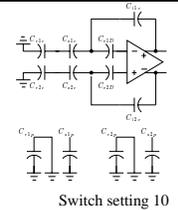
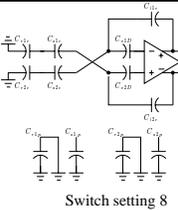
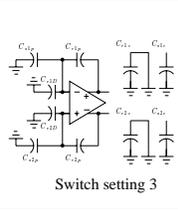
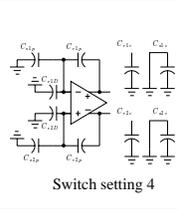
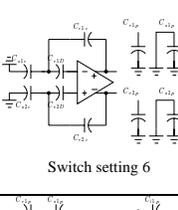
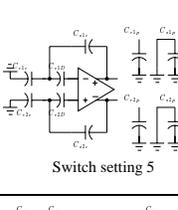
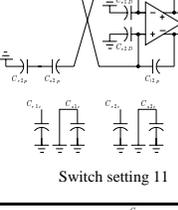
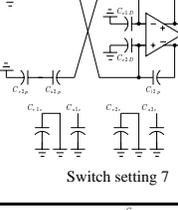
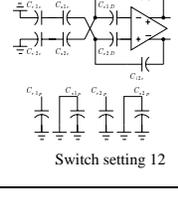
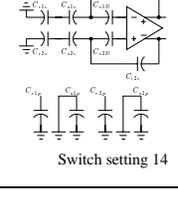
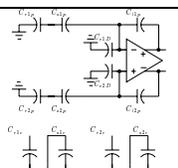
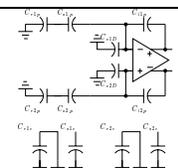
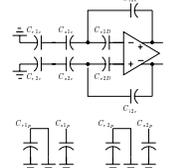
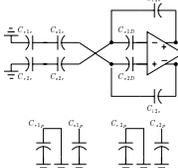
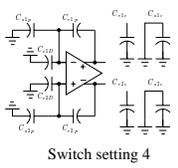
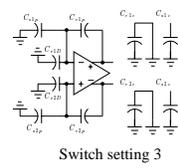
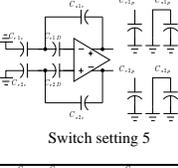
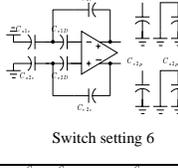
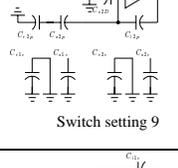
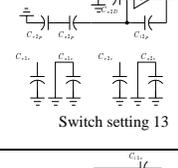
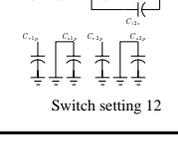
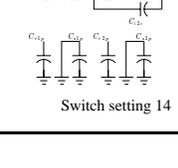
	SUB/ADD(R)	Charge	SUB/ADD (S)	Charge
ϕ_1	 <p>Switch setting 13</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1-\beta}{2}q \quad \frac{1+\beta}{2}q \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $q \quad 0 \quad 0$	 <p>Switch setting 9</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1-\beta}{2}q \quad \frac{1+\beta}{2}q \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $0 \quad q \quad 0$
ϕ_2	 <p>Switch setting 10</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $0 \quad \frac{1+\beta}{2}q \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $\frac{1-\alpha}{2}q \quad \frac{1+\alpha}{2}q \quad -\frac{1+\alpha}{2}q$	 <p>Switch setting 8</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $0 \quad \frac{1+\beta}{2}q \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $\frac{1-\alpha}{2}q \quad \frac{1+\alpha}{2}q \quad -\frac{1+\alpha}{2}q$
ϕ_3	 <p>Switch setting 3</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1+\beta}{2}q \quad 0 \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $0 \quad \frac{1+\alpha}{2}q \quad -\frac{1+\alpha}{2}q$	 <p>Switch setting 4</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1+\beta}{2}q \quad 0 \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $\frac{1-\alpha}{2}q \quad 0 \quad -\frac{1-\alpha}{2}q$
ϕ_4	 <p>Switch setting 6</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1+\beta}{2}q \quad 0 \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $\frac{1+\alpha}{2}q \quad 0 \quad -\frac{1+\alpha}{2}q$	 <p>Switch setting 5</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1+\beta}{2}q \quad 0 \quad -\frac{1+\beta}{2}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $0 \quad \frac{1-\alpha}{2}q \quad -\frac{1-\alpha}{2}q$
ϕ_5	 <p>Switch setting 11</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1}{4}q \quad \frac{1+2\beta}{4}q \quad -\frac{1}{4}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $\frac{1+\alpha}{2}q \quad 0 \quad -\frac{1+\alpha}{2}q$	 <p>Switch setting 7</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1}{4}q \quad \frac{1+2\beta}{4}q \quad -\frac{1}{4}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $0 \quad \frac{1-\alpha}{2}q \quad -\frac{1-\alpha}{2}q$
ϕ_6	 <p>Switch setting 12</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1}{4}q \quad 0 \quad -\frac{1}{4}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $\frac{1}{4}q \quad \frac{1+2\alpha}{4}q \quad -\frac{1}{4}q$	 <p>Switch setting 14</p>	$C_{rp} \quad C_{sp} \quad C_{ip}$ $\frac{1}{4}q \quad 0 \quad -\frac{1}{4}q$ $C_{rc} \quad C_{sc} \quad C_{ic}$ $\frac{1-2\alpha}{4}q \quad \frac{1}{4}q \quad -\frac{1}{4}q$

TABLE 2.4: SUB/SUB Sequence

	SUB/SUB(R)	Charge	SUB/SUB (S)	Charge
ϕ_1	 <p>Switch setting 13</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1-\beta}{2}q & \frac{1+\beta}{2}q & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ q & 0 & 0 \end{matrix}$	 <p>Switch setting 9</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1-\beta}{2}q & \frac{1+\beta}{2}q & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & q & 0 \end{matrix}$
ϕ_2	 <p>Switch setting 10</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ 0 & \frac{1+\beta}{2}q & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-\alpha}{2}q & \frac{1+\alpha}{2}q & -\frac{1+\alpha}{2}q \end{matrix}$	 <p>Switch setting 8</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ 0 & \frac{1+\beta}{2}q & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-\alpha}{2}q & \frac{1+\alpha}{2}q & -\frac{1-\alpha}{2}q \end{matrix}$
ϕ_3	 <p>Switch setting 4</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-\alpha}{2}q & 0 & -\frac{1-\alpha}{2}q \end{matrix}$	 <p>Switch setting 3</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & \frac{1-\alpha}{2}q & -\frac{1-\alpha}{2}q \end{matrix}$
ϕ_4	 <p>Switch setting 5</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & \frac{1-\alpha}{2}q & -\frac{1+\alpha}{2}q \end{matrix}$	 <p>Switch setting 6</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1+\beta}{2}q & 0 & -\frac{1+\beta}{2}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1+\alpha}{2}q & 0 & -\frac{1-\alpha}{2}q \end{matrix}$
ϕ_5	 <p>Switch setting 9</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & \frac{1+2\beta}{4}q & -\frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ 0 & \frac{1-\alpha}{2}q & -\frac{1+\alpha}{2}q \end{matrix}$	 <p>Switch setting 13</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & \frac{1+2\beta}{4}q & -\frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1+\alpha}{2}q & 0 & -\frac{1-\alpha}{2}q \end{matrix}$
ϕ_6	 <p>Switch setting 12</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & 0 & -\frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1-2\alpha}{4}q & \frac{1}{4}q & -\frac{3}{4}q \end{matrix}$	 <p>Switch setting 14</p>	$\begin{matrix} C_{rp} & C_{sp} & C_{ip} \\ \frac{1}{4}q & 0 & -\frac{3+4\beta}{4}q \\ \\ C_{rc} & C_{sc} & C_{ic} \\ \frac{1}{4}q & \frac{1+2\alpha}{4}q & -\frac{3}{4}q \end{matrix}$

sequence if the error free charge is initially on C_{sig} . Notice that in these tables two mismatch coefficients have been used: α is for conversion phase related capacitors and β is for prediction phase related capacitors.

Chapter 3

Predictive Correlated Triple Sampling (CTS)

3.1 Introduction

As discussed in chapter 2, circuit non-idealities exist in any switched capacitor circuit, such as op-amp finite gain and offset voltage, parasitic capacitances, signal dependent charge injection, and nonlinear charge/voltage characteristics of the capacitors, etc. These circuit non-idealities cause nonlinear distortions in the performance of switched capacitor circuits. Since a low voltage switched capacitor SAR - ADC is to be designed in this thesis and it is difficult to obtain very high op-amp gain in the normal signal range, finite gain and offset voltage must be of concern.

The correlated double sampling (CDS) technique [2, 4, 5, 7, 12, 21, 22, 24] is well known and widely used in switched capacitor circuits, such as SC S/H and delay stages, integrators, equalizers and amplifiers. It is proved that this technique can be used in switched capacitor circuit to effectively suppress nonlinear distortions thus the technique has been imbedded into the design of the switched capacitor SAR – ADC in this thesis. The essence of predictive CDS adopted into the design described in chapter 2 is that during the predictive phase, voltage deviation of virtual ground due to finite gain and offset voltage from analog ground is stored in error capacitor C_{err} , and in the conversion phase this error charge will be kept and bring the “pivot” of charge transfer between signal capacitor C_{sig} and integrating capacitor C_{int} to a voltage value closer to the analog ground, or the charge transfer “pivot” exhibits less

voltage deviation from analog ground than op-amp virtual ground does, which ensures more ideal charge transfer between C_{sig} and C_{int} hence less distortion after the signal passes the designed SC stage. There is a subtle difference between the applications of CDS in the above mentioned SC circuits and in successive approximation ADC. For the normal applications of CDS in SC circuits such as S/H and integrator stages, signal passes the designed SC stage once, higher order errors after CDS compensation is negligible compared to the magnitude of processed signal itself. But in case of SAR – ADC, the processed signal is the reference voltage that passes the designed integrating stage (behaves as an internal DAC) repeatedly, any small error after normal CDS compensation will be accumulated and amplified (according to the capacitance ratio) N times (number of bits generated by the ADC). On the other hand, the processed signal itself (the reference voltage) is halved each time it passes the integrating stage, therefore the error left over after CDS compensation in SAR – ADC may not be negligible compared to the processed signal and causes significant nonlinear distortions.

This chapter starts from the theoretical analysis of the operation of the designed switched capacitor SAR – ADC described in chapter 2 and shows that the normal predictive CDS is not good enough for high resolution SAR – ADCs. Then an improvement of the predictive CDS is proposed based on the operation of normal predictive CDS. SWITCAP simulations of the SAR – ADC given in chapter 2 are performed to verify this improvement. This new version of the predictive CDS technique – “

predictive Correlated Triple Sampling (CTS) technique” – which is proposed and verified in this chapter, is used in the final design discussed in chapter 4.

3.2 Theoretical Analysis of The Switched Capacitor SAR – ADC

The predictive CDS technique in the switched capacitor SAR – ADC will be explored in this section under the condition that the only circuit non-idealities are from op-amp finite gain and offset voltage, while all capacitors have the same value. Data conversion follows the same switch sequences described in chapter 2, except that the charge swap procedures (ϕ_3 and ϕ_4) between high bit and low bit conversion are omitted. As mentioned in chapter 2, ϕ_3 and ϕ_4 transfer charge either from signal capacitor C_{sig} to the reference capacitor C_{ref} or vice versa to guarantee the “same path charge flow” principle. Obviously this charge transfer is not complete because of voltage deviation of op-amp virtual ground from analog ground. Since it is difficult to mathematically track the direction of charge transfer, this analysis simply assumes that this charge transfer is complete and exactly the same amount of reference charge will be used in the following low bit conversion. However, even with this somewhat ideal implementation, observable nonlinear distortion still appears.

3.2.1 Initial Charges Introduced by Sampling

The sampling of the signal is performed by two switch settings (prediction phase and actual sampling phase) demonstrated in Fig. 3.1. These two steps bring signal charge into integrating capacitor C_i and reference charge into reference capacitor C_r . Notice that the second subscript ‘ p ’ or ‘ c ’ for capacitors is used to denote prediction phase and conversion phase. Obviously the error capacitor C_e will be charged during prediction phase ϕ_1 because of op-amp finite gain and offset voltage. Equations

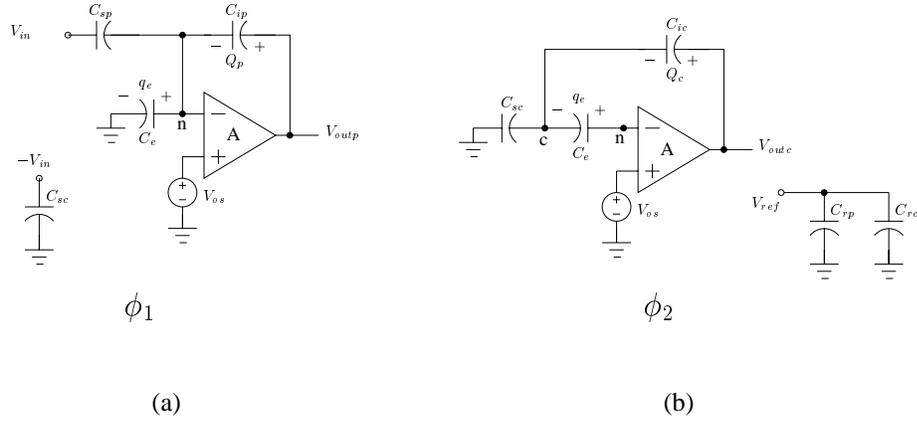


FIGURE 3.1: Demonstration of input signal sampling

necessary to describe the sampling phase ϕ_1 are:

$$A(v_{os} - v_n) = v_{outp} \quad (3.1)$$

$$C_e v_n + C_{sp}(v_n - v_{in}) + C_{ip}(v_n - v_{outp}) = 0 \quad (3.2)$$

Solving the above two equations and using notation $\mu = 1/A$, it is found that

$$v_{outp} = -\frac{C_{sp}v_{in}}{C_{ip} + \mu(C_e + C_{sp} + C_{ip})} + \frac{(C_e + C_{sp} + C_{ip})v_{os}}{C_{ip} + \mu(C_e + C_{sp} + C_{ip})} \quad (3.3)$$

with the assumption $C_{sp} = C_{ip} = C_e = C$,

$$v_{outp} = \frac{-v_{in} + 3v_{os}}{1 + 3\mu} \quad (3.4)$$

and

$$v_n = v_{os} - \mu v_{outp} = \frac{v_{os} + \mu v_{in}}{1 + 3\mu} \quad (3.5)$$

which gives the error charge q_e on C_e caused by op-amp finite gain and offset voltage, and charge Q_p on integrating capacitor C_{ip}

$$q_e = C_e v_n = \frac{C(v_{os} + \mu v_{in})}{1 + 3\mu} \quad (3.6)$$

$$Q_p = C(v_{outp} - v_n) = \frac{C[2v_{os} - (1 + \mu)v_{in}]}{1 + 3\mu} \quad (3.7)$$

The error charge q_e on C_e will remain unchanged during sampling phase ϕ_2 .

Equations necessary to describe the sampling phase ϕ_2 are:

$$A[v_{os} - (v_c + q_e/C_e)] = v_{outc} \quad (3.8)$$

$$C_{sc}v_c + C_{ic}(v_c - v_{outc}) = C_{sc}v_{in} \quad (3.9)$$

Solving the above two equations (with the assumption $C_{sc} = C_{ic} = C_e = C$), it is found that

$$v_{outc} = \frac{-(1 + 5\mu)v_{in} + 6\mu v_{os}}{(1 + 2\mu)(1 + 3\mu)} \quad (3.10)$$

$$v_c = \frac{3\mu(\mu v_{in} + v_{os})}{(1 + 2\mu)(1 + 3\mu)} \quad (3.11)$$

which gives

$$Q_c = C(v_{outc} - v_c) = \frac{C[3\mu v_{os} - (1 + 5\mu + 3\mu^2)v_{in}]}{(1 + 2\mu)(1 + 3\mu)} \quad (3.12)$$

During sampling phase ϕ_2 , reference capacitors C_{rp} and C_{rc} are charged with reference voltage v_{ref} , which give the initial reference charge

$$q_p = C_{rp}v_{ref} \quad (3.13)$$

$$q_c = C_{rc}v_{ref} \quad (3.14)$$

Eq. 3.6, Eq. 3.7, Eq. 3.12, Eq. 3.13 and Eq. 3.14 provide the initial charges in the circuit for the rest of converting cycles of signal v_{in} . At the same time, the polarity of v_{outc} calculated by Eq. 3.10 determines the MSB:

$$b_1 = \begin{cases} 1 & \text{if } v_{outc} > 0 \\ 0 & \text{otherwise} \end{cases}$$

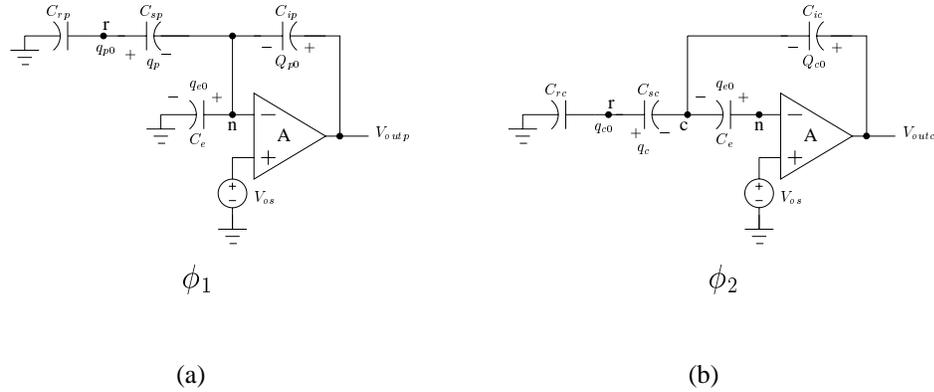


FIGURE 3.2: Demonstration of normal converting cycles

3.2.2 Charge Domain Analysis of Normal Converting Cycles

With all necessary initial charges in hand, it is possible now to proceed with the charge domain analysis of the normal converting cycles. Since all converting cycles repeat the same switch sequence (again for mathematical simplicity two charge swap phases ϕ_3 and ϕ_4 of actual implementation in chapter 2 are ignored, as explained in the last section), it is proper to deal with this problem in an iteration manner. The following analysis assumes that for the i th bit cycle, error charge q_{e0} , reference charges q_{p0} and q_{c0} , integrating charges Q_{p0} and Q_{c0} are left over by the $i - 1$ bit cycle. Circuit configurations of both ϕ_1 and ϕ_2 for normal converting cycles are illustrated in Fig. 3.2.

It is worth mentioning that Fig. 3.2 is sufficient to represent both cases of direct coupling and cross coupling in a differential structure described in chapter 2, where the manner of coupling varies with ADD or SUB operations. Notice that Fig. 3.2 agrees with the direct coupling configuration of [27], which corresponds to a SUB operation. Mathematical treatment in this analysis for cross coupling is described

as following: (1) When the new reference charges q_p and q_c are to be calculated for cross coupling configuration, it is necessary to flip the signs of the initial error charge q_{e0} , integrating charges Q_{p0} and Q_{c0} , while the signs of initial reference charges q_p and q_{c0} remain unchanged; (2) with the new error charge q_e , integrating charges Q_p and Q_c are calculated, and the signs of q_{p0} and q_{c0} should be flipped, while the signs of q_{e0} , Q_{p0} and Q_{c0} remain unchanged.

Equations necessary to describe predicting phase ϕ_1 are:

$$A(v_{os} - v_n) = v_{outp} \quad (3.15)$$

$$C_e v_n + C_{ip}(v_n - v_{outp}) + C_{sp}(v_n - v_r) = q_{e0} + (-Q_{p0}) \quad (3.16)$$

$$C_{rp}v_r + C_{sp}(v_r - v_n) = q_{p0} \quad (3.17)$$

Solving the above three equations, using notation $\mu = 1/A$ and assuming $C_{sp} = C_{ip} = C_e = C$, it is found that

$$v_{outp} = \frac{5v_{os} + 2\frac{Q_{p0}-q_{e0}}{C} - (-1)^{b_{i-1}+1}\frac{q_{p0}}{C}}{2 + 5\mu} \quad (3.18)$$

$$v_n = \frac{2v_{os} + 2\mu\frac{q_{e0}-Q_{p0}}{C} + (-1)^{b_{i-1}+1}\mu\frac{q_{p0}}{C}}{2 + 5\mu} \quad (3.19)$$

which gives

$$q_e = C_e v_n = \frac{2[Cv_{os} + \mu(q_{e0} - Q_{p0})] + (-1)^{b_{i-1}+1}\mu q_{p0}}{2 + 5\mu} \quad (3.20)$$

$$q_p = C_{sp}(v_r - v_n) = \frac{-Cv_{os} + (1 + 2\mu)q_{p0} + (-1)^{b_{i-1}+1}\mu(Q_{p0} - q_{e0})}{2 + 5\mu} \quad (3.21)$$

$$Q_p = C(v_{outp} - v_n) = \frac{3Cv_{os} + 2(1 + \mu)(Q_{p0} - q_{e0}) - (-1)^{b_{i-1}+1}(1 + \mu)q_{p0}}{2 + 5\mu} \quad (3.22)$$

Note that in the above derivations a sign factor $(-1)^{b_{i-1}+1}$ has been introduced to take care of the cross coupling circuit configuration when an ADD operation is needed. Here b_{i-1} is the value of $(i - 1)$ th bit, which means that if $b_{i-1} = 1$ a set of SUB operation (direct coupling) formula is obtained, while if $b_{i-1} = 0$ the above formula correspond to an ADD operation (cross coupling). The new error charge q_e on C_e calculated in phase ϕ_1 will remain unchanged during converting phase ϕ_2 .

Equations necessary to describe the converting phase ϕ_2 are:

$$A[v_{os} - (v_c + q_e/C_e)] = v_{outc} \quad (3.23)$$

$$C_{sc}(v_c - v_r) + C_{ic}(v_c - v_{outc}) = -Q_{c0} \quad (3.24)$$

$$C_{rc}v_r + C_{sc}(v_r - v_c) = q_{c0} \quad (3.25)$$

Solving the above three equations (with the assumption $C_{sc} = C_{ic} = C_e = C$) and combining solutions Eq. 3.20 through Eq. 3.22 for converting phase ϕ_1 , it is found that

$$v_{outc} = \frac{15\mu v_{os} + 6\mu \frac{Q_{p0} - q_{e0}}{C} + (4 + 10\mu) \frac{Q_{c0}}{C} - (-1)^{b_{i-1}+1} \frac{3\mu q_{p0} + (2+5\mu)q_{c0}}{C}}{(2 + 3\mu)(2 + 5\mu)} \quad (3.26)$$

$$\begin{aligned} q_c &= C_{sc}(v_r - v_c) \\ &= \frac{-5\mu C v_{os} + (1 + \mu)(2 + 5\mu)q_{c0} + \mu q_{p0}}{(2 + 3\mu)(2 + 5\mu)} \\ &\quad + (-1)^{b_{i-1}+1} \frac{\mu[(2 + 5\mu)Q_{c0} + 2(q_{e0} - Q_{p0})]}{(2 + 3\mu)(2 + 5\mu)} \end{aligned} \quad (3.27)$$

$$\begin{aligned} Q_c &= C_{ic}(v_{outc} - v_c) \\ &= \frac{5\mu C v_{os} + 2\mu(Q_{p0} - q_{e0}) + 2(1 + \mu)(2 + 5\mu)Q_{c0}}{(2 + 3\mu)(2 + 5\mu)} \\ &\quad - (-1)^{b_{i-1}+1} \frac{\mu q_{p0} + (1 + \mu)(2 + 5\mu)q_{c0}}{(2 + 3\mu)(2 + 5\mu)} \end{aligned} \quad (3.28)$$

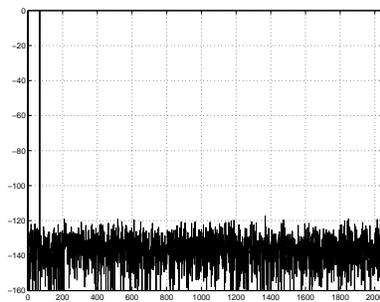
Eq. 3.20, Eq. 3.21, Eq. 3.22, Eq. 3.27 and Eq. 3.28 can be used to calculate the initial charges for the next bit's converting, while Eq. 3.26 is used to determine the digital value of present (i th) bit:

$$b_i = \begin{cases} 1 & \text{if } v_{outc} > 0 \\ 0 & \text{otherwise} \end{cases}$$

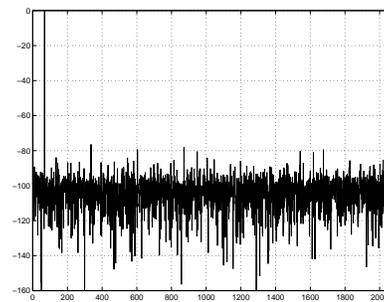
The above formula optimistically describes the charge transportation of the ideal switched capacitor SAR A/D converter described in chapter 2 since the only imperfection is caused by opamp non-ideality and the incomplete charge swap phases ϕ_3 and ϕ_4 are ignored. It is easy to use above formula of such a converter to analyze nonlinear distortions caused only by op-amp finite gain and offset voltage after CDS compensation.

3.2.3 Calculation of Harmonic Distortion after CDS Compensation

The following steps are used to calculate the harmonic distortion:



(a) $A = 2 \times 10^6, v_{os} = 30mV$



(b) $A = 2000, v_{os} = 30mV$

FIGURE 3.3: Harmonic distortion caused by op-amp non-ideality still exists after normal CDS

1. A sample $v_{in}(t)$ is obtained from a sinusoidal signal $\sin(\omega_0 t)$ and is used to calculate initial charges by (3.6), (3.7), (3.12), (3.13) and (3.14). MSB b_1 is determined by the polarity of (3.10).
2. With the value of b_{i-1} and $q_{e0}, q_{p0}, Q_{p0}, q_{c0}$ and Q_{c0} being determined in the last step, new charges q_e, q_p, Q_p, q_c and Q_c are calculated by (3.20), (3.21), (3.22), (3.27) and (3.28) respectively. At the same time, b_i is determined by the polarity of (3.26).
3. Repeat step 2 until all 16 bits are determined.

4. The decimal representation of this sample is calculated from 16-bit digital output.
5. Go to step 1 for the next sample.
6. Repeat above procedure until 4096 samples are converted which contain 67 bins.
7. FFT calculation is performed for these 4096 samples.

The output spectra of this A/D converter with perfectly matched capacitors are depicted in Fig. 3.3.

3.2.4 Discussion and Conclusion

The above theoretical analysis of a switched-capacitor SAR A/D converter with perfectly matched capacitors shows that observable harmonic distortion still exists even when the op-amp finite gain and offset voltage are compensated by the normal CDS technique. This should be reasonable because even CDS technique decreases virtual ground voltage dramatically compared to the case without CDS, the voltage of the virtual ground still exhibits a finite small deviation from the analog ground. Therefore charge transfers across virtual ground can never be complete, which means that the division of reference charge will deviate from the ideal factor 1/2 for each bit. This deviation is negligible for determining the polarity of v_{outc} when integrating charge Q_c is significantly different than zero. However, this deviation, even small for each bit because of CDS compensation, should accumulate as converting continues. On the other hand the integrating charge Q_c approaches zero as the reference charge is being halved for each bit. After a certain number of bits' conversion, the magnitude

of Q_c will be comparable to the accumulated error and the limit of the converting resolution is achieved, hence an error code should appear. Because the time when Q_c approaches zero depends on the magnitude of input signal, the above error code is signal dependent, and appears as harmonic distortion.

3.3 Improvement of Predictive CDS in SC SAR – ADC

The last section reveals that when it is difficult to obtain high gain op-amp, which is true in case of low voltage design, normal predictive CDS compensation is not good enough for the high resolution switched capacitor SAR – ADC. However, this normal predictive CDS technique can be improved with the concept of “Predictive Correlated Triple Sampling (CTS)” in the context of switched capacitor SAR – ADC, and this will be explained next.

As mentioned before, the compensation of predictive CDS to op-amp finite gain and offset voltage happens because the error charge stored on the error capacitor in the predictive phase brings the “pivot” of the charge transfer in converting phase closer to the analog ground, which is clearly illustrated in Fig. 3.2. In the predictive phase ϕ_1 , charge transfer “pivot” from C_{sp} to C_{ip} is op-amp virtual ground “ n ”. Due to op-amp finite gain and offset voltage, voltage of node “ n ” deviates from analog ground and is stored in C_e as error charge. In converting phase ϕ_2 the “pivot” of charge transfer from C_{sc} to C_{ic} is node “ c ”. As this node in ϕ_1 is connected to the analog ground while the voltage of op-amp virtual ground will not change much between ϕ_1 and ϕ_2 and error charge q_{e0} on C_e remains unchanged from ϕ_1 to ϕ_2 , thus

compared to that of node “ n ”, the voltage of node “ c ” is closer to analog ground, which results in less signal distortion.

Having understood the above compensation mechanism, it is possible to extend this mechanism and bring the “pivot” voltage of charge transfer even closer to analog ground, which is illustrated in Fig. 3.4. Here, three phases have been used to realize the improved compensation mechanism. In phase ϕ_1 , capacitor C_{e2} is charged by error charge due to op-amp finite gain and offset voltage. This operation is the same as in the predictive phase of normal predictive CDS except that an additional capacitor C_{e1} is added and discharged. In phase ϕ_2 , node “ c ” is used as the “pivot” of charge transfer from C_s to C_i , and the small voltage deviation of node “ c ” is stored in C_{e1} . In phase ϕ_3 , node “ d ” is used as the “pivot” of charge transfer from C_{sc} to C_{ic} . With error charges on both C_{e1} and C_{e2} , voltage of node “ d ” will be closer to the analog ground than both node “ n ” and node “ c ”. If phase ϕ_3 is used in any critical charge transfer operation while phases ϕ_1 and ϕ_2 are used in any non-critical ones as predictive operations, then this predictive correlated “triple” sampling (CTS) technique can increase circuit linearity significantly.

The above predictive CTS inevitably poses a higher burden of clock consumption to the switched capacitor circuits. Fortunately, in the operation of the successive approximation ADC it is not necessary to use three phases for all operations. LSB is the non-critical bit thus ϕ_1 and ϕ_2 can be used as normal predictive CDS operation to generate this bit. At the same time the error charge on C_{e2} is refreshed and kept for ϕ_2 and ϕ_3 . All bits other than LSB are regarded as critical bits so ϕ_2 and ϕ_3 are used as predictive and converting phases respectively to generate those bits. This arrangement of clock phases will use the same number of clocks as before when normal predictive CDS technique was used, but higher circuit linearity will be obtained, as will be shown in the next section by SWITCAP simulations.

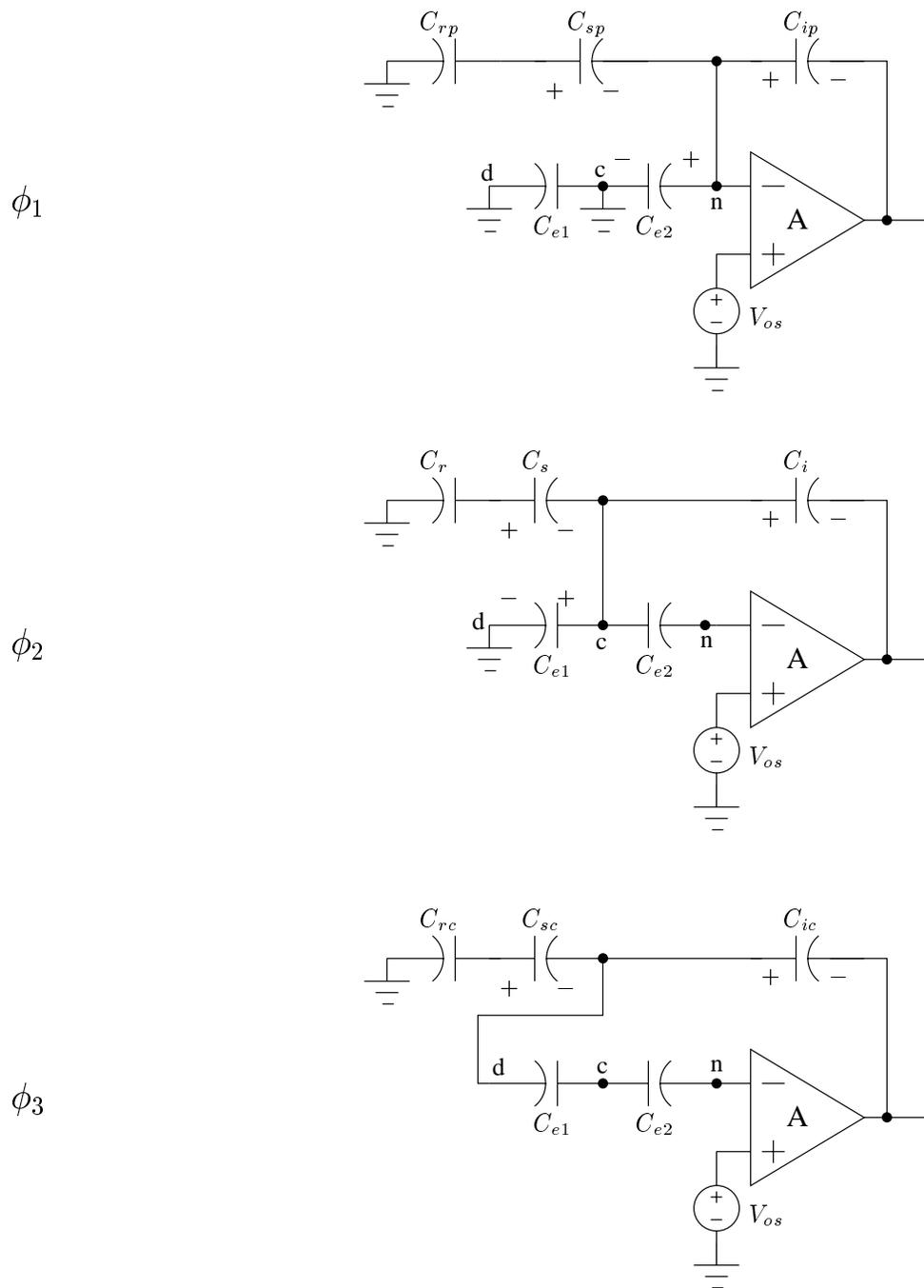


FIGURE 3.4: predictive CTS operation

3.4 Verification of Predictive CTS by SWITCAP Simulations of SAR – ADC

SWITCAP simulations have been performed, which compares the improvement of predictive CTS technique over predictive CDS technique in the operation of SAR – ADC. Fig. 3.5 shows the output spectrum of the SAR – ADC with predictive CDS technique, where op-amp gain is 66dB and offset voltage is 30mV. No capacitance mismatch and parasitic capacitances are included. The same condition is simulated with predictive CTS technique proposed in this chapter, and the result is shown in Fig. 3.6.

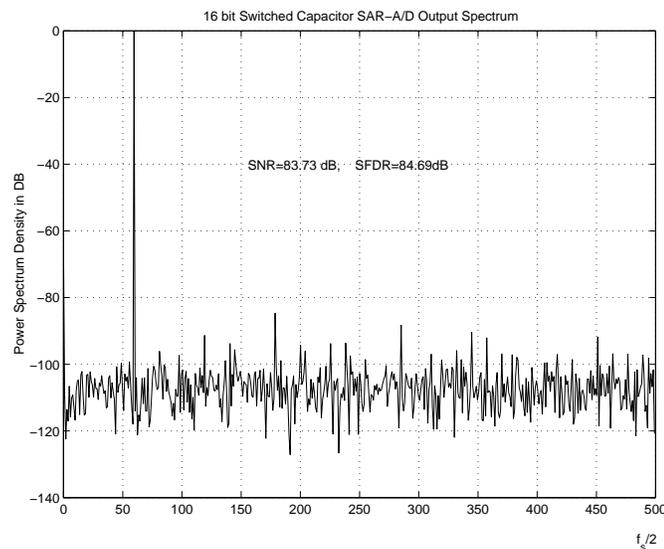


FIGURE 3.5: Output spectrum of a SAR–ADC with predictive CDS, op-amp $A = 66dB$, $V_{os} = 30mV$, no mismatch and parasitic

The improvement of predictive CTS over predictive CDS is obvious: the Signal to Noise Ratio of 84dB is increased to 101 dB, while the Spur Free Dynamic Range

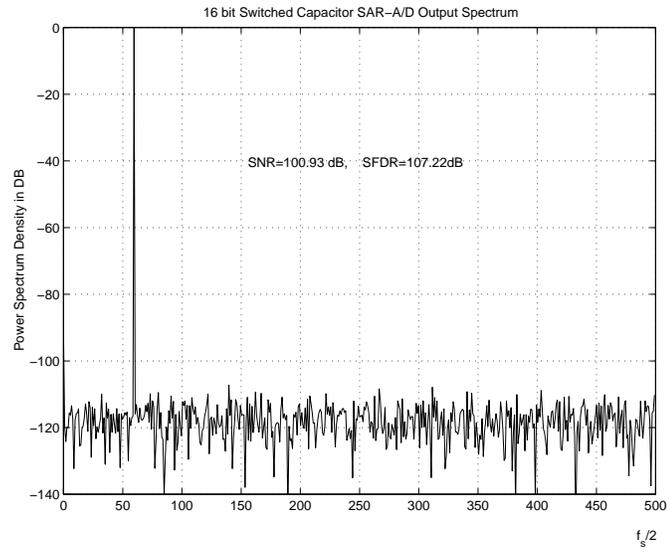


FIGURE 3.6: Output spectrum of a SAR-ADC with predictive CTS, op-amp $A = 66\text{dB}$, $V_{os} = 30\text{mV}$, no mismatch and parasitic

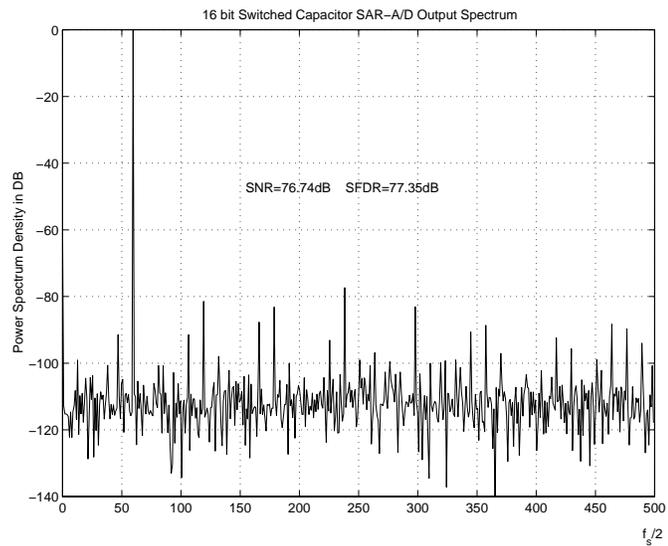


FIGURE 3.7: Output spectrum of a SAR-ADC with predictive CDS. op-amp $A = 66\text{dB}$, $V_{os} = 30\text{mV}$, mismatch and parasitic exist

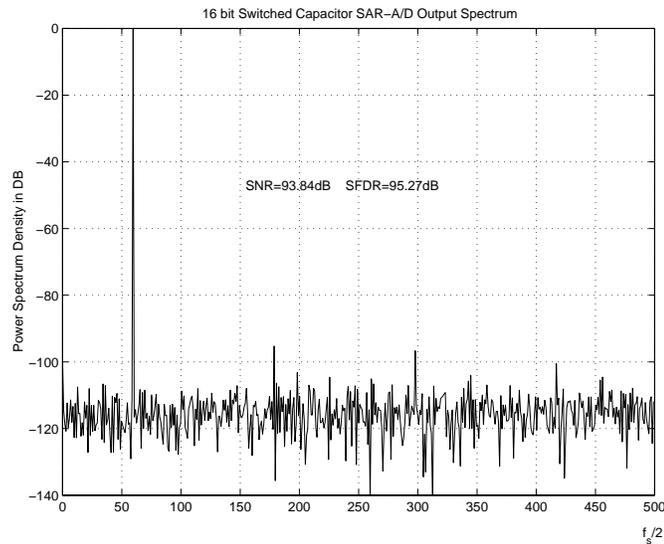


FIGURE 3.8: Output spectrum of a SAR-ADC with predictive CTS. op-amp $A = 66\text{dB}$, $V_{os} = 30\text{mV}$, mismatch and parasitic exist

of 85 dB is increased to 107 dB.

In the actual circuit, there exist capacitance mismatch and parasitic capacitances, so the comparison between predictive CDS and predictive CTS is also performed with SWITCAP simulations under the condition that in addition to op-amp finite gain and offset voltage, randomized capacitance mismatch with 1% 3σ RMS, 20% randomized bottom parasitic and 10% randomized top parasitic are also included in the simulations. As expected, under conditions of capacitance mismatch and parasitic capacitances, predictive CTS operation behaves much better than predictive CDS:

the SNR is increased from 76.7dB in Fig. 3.7 to 93.8dB in Fig. 3.8, and SFDR is increased from 77.4dB in Fig. 3.7 to 95.3dB in Fig. 3.8.

Chapter 4

Design of A 1.8V Switched Capacitor SAR – ADC

4.1 Introduction

In chapter 2 the operating principle and system level circuit configurations of a switched capacitor SAR – ADC were discussed, where the novel capacitance mismatch error cancellation algorithm proposed in [25] and [27] was used with some algorithm improvement. The predictive CDS compensation technique in the proposed SAR – ADC was studied in chapter 3, where the deficiency of normal predictive CDS for low voltage high resolution SC SAR – ADC was revealed and the double predictive CDS was proposed to overcome this deficiency, which was verified by SWITCAP simulations. In this chapter, an actual Switched Capacitor SAR – ADC will be designed with 0.18μ CMOS9 process from National Semiconductor Corporation. This design aims to become the test vehicle for the algorithms and techniques discussed in previous chapters.

4.2 Design Specifications

The fast evolution of modern VLSI benefits from the fact that people are able to steadily scale down device dimensions with advanced process technology. If power supply voltage remains unchanged, the direct impact of reducing device dimension on device physics is the enhanced electric field that is detrimental to device performances. Nevertheless, the trend to develop portable and battery operated electronic

instruments requires low power consumption electronics. Therefore low power supply voltage is a natural choice in modern IC designs to meet above requirements. In this design 1.8V is chosen as the power supply voltage, which is supported by 0.18 μ CMOS9 process of National Semiconductor Corporation.

Another target of this design is high resolution, which is chosen as 95dB of dynamic range. This aim requires very small kT/C noise from switched capacitor circuit and determines the lower limit of capacitors used in the circuit. The peak to peak signal voltage of 1V is used in this design, thus a unit capacitance of 16pF will satisfy this resolution.

The following table summarizes all parameter specifications of this SAR – ADC.

TABLE 4.1: Switched Capacitor SAR ADC Specifications

Parameter	Specification
power supply voltage	1.8V
dynamic range	95 dB
peak to peak input signal swing	1V
input signal bandwidth	0 ~ 20kHz
clock frequency	1.4 MHz
technology	NSC 0.18 μ CMOS9 process

The design of this SAR – ADC consists of two blocks: analog components and

digital control block for switch clocks. These are described in the following sections.

4.3 Analog Component Design

The analog block of this converter includes two parts – ADC core and comparator – as shown in Fig. 2.2 of chapter 2. From this figure, ADC core is the part on the left side of switch S67 and S68, which consists of an op-amp, 14 capacitors with 16pF for each, and 66 switches. As mentioned in chapter 3, in order to perform

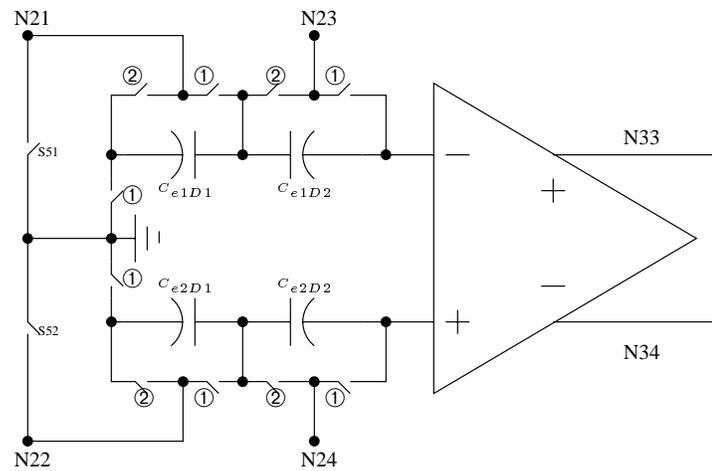


FIGURE 4.1: Modification of circuit from normal predictive CDS to double predictive CDS

double predictive CDS compensation technique, two more error charge capacitors will be added to the ADC core. At the same time, 10 more switches are also needed to carry out the necessary charge transfer operations. All modifications are made between nodes N21 and N23, and between nodes N22 and N24. Fig. 4.1 shows the circuit modification based on Fig. 2.2 of chapter 2. In Fig. 4.1 phase ① is for

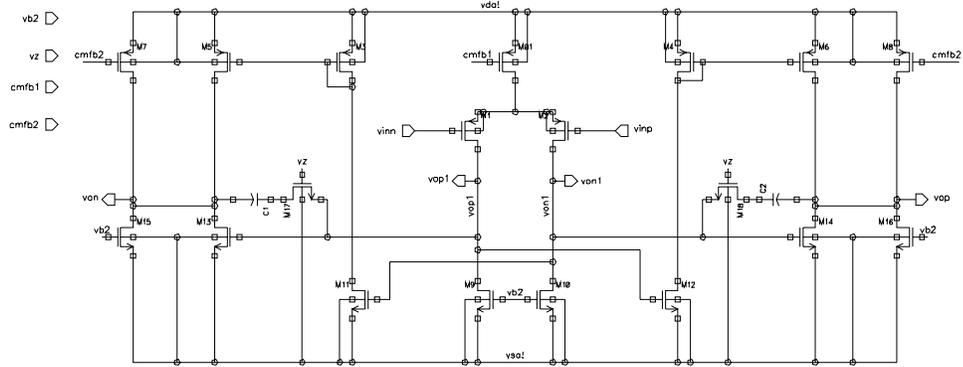


FIGURE 4.3: Two stage class A/AB operational amplifier

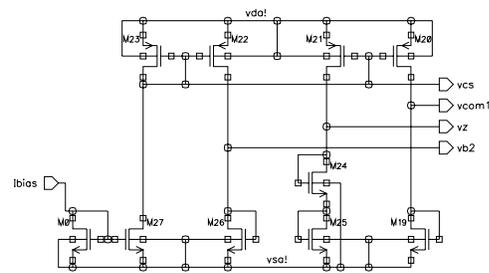


FIGURE 4.4: Bias circuit of the operational amplifier

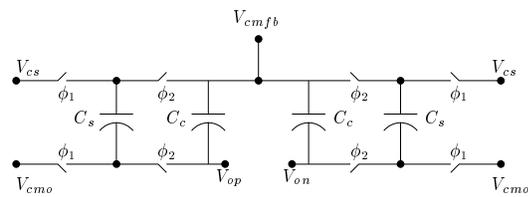


FIGURE 4.5: Switched capacitor common mode feedback circuit

non-dominant pole frequency, the output branch current is only about half of that of a two stage class A structure, therefore it consumes less power than a two stage class A op-amp, this advantage is more obvious in low-speed applications; (2) PSRR is better than two stage class A; (3) it has a larger signal swing compared to the folded cascode topology, and this is critical in low voltage design. Fig. 4.3 shows the detailed structure of this op-amp. Fig. 4.4 is its bias circuit. From Fig. 4.3 it can be seen that bias of the second stage is determined by the output common mode voltage of the first stage. A current mirror is used to ensure the “push and pull” operation for the differential input signal, however, this also cancels the influence of the first stage common mode voltage on the second stage common mode voltage, which means that two separate common mode voltage feedback circuits are needed for two stages. The split of transistors in the output branches is to improve the phase margin of the common mode feedback loop and adjust the output common mode voltage. The switched capacitor common mode feedback circuit is used in both stages of this op-amp and is shown in Fig. 4.5. Capacitances in Fig. 4.5 will affect the phase margin of the op-amp, and they are determined by simulations of 14 switch configurations described in chapter 2. Even the Bode plot varies somewhat from switch setting to switch setting, the

typical one of the op-amp is shown in Fig. 4.6.

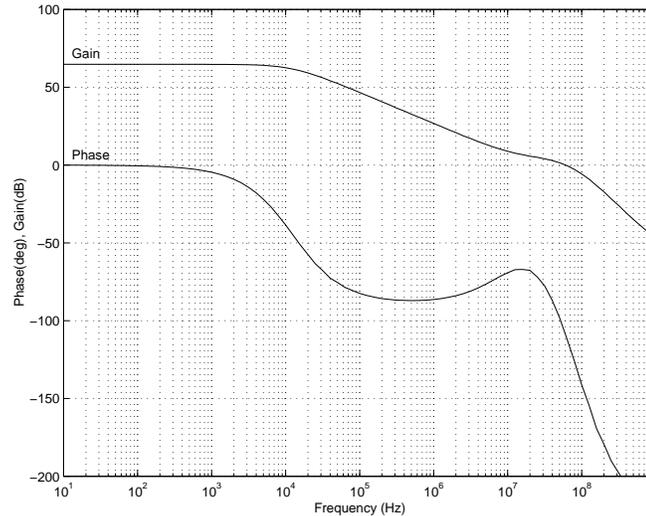


FIGURE 4.6: Typical frequency response of the two stage class A/AB operational amplifier

Fig. 4.7 shows the circuit for the pre-amplifier used in the comparator. This is a normal folded cascode amplifier, and its bias circuit is shown in Fig. 4.8. The common mode feedback circuit of this folded cascode pre-amplifier has the same structure as Fig. 4.5.

The latch circuit in Fig. 4.2 is shown in Fig. 4.9. When the latch signal is low, M2 and M3 work in the triode region while M4 and M5 are cut off. This serves to clear the memory of the latch and isolate the output status from the input signal. Since both \bar{S} and \bar{R} (port Sb and Rb in Fig. 4.9) are set to high when the latch signal is low, M6 and M7 are turned on thus the input differential signal reaches the drains of these two transistors. When latch signal becomes high, M2 and M3 are turned off

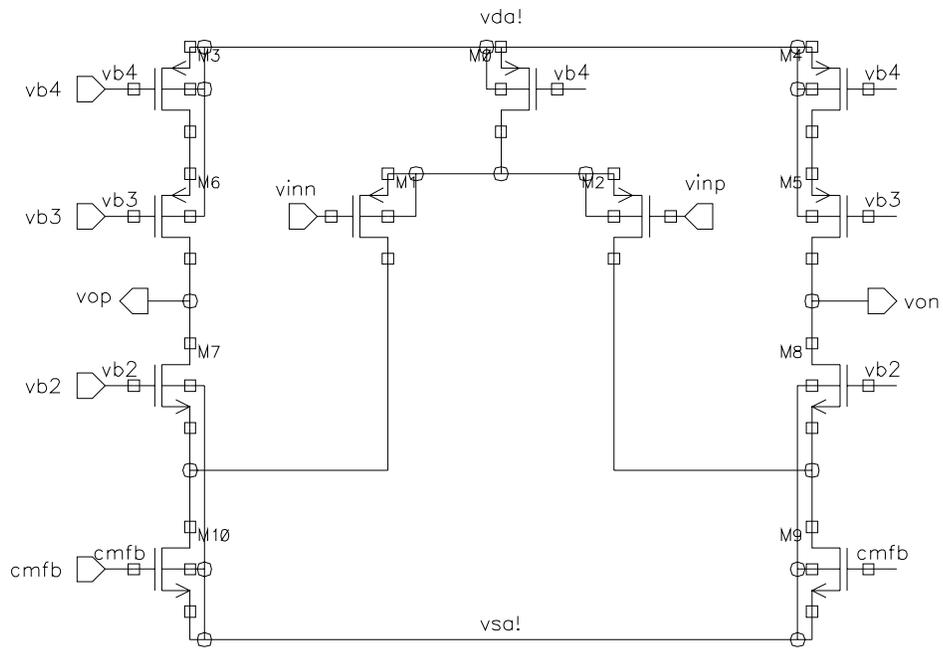


FIGURE 4.7: Pre-amplifier of comparator

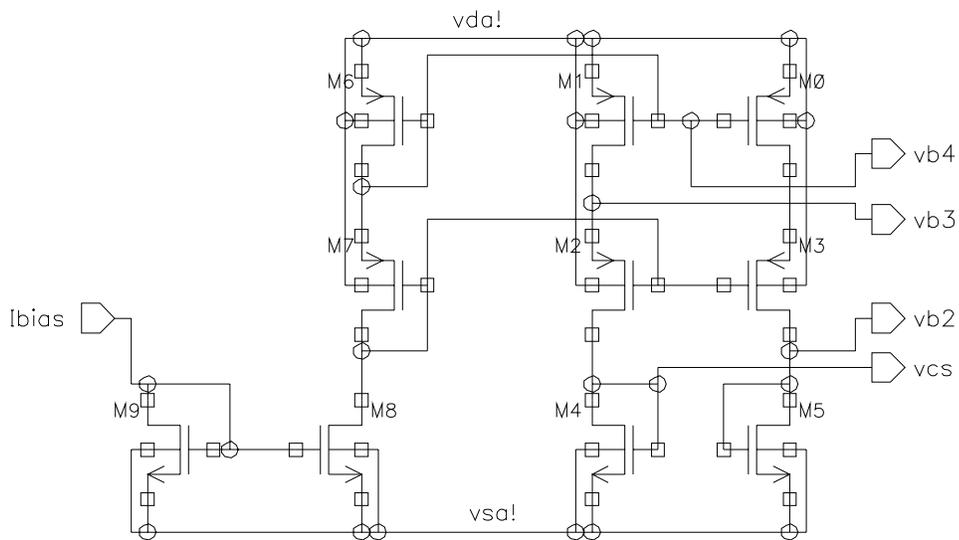


FIGURE 4.8: Bias circuit of the pre-amplifier of comparator

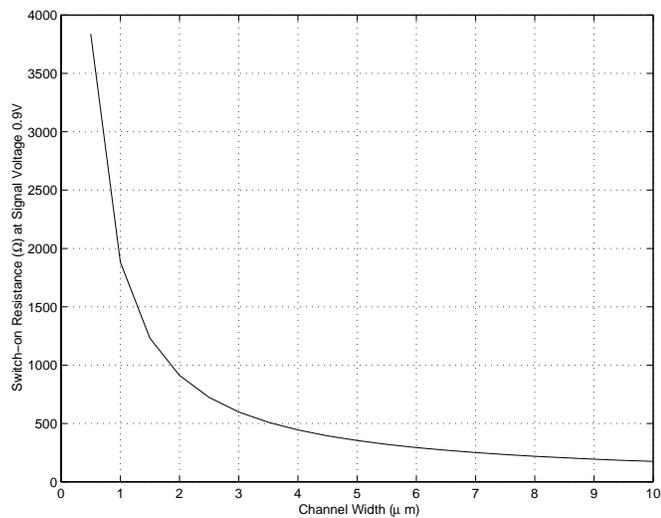


FIGURE 4.10: NMOS switch-on resistance varies with switch size

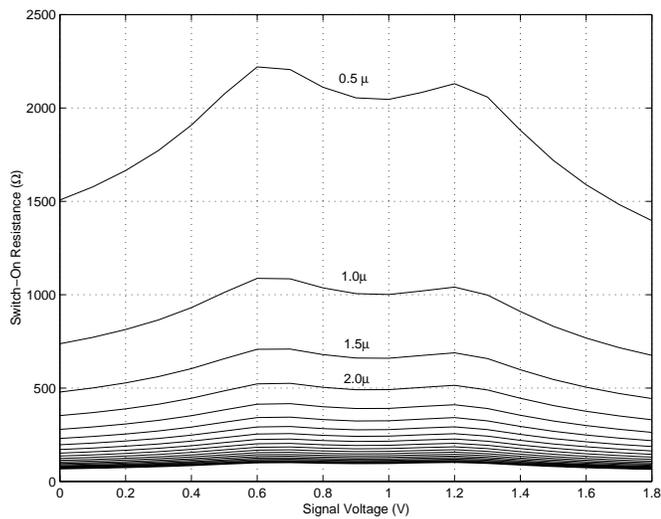


FIGURE 4.11: CMOS switch-on resistance R with different switch sizes vary with settling voltage

age is close to the analog ground, while CMOS switches have to be used for those nodes where settling voltage varies in a wide range, such as switches connected to the output of op-amp or the top plate of signal capacitor C_{sig} or reference capacitor C_{ref} , etc. Switch sizes are first estimated from the manual calculations based on the RC time constants of each possible connection and available settling time for those connections. Fig. 4.10 and Fig. 4.11 are typical relationships between switch-on resistance and transistor size and can be used to manually estimate the switch size. These two figures are obtained under the condition that channel lengths of both PMOS and NMOS are fixed to be 0.18μ . Both figures are results from HSPICE simulations. Simulation for Fig. 4.10 are straight forward, but that of Fig. 4.11 needs additional steps. Because of the difference of carrier mobilities between PMOS and NMOS, in order to obtain symmetric switch-on resistance of CMOS switch with settling voltages relative to the analog ground, PMOS channel width must be wider than that of NMOS. The ratio W_p/W_n is found to be 3.4 through HSPICE simulations. The channel width above each curve in Fig. 4.11 corresponds to that of NMOS. Fig. 4.12 and Fig. 4.13, which are the intermediate results for obtaining Fig. 4.11 by HSPICE simulations, serve for better understanding the fact that there are two humps at the settling voltages around the analog ground.

Note that intensive HSPICE simulations are indispensable for the optimization of final switch sizes. Simulation shows that switch sizes are critical for the performance of the designed switched capacitor SAR ADC.

4.4 Digital Component Design

In this switched capacitor successive approximation A/D converter with the capacitance mismatch error cancellation algorithm, the function of the digital block is not

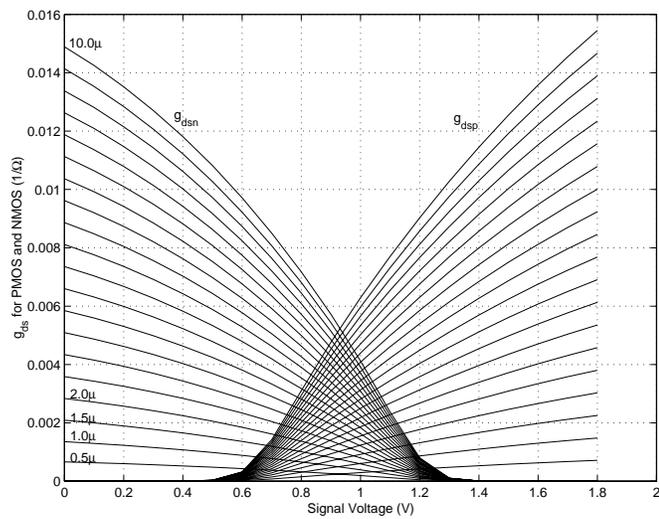


FIGURE 4.12: CMOS switch-on transconductances g_{dsn} and g_{dsp}

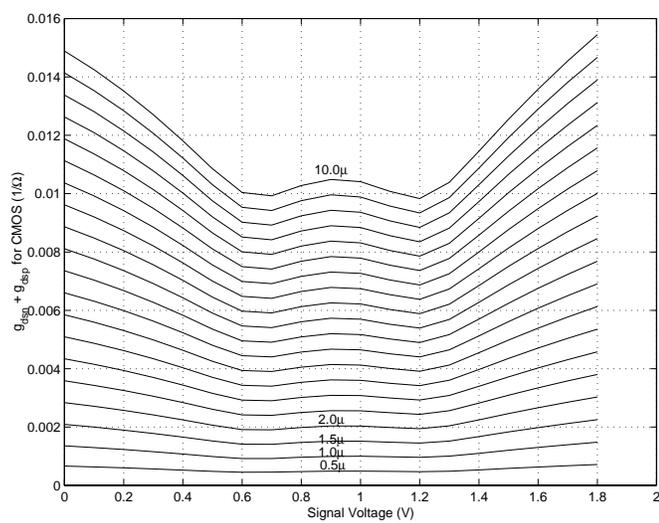


FIGURE 4.13: CMOS switch-on transconductance $g_{ds} = g_{dsn} + g_{dsp} = 1/R$

only a clock generator that produces periodic non-overlap clock signals, but also a finite state machine that produces the non-periodic sequential logic control signal to realize the algorithm. The top level of the digital block is shown in Fig. 4.14.

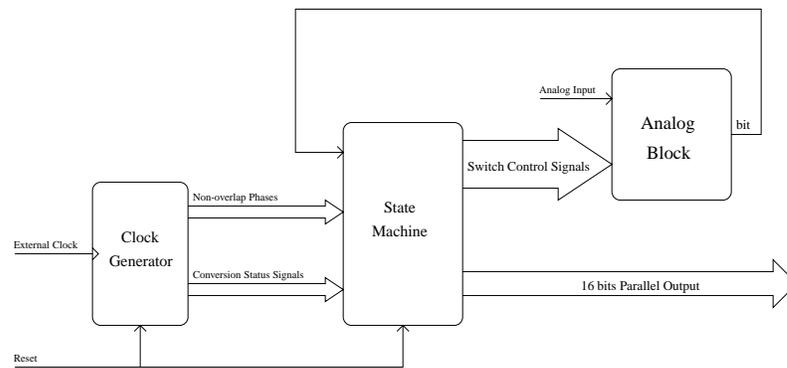


FIGURE 4.14: Top level of digital block relative to analog block of the SC SAR-ADC

4.4.1 Clock Generator

The timing diagram of all clock signals is shown in Fig. 4.15. Driven by the external master clock, a two-phase non-overlap clock Φ_1 and Φ_2 are generated by circuit introduced in [6]. Signal “clearF” starts the conversion of a new sample. This signal is necessary to reset the flag of the state machine that traces the error charge free capacitor, as described in chapter 2. At the beginning of each sample, the error free capacitor must be reset to C_{ref} . Another function of signal “clearF” is to gate Φ_1 and Φ_2 and generate ϕ_{01} and ϕ_{02} for predictive phase and actual sampling phase to sample the input signal. Signal “Refresh” marks two phases of predictive CDS operation of the LSB, which corresponds to phase ① in Fig. 4.1. Its invert signal “ $\overline{Refresh}$ ”

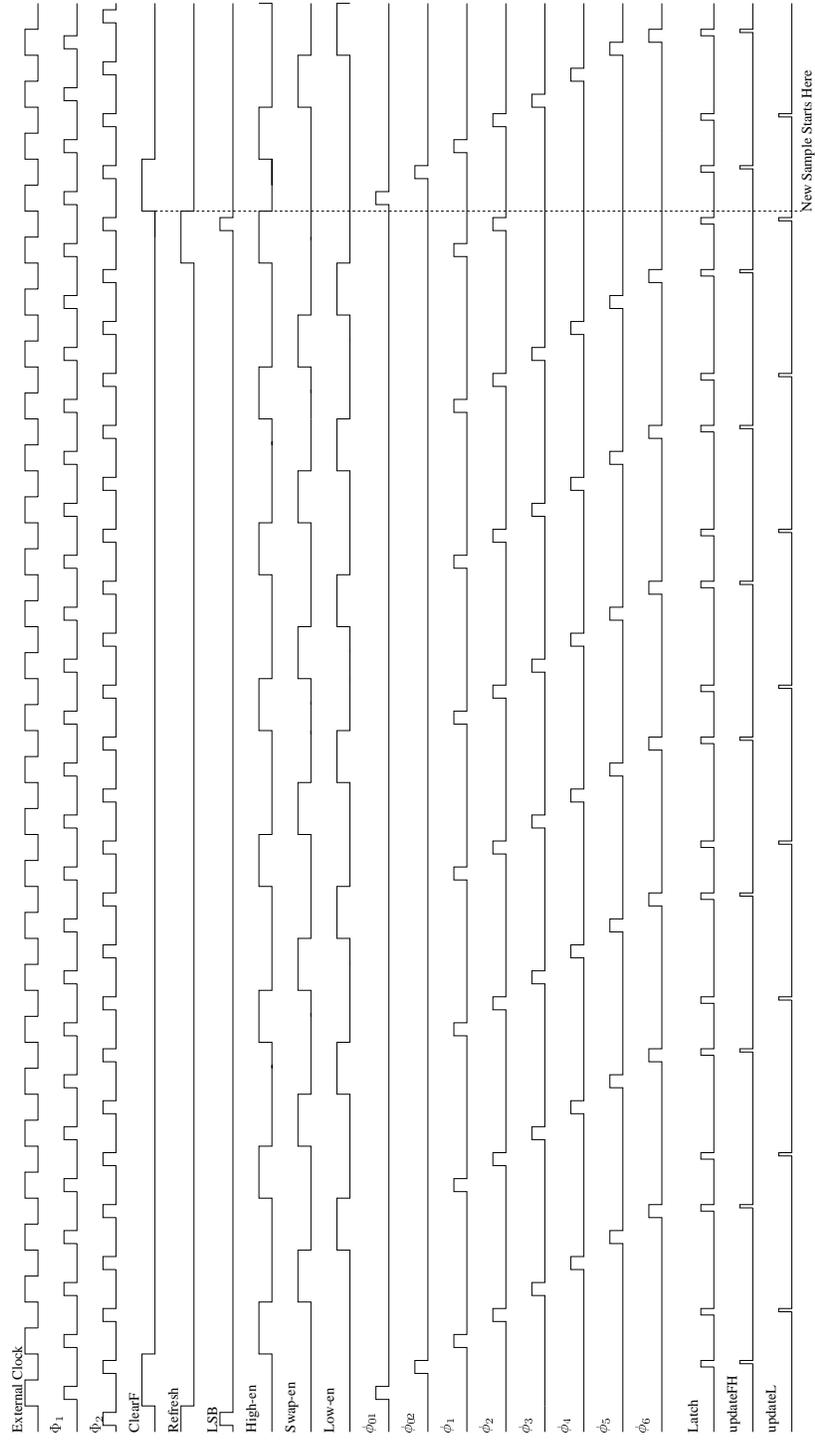


FIGURE 4.15: Timing diagram of the clock generator

corresponds to phase ② in the same figure. Signal “LSB” is created by “Refresh” and Φ_2 , which is necessary to discharge the relevant capacitors for preparing to sample the next input signal. As shown in Fig. 4.15, each sample needs 23 external clock periods, therefore a 0 ~ 22 counter is needed.

MSB is generated by sampling phases ϕ_{01} and ϕ_{02} . Because of the operational difference between sampling and normal conversion, these two phases are separated from normal 6-phase conversion sequences. This leads to a non-periodic clock structure for ϕ_1 through ϕ_6 , as shown in Fig. 4.15, however, this reduces the number of clocks needed for each sample. Otherwise 27 clocks are needed for each sample, among them 3 clocks are wasted to maintain the periodic 6-phase clock structure. In order to obtain the non-periodic 6-phase clock structure, 3 internal clock envelope signals “High_en”, “Swap_en” and “Low_en” are generated from the counter. These envelope signals will be used to gate the normal non-overlap 2-phase clocks Φ_1 and Φ_2 . Specifically, Φ_1 and Φ_2 are gated by “High_en” to generate ϕ_1 and ϕ_2 , by “Swap_en” to generate ϕ_3 and ϕ_4 , by “Low_en” to generate ϕ_5 and ϕ_6 .

“Latch” signal is generated at the end of phases ϕ_{02} , ϕ_2 and ϕ_6 for latching the results of the comparator. After a short delay for binary signal regeneration in the latch of Fig. 4.2, output “bit” of the comparator is updated either as the higher bit by signal “updateFH” or the lower bit by signal “updateL”.

Conversion status signals “clearF”, “Refresh”, “LSB”, “Latch”, “updateFH” and “updateL” may be directly used by switches in the analog block, while phase clock signals ϕ_{01} , ϕ_{02} , ϕ_1 , ϕ_2 , ϕ_2 , ϕ_2 , ϕ_5 and ϕ_6 must be gated by state machine to generate proper switch clocks for the algorithm discussed in chapter 2 and chapter 3. The state machine is discussed in the following section.

The circuit implementation of the clock generator is shown in Fig. 4.16.

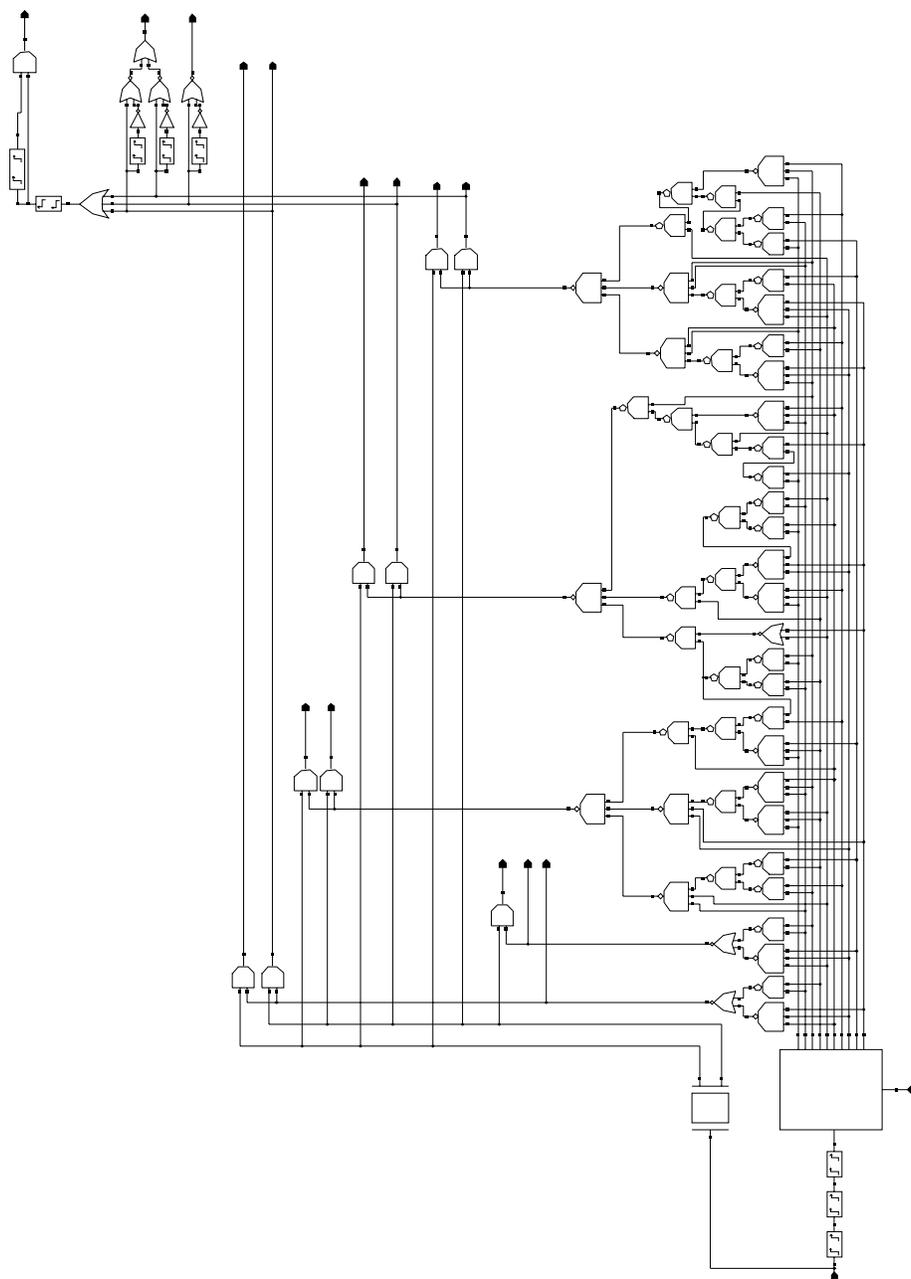


FIGURE 4.16: Circuit implementation of clock generator

4.4.2 Finite State Machine

The state transition diagram of the finite state machine in Fig. 4.14 is shown in Fig. 4.17.

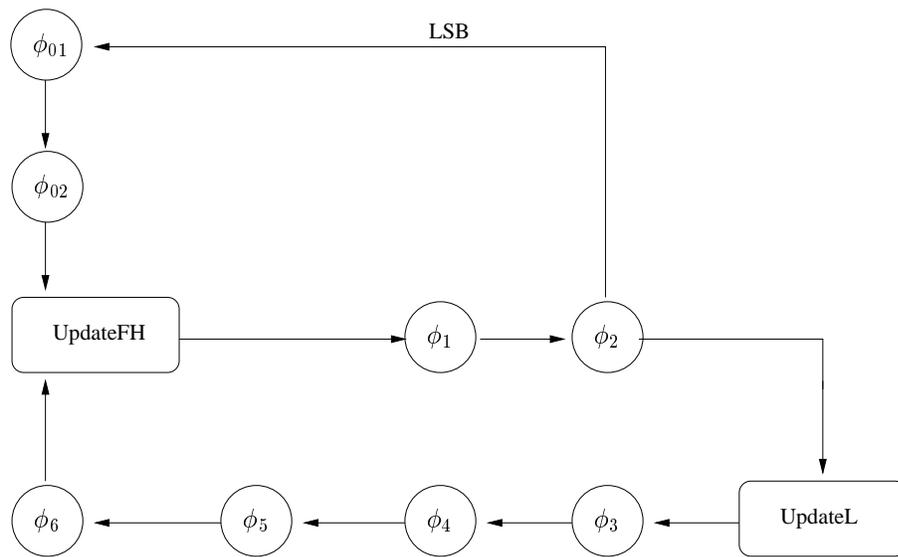


FIGURE 4.17: State transition diagram of SAR – ADC

Strictly speaking, the clock generator described above is part of the finite state machine, because the state transition sequence has already been determined by the sequence of non-overlap phases and timing of the conversion status signals. However, the type of operation (ADD/ADD, ADD/SUB, SUB/ADD and SUB/SUB) must be determined in the finite state machine based on the result of the analog output “bit”. This is implemented by updating certain flags in the finite state machine by “UpdateFH” and “UpdateL” operations. Since non-overlap phase signals cannot be directly used as switch clocks, they must be gated and multiplexed into actual switch

clocks by this finite state machine.

Circuit implementation of the state machine is shown in Fig. 4.18.

In order to eliminate signal dependent charge injection, switches connected to the signal voltage dependent nodes should be closed after other switches are closed. Therefore short delays are necessary for some switch signals after the finite state machine.

4.5 Full Chip Simulation

Full chip simulations are performed during the design parameter optimizations. Since there are a lot of transistors inside digital block, a full transistor level simulation, which include both analog and digital components, will be too time consuming to be implemented. Therefore the following approach is used. Digital block is first simulated in the full transistor level by HSPICE. Once the correct control logic has been verified by transistor level simulations, all gates in digital block will be represented by proper verilog models. The full chip simulations are then performed by simulator “spectreSVerilog” inside CADENCE. In simulations the numerical relative tolerance is 10^{-3} , voltage absolute tolerance 10^{-6} and current absolute tolerance 10^{-12} . The final simulation result is shown in Fig. 4.19.

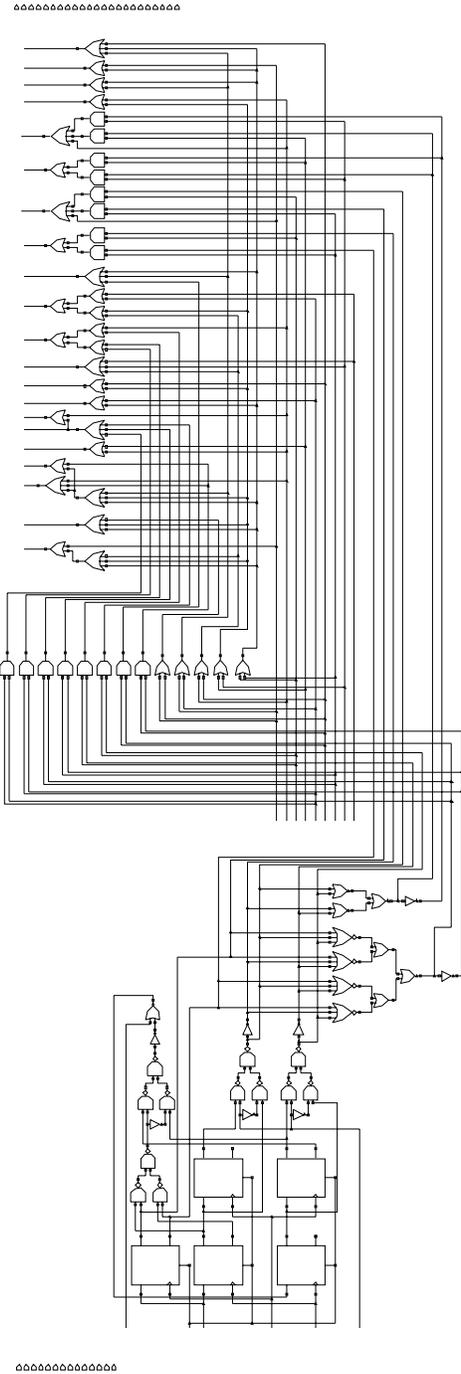


FIGURE 4.18: Circuit implementation of state machine

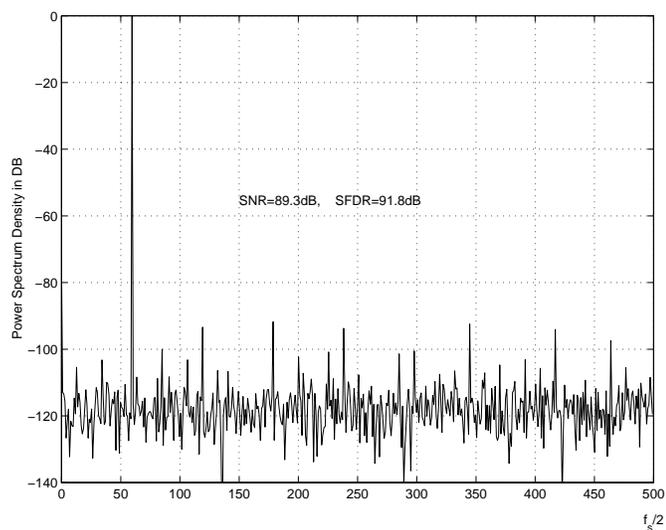


FIGURE 4.19: Output spectrum of the switched capacitor SAR – ADC by full chip simulation

The layout of this chip with National Semiconductor CMOS9 process is shown in Fig. 4.20.

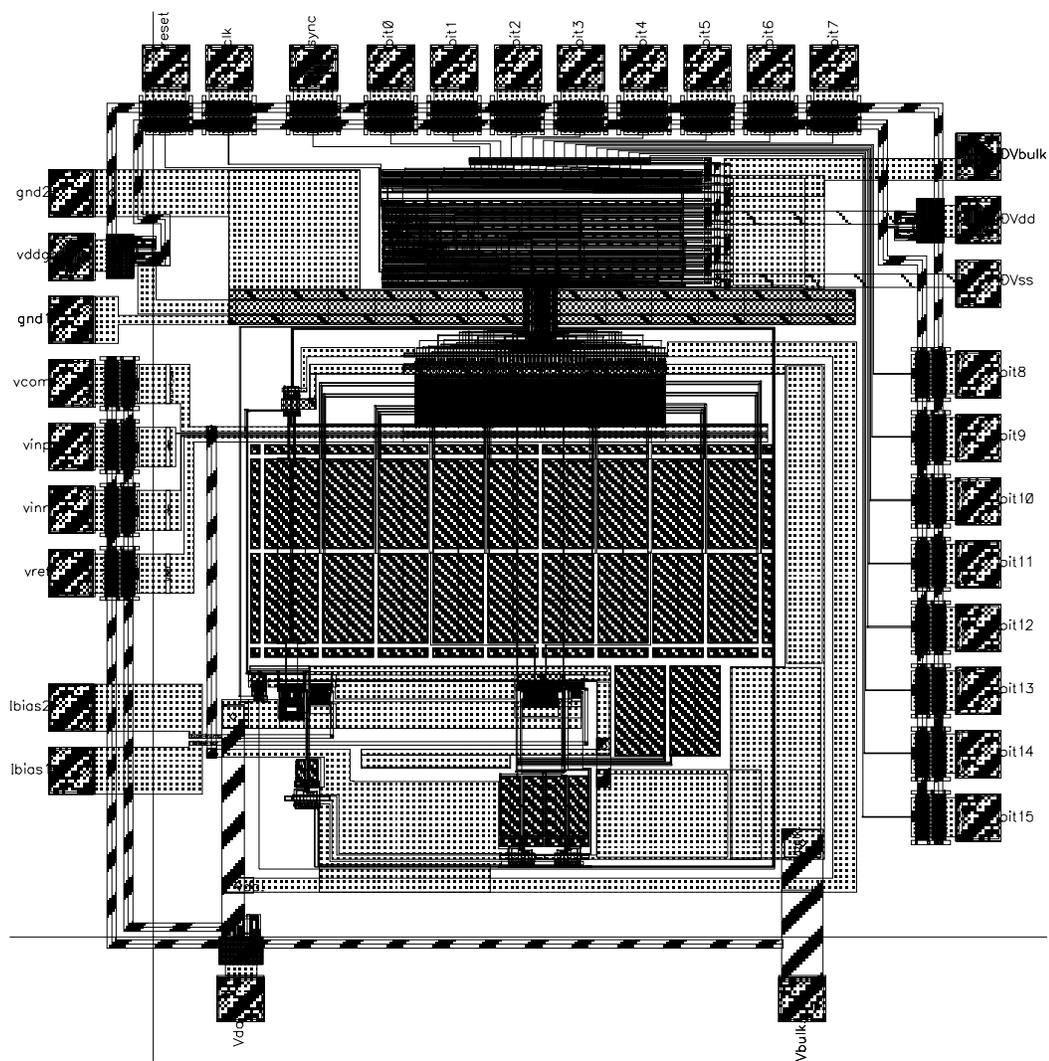


FIGURE 4.20: Layout of the switched-capacitor successive approximation ADC

Chapter 5

Summary and Future Work

5.1 Summary

The mismatch error canceling algorithm of the switched capacitor successive approximation A/D converter has been improved. Compared to the original algorithm, the finite state machine of the digital block for switch control is expanded because of the tracing of the error charge free capacitor, but the error canceling operation becomes more consistent.

The predictive correlated double sampling technique in the switched capacitor successive approximation A/D converter was studied theoretically, which revealed that normal predictive correlated double sampling technique is not adequate to achieve high resolution SC SAR – ADC. The operational difference of predictive CDS in SC SAR – ADC from that in other applications were explained. Based on the above studies, a predictive CTS technique was proposed as an improvement of predictive CDS in SC SAR – ADC, which was proved efficient by SWITCAP simulations.

A 1.8V switched capacitor SAR – ADC was designed with National Semiconductor CMOS9 technology, which adopted results of above researches. The detailed transistor level design and its layout were provided. Full chip simulation shows that the design was successful, and this switched- capacitor ADC was fabricated.

5.2 Plan of Future Work

The test board of the designed SC SAR – ADC needs to be designed and fabricated in order to test the performance of the designed chip. The improvement of this A/D converter should eventually result in the application of a real product.

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