Design of High Efficiency Step-Down Switched Capacitor

DC/DC Converter

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A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented May 21, 2003
Commencement June 2003

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1. INTRODUCTION

1.1. Background

A DC/DC converter is a device that accepts a DC input voltage and produces a DC output voltage. Typically, the output produced is at a different voltage level than input.

Portable electronic devices, such as cell phones, PDAs, pagers and laptops, are usually powered by batteries. After the battery has been used for a period of time, the battery voltage drops depending on the types of batteries and devices. This voltage variation may cause some problems in the operation of the electronic device powered by the batteries. So, DC/DC converters are often used to provide a stable and constant power supply voltage for these portable electronic devices.

According the components used for storing and transferring energy, there are two main kinds of topologies in DC/DC converters: inductive converters and switched capacitor converters. The inductive converter using inductor as energy storing and transferring component has been a power supply solution in all kinds of applications

for many years. It is still a good way to deliver a high load current over 500mA. But in recent years, since the size of portable electronic device is getting smaller and smaller, and the load current and supply voltage are getting lower and lower, the inductorless converters based on switched capacitor are more and more popular in the space-constrained applications with 10mA to 500mA load current. Such converters avoid the use of bulky and noisy magnetic components, inductors. They are available in small packages, operate with very low quiescent current and require minimal external components. They have been the main power supply solution for handheld portable instrumentations.

1.2. Motivation

For current handheld instrumentations, such as cell phones and PDAs, the power supply voltage is about 1.8V or lower in the conceivable future, however, their battery voltage variation is from 4.2V to 2.8V for usable range and about 5.0V during being charged. Consequently, step-down DC/DC converters, accepting a high input and providing a low output, are needed.

In this thesis, two high efficiency step-down switched capacitor DC/DC converters are designed, and the architecture of converters will be described and the design issues will be discussed.

1.3. Organization of the Thesis

The thesis is organized as follows. The basic concepts of switched capacitor array and gain configuration are explained in Chapter 2. The related techniques in switched capacitor DC/DC converters are described in Chapter 3. A switched capacitor DC/DC converter with fixed output options 1.5V, 1.8V and 2.0V is designed and the design issues are discussed in Chapter 4. Another design of switched capacitor DC/DC converter with output 1.2V is investigated in Chapter 5. Conclusions are given in Chapter 6.

2. BASIC CONCEPTS OF SWITCHED CAPACITOR ARRAY

The core circuit of switched capacitor DC/DC converters is the switched capacitor array, which is composed of switches and a few capacitors, traditionally called "flying capacitors", used for storing and transferring energy. By turning on and turning off switches to change the connection of flying capacitors, these capacitors can be charged or discharged and the charges can be delivered to or removed from the output. This topology is called charge pump and the switched capacitor converter is also called charge pump converter. In this chapter, an example of switched capacitor array is given to introduce some basic concepts and explain how the charge pump converter works.

2.1. Structure of Switched Capacitor Array

Figure 2.1 shows a switched capacitor array [1], which is used in converter LM3352, a multiple-gain DC/DC converter designed by National Semiconductor Corporation.

For LM3352, there are three flying capacitors, C1, C2 and C3, which are used to deliver charges from the input to the output. Because of their large values, such as 1μF, these capacitors are external to the integrated circuit.
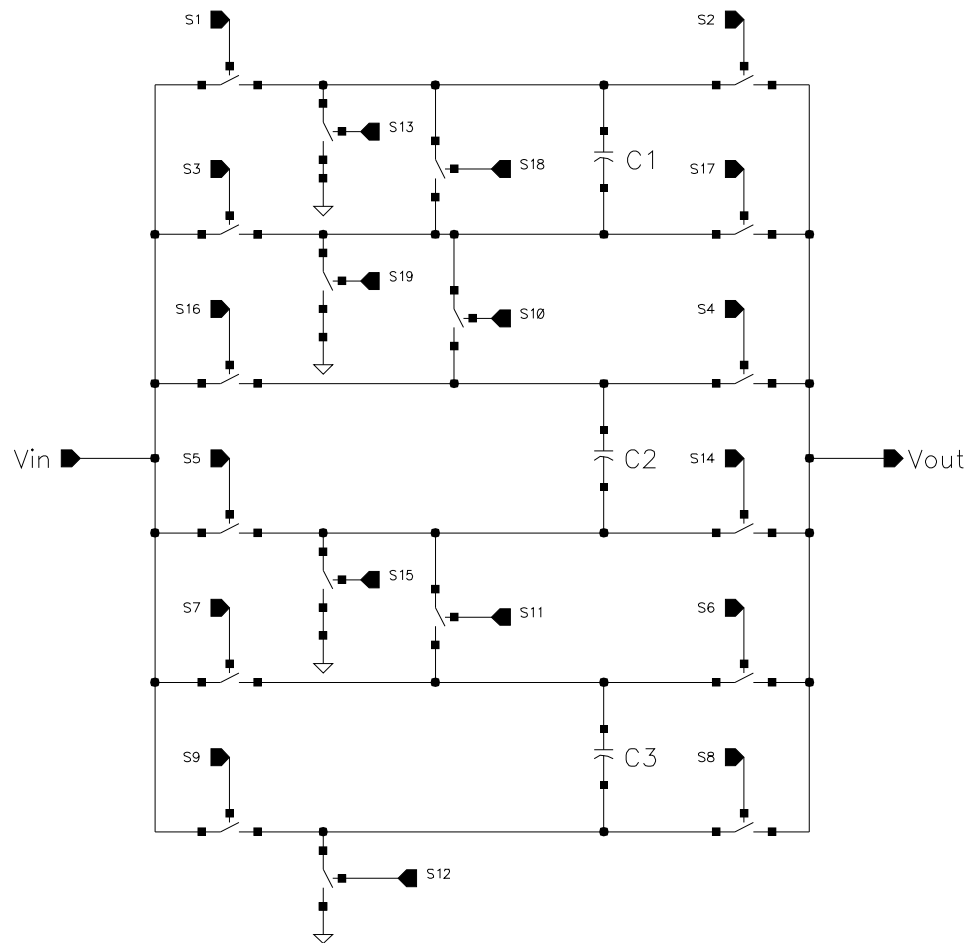
Figure 2.1. Switched capacitor array of LM3352

S1 through S19 are switches, which are implemented in the integrated circuit using N type or P type MOS transistors. Their gate controlling signals, usually using clock signals, control the connections of the flying capacitors by turning on or turning off the switches.

When the switch is closed, the resistance of switch is called switch-on

resistance, which can be described as the equation: $Ron = \dfrac{1}{\mu Cox \dfrac{W}{L} Veff}$ [2]. In order

to minimize the energy dissipated in the switch-on resistance, the transistors used as

switches are designed to have a very large ratio of $\dfrac{W}{L}$, where W is the gate width and

L is the effective gate length.

2.2. Gain Configurations

By the operation of switches, the switched capacitor array of LM3352 is

capable of providing one common phase and seven gain phases, with the gain being

the ratio of the output voltage V_{out} to the input voltage V_{in}. The equivalent circuits of

these phases are shown in Figure 2.2 [1].

In these configurations, there are three gain configurations referred as boost

stages whose gains are greater than 1, three gain configurations referred as buck stages

whose gains are less than 1 and one gain configuration referred as unit gain with gain

equal to 1. According to the input and the output, the DC/DC converters are divided to

two types: step-up or boost converters ($V_{out}>V_{in}$) and step-down or buck converters

($V_{out}<V_{in}$).

common

gain=1

gain=1/2

gain=2

gain=2/3

gain=3/2

gain=3/4

gain=4/3
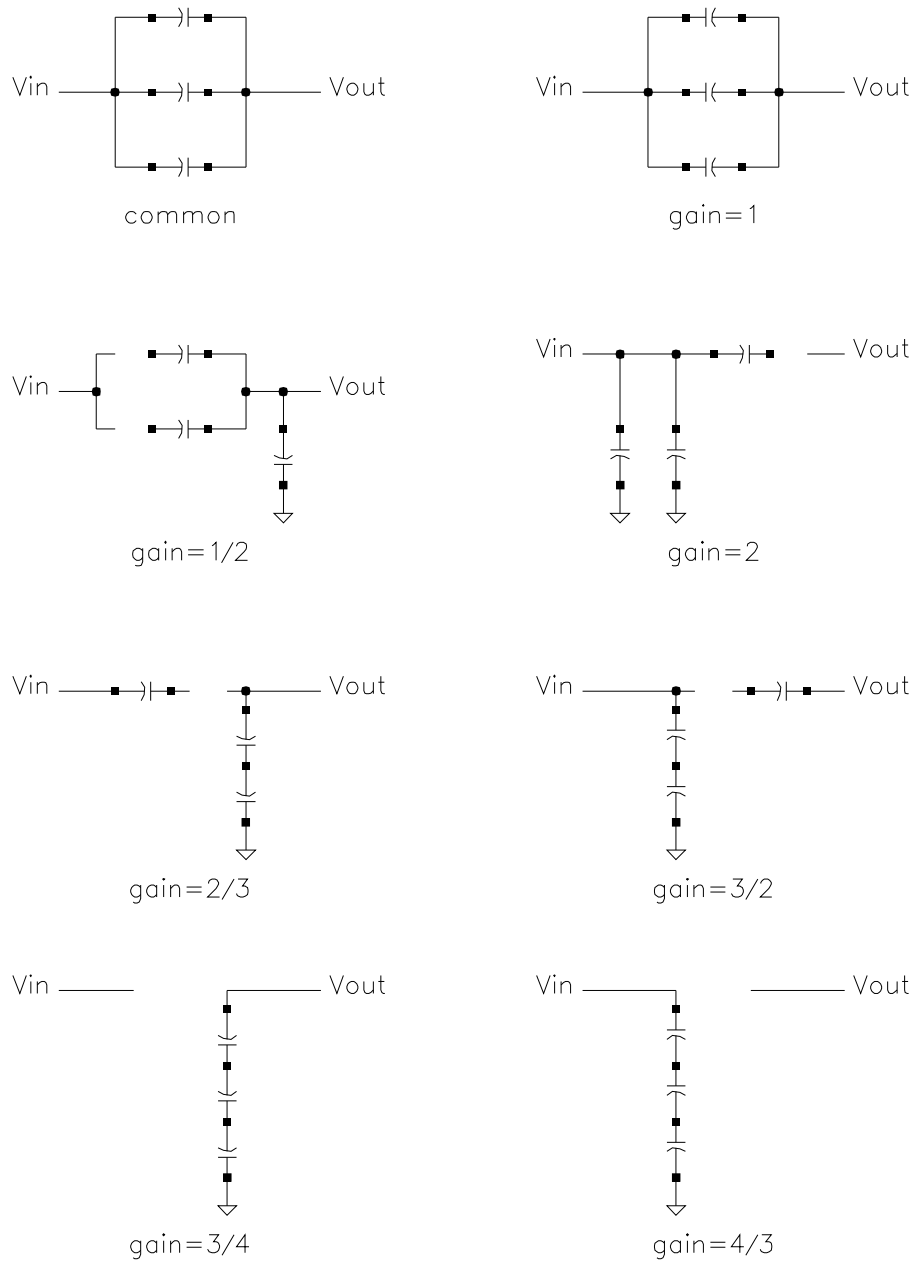
Figure 2.2. Common phase and gain phase configurations of LM3352

When the converter is clocked and the gain setting is chosen, the switched capacitor array is switched between the common phase and one of seven gain phases to deliver charges from the input to the output to keep a constant output voltage. The gain configuration of 1/2 is used as an example to explain the implementation of gains through the switched capacitor array. The equivalent circuit of gain configuration of 1/2 is shown in Figure 2.3 below. The flying capacitor Cf is used to store and transfer energy, and capacitor Ch is the hold capacitor for the output.
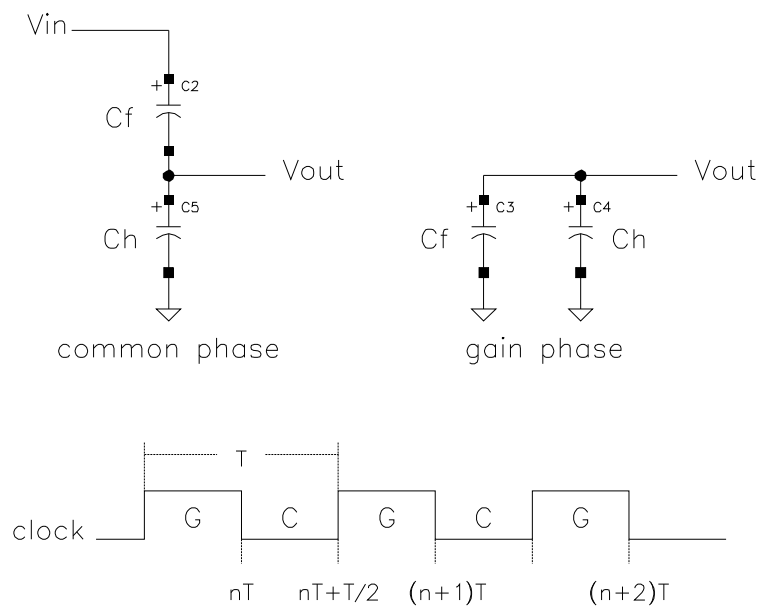
Figure 2.3. Equivalent circuit of the gain configuration with gain of 1/2

At time nT, the charge pump stays at the end of the gain phase, and the charges in the capacitors Ch and Cf are

$$Qch(nT) = Ch * Vout(nT) \tag{3.1}$$

$$Qcf(nT) = Cf * Vout(nT) \tag{3.2}$$

At time nT+T/2, the charge pump stays at the end of the common phase, the charges in the capacitors Ch and Cf are

$$Qch(nT + T/2) = Ch * Vout(nT + T/2) \tag{3.3}$$

$$Qcf(nT + T/2) = Cf * [Vin - Vout(nT + T/2)] \tag{3.4}$$

According to the theory of charge conversation, we have

$$Qch(nT + T/2) - Qcf(nT + T/2) = Qch(nT) - Qcf(nT) \tag{3.5}$$

Solving Equation (3.1) (3.2) (3.3) (3.4) and (3.5) results in

$$Vout(nT + T/2) = \frac{Cf}{Ch + Cf}Vin + \frac{Ch - Cf}{Ch + Cf}Vout(nT) \tag{3.6}$$

$$Qch(nT + T/2) = \frac{Ch * Cf}{Ch + Cf}Vin + \frac{Ch * (Ch - Cf)}{Ch + Cf}Vout(nT) \tag{3.7}$$

$$Qcf(nT + T/2) = \frac{Ch * Cf}{Ch + Cf}Vin - \frac{Cf * (Ch - Cf)}{Ch + Cf}Vout(nT) \tag{3.8}$$

At time nT+T, the charge pump is switched back to the gain phase. According to the theory of charge conservation, the total charges in the capacitors Ch and Cf are

$$Qtotal(nT + T) = Qch(nT + T/2) + Qcf(nT + T/2) \tag{3.9}$$

So the output voltage at time nT+T is

$$Vout(nT + T) = \frac{Qtotal}{Ch + Cf} = \frac{2ChCf}{(Ch + Cf)^2}Vin + \frac{(Ch - Cf)^2}{(Ch + Cf)^2}Vout(nT) \tag{3.10}$$

Assuming $a = \dfrac{2ChCf}{(Ch + Cf)^2}$ and $b = \dfrac{(Ch - Cf)^2}{(Ch + Cf)^2}$, Equation (3.10) can be rewritten as

$$Vout(nT + T) = a * Vin + b * Vout(nT) \tag{3.11}$$

According to Equation (3.11), we can have

$$Vout(nT + 2T) = a * Vin + b * Vout(nT + T)$$

$$= a * Vin + b * [a * Vin + b * Vout(nT)]$$

$$= aVin * (1 + b) + Vout(nT) * b^2 \tag{3.12}$$

$$Vout(nT + 3T) = a * Vin + b * Vout(nT + 2T)$$

$$= a * Vin + b * [aVin * (1 + b) + Vout(nT) * b^2]$$

$$= aVin * (1 + b + b^2) + Vout(nT) * b^3 \tag{3.13}$$

From Equation (3.12) and (3.13), we can have

$$Vout(nT + kT) = aVin * (1 + b + b^2 + ... + b^{k-1}) + Vout(nT) * b^k$$

$$= aVin * \frac{1 - b^k}{1 - b} + Vout(nT) * b^k \tag{3.14}$$

where k = 0, 1, 2, 3 …

Since $b = \dfrac{(Ch - Cf)^2}{(Ch + Cf)^2} < 1$, we can have

$$\lim_{k \to +\infty} Vout(nT + kT) = \frac{aVin}{1 - b} = Vin * \frac{2ChCf}{(Ch + Cf)^2} * \frac{1}{1 - \dfrac{(Ch - Cf)^2}{(Ch + Cf)^2}} \qquad (3.15)$$

$$= \frac{Vin}{2}$$

3. RELATED TECHNIQUES IN CONVERTERS

In order to provide a desired constant power supply voltage and improve the conversion efficiency, there are three important techniques to be used in the designed switched capacitor DC/DC converters: pulse frequency modulation (PFM), multiple gains and gain hopping, which will be explained in this chapter.

3.1. Pulse Frequency Modulation

Pulse frequency modulation (PFM) or pulse skipping is one of typical methods to be used to regulate voltages in DC/DC converters. The basic idea is illustrated in Figure 3.1.

When the output voltage V_{out} is less than the desired voltage $V_{desired}$, the skip signal is low, and the switched capacitor array is clocked to deliver charges constantly to the output. Accordingly, the output voltage V_{out} is raised. On the other hand, when V_{out} is greater than $V_{desired}$, the skip signal is high, the gate clock of switches is disabled and the charge pump stays in the common phase. Accordingly, there are no more charges to be delivered to the output. Then, V_{out} is reduced by the load current. Depending on the charge pump's running or stopping, the converter stays in one of two modes: the pump mode or the skip mode.
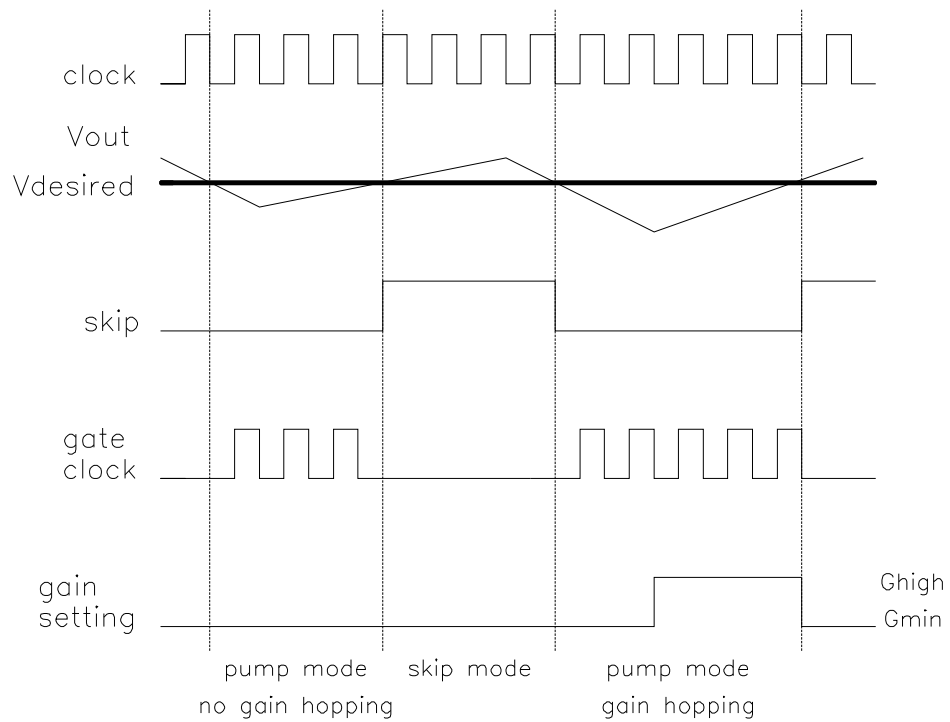
Figure 3.1. Waveform of PFM and gain hopping

3.2. Multiple Gains

As battery use continues, the battery voltage drops. For example, when a lithium ion (LiIon) battery, a typical battery for cell phones and PDAs, is discharged by a 100mA constant load current, the battery voltage drops from about 4.2V to 2.8V gradually [4]. During the beginning of a battery's life, the battery voltage may be higher than the desired voltage, so a step-down converter is used to provide the power

supply voltage. During the end of the battery's life, the battery voltage may be less than the desired voltage, so a step-up converter must be used. For some applications in which the desired power supply voltage is between the battery's highest voltage and lowest voltage during the battery life, a multiple-gain converter is need. It can change its gain configurations from the buck stage to the boost stage to provide the power supply voltage. Compared to the single-gain converter, the multiple-gain converter extends the usable battery life.

Another reason why we prefer the multiple-gain topology to the single-gain buck or boost topology is to improve conversion efficiency. For the same input and output voltage, the average conversion efficiency of multiple-gain converter is higher than that of single-gain converter. The conversion efficiency of single-gain topology may suffer at certain input voltages.

Efficiency can be approximated as follows [1]:

$$Eff = \frac{Vout}{Gsc * Vin} \tag{3.16}$$

G_{sc} denotes to the gain of switched capacitor array used in a DC/DC converter. $V_{desired}$ and V_{in} denote the desired output voltage and input voltage, respectively.

For example, if the desired output voltage is 2V and the gain of switched capacitor array G_{sc} is 2/3, the efficiency is maximized when V_{in} is 3.0V. However, if V_{in} is greater than 3.0V, then the output voltage provided from the gain of 2/3 is

greater than what is required, thereby reducing efficiency. In order to increase efficiency, other gains that are lower than 2/3 are needed in the converter.
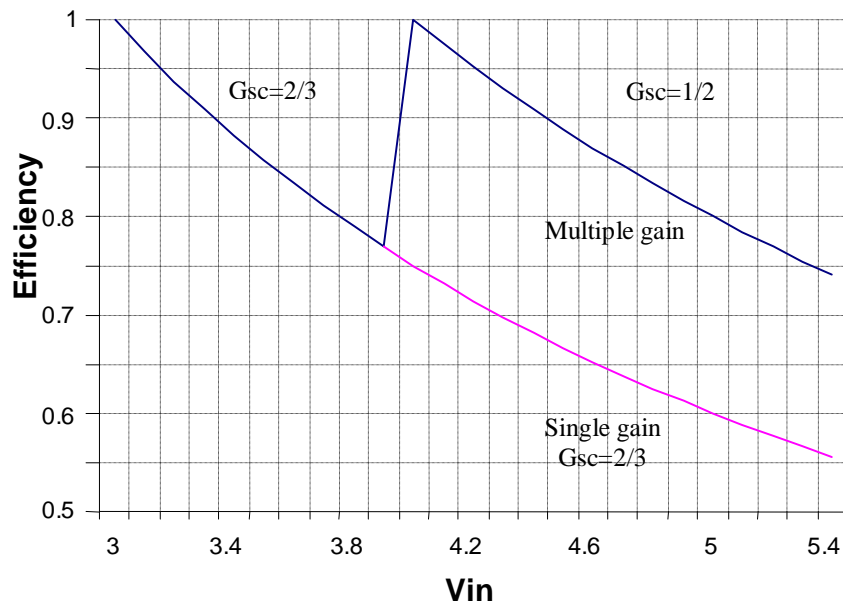
Figure 3.2 Efficiency of single-gain converter and multiple-gain converter

Figure 3.2 shows all efficiency comparison of a single-gain converter and a multiple-gain converter. The input voltage is from 3.0V to 5.4V and the desired output voltage is 2.0V. For the single-gain converter with a gain of 2/3, the average efficiency is about 78%. For the multiple-gain converter, the gain is set to 2/3 when the input voltage is less than 4.0V, and to 1/2 when the input voltage is larger than 4.0V. The

average efficiency of the multiple-gain converter is about 88%, which is 10% higher than that of the single-gain converter.

3.3. Gain Hopping

For the multiple-gain DC/DC converter, the minimum gain G_{min} chosen in the charge pump must satisfy the requirement $G_{min}*V_{in}>V_{desired}$. Otherwise, the converter can not provide a high enough output voltage. For some input voltages, if the load current is so large that the switched capacitor circuit with minimum gain G_{min} still can not deliver enough charges to the output to support a desired output voltage, another higher gain can be used. Under this condition, as discussed before, this higher gain, greater than the gain required (minimum gain), reduces efficiency.

To improve the efficiency, for some input voltages and load current, the charge pump is controlled to hop between the minimum gain and a higher gain, so that the charge pump can deliver enough charges to support a large load current at a desired output voltage without reducing the efficiency too much. As shown in Figure 3.1, during the pump mode, the charge pump runs at a lower gain for a few clock cycles, and runs at a higher gain for another few clock cycles. Consequently, the converter keeps hopping between different gains to make the average gain as low as possible to maximize the efficiency.

4. DESIGN OF A CONVERTER WITH FIXED

OUTPUT OPTIONS 1.5V, 1.8V AND 2.0V

In this chapter, a high efficiency switched capacitor step-down DC/DC converter will be presented; the simulation results will be given, and some important design issues will be discussed.

4.1. Design Motivation

Currently, for handheld portable devices, such as cell phones, pagers and PDAs, the battery voltage usually drops from 4.2V to 2.8V as battery use continues, and it varies to about 5.0V when the battery is charged. However, the power supply voltage for these electronic devices is around 1.8V, so a step-down DC/DC converter with high performance is needed.

4.2. Design Specification

The switched capacitor step-down DC/DC converter to be designed must efficiently produce a 200mA regulated low-voltage rail from 2.7V to 5.5V inputs. Fixed output voltage options of 1.5V, 1.8V, and 2.0V must be available. Multiple

fractional gain configurations are used to maximize conversion efficiency over the entire input voltage and output current ranges.

Two 1µF flying capacitors and two 10µF bypass capacitors are all the external components required, and no inductors are needed. It also features short-circuit protection, over-temperature protection and soft-start circuit.

The design specifications are listed below:

- 2.7V to 5.5V input range

- Output voltage options: 1.5V, 1.8V, 2.0V

- 200mA output current capability

- Multi-gain and gain hopping for highest possible efficiency

- Two 1µF flying capacitors and two 10µF bypass capacitors are all the external components required, and no inductors

- Shutdown supply current 0.1uA

- Soft start

- Thermal and short circuit protection

- Available in an 8-Pin MSOP package

In our design, a converter with output voltage 1.8V is designed first, and then it is changed for output options 1.5V and 2.0V.

4.3. Architecture of Converter

The architecture of designed converter is shown in Figure 4.1. There are two 1μF flying capacitors C1 and C2, which are external to the chip. On the chip, there are two control loops: pulse frequency modulation (PFM) loop and gain hopping loop.
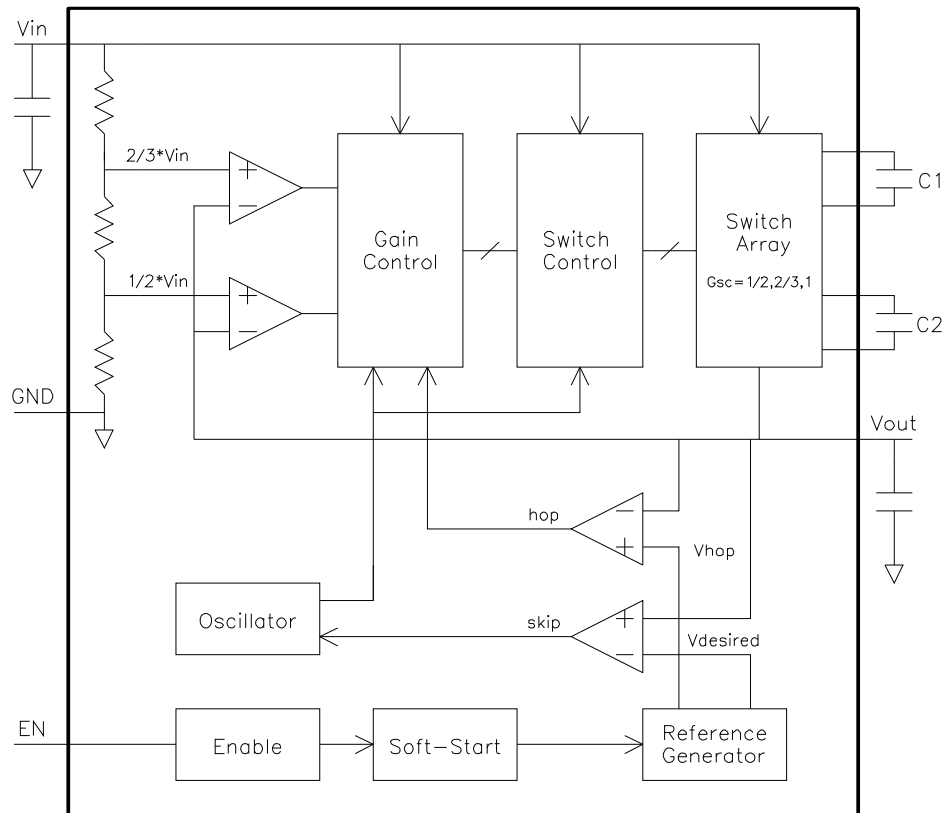

Figure 4.1 Architecture of converter

The PFM loop is composed of a reference generator, a comparator with an output signal *skip*, an oscillator and the Switch Control block. The reference generator

generates a desired output voltage $V_{desired}$. The comparator with the output signal *skip* compares the output voltage V_{out} with the desired output voltage $V_{desired}$. If V_{out} is less than $V_{desired}$, *skip* is low and it enables the oscillator to send out the clock signal driving the charge pump to deliver charges to the output. If V_{out} is greater than $V_{desired}$, *skip* is high and it disables the oscillator, so the charge pump stops to deliver charges to the output. Then, the output voltage V_{out} is reduced by the load current until V_{out} is less than $V_{desired}$ again. With the operation of PFM loop, the output voltage oscillates around the desired voltage, i.e. V_{out} is regulated to $V_{desired}$.

The gain hopping loop is composed of a reference generator, a comparator with an output signal *hop* and the Gain Control block. The reference generator generates a hopping voltage V_{hop}, and the comparator with the output signal *hop* compares V_{out} with V_{hop}. If V_{out} is greater than V_{hop}; *hop* is low and the charge pump is set to run at the minimum gain that is required. If the V_{out} is less than V_{hop}; *hop* is high and the charge pump is set to run at a higher gain. The function of gain hopping loop is deciding whether the required minimum gain or a higher gain is to be used.

In addition to the signal *hop*, the gain to be used in the converter is also related to the ratio of the output voltage to input voltage. A resistor string connected to the input and two comparators are used to for the Gain Control block to choose which gains can be used for different input voltages and output voltages.

The Switch Control block sets the gate clock signals of the switches in the Switch Array block. The Switch Array block with the two external flying capacitors together can provide three gain configurations with gain of 1/2, 2/3 and 1.

The typical circuit application of the converter is shown in Figure 4.2.
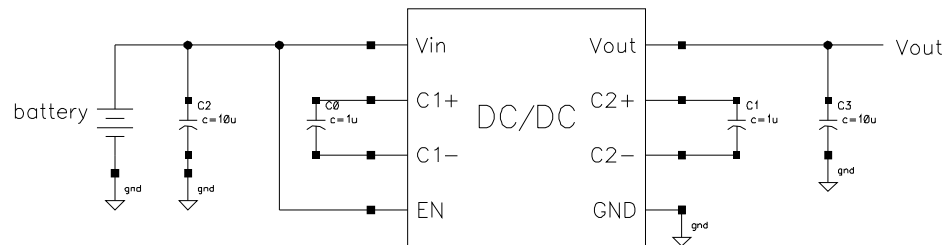
Figure 4.2. Typical application circuit

4.4. Gain Mapping

As mentioned before, the minimum gain used in the converter must satisfy the requirement $V_{desired} < G_{min} * V_{in}$. This requirement divides the entire range of V_{out} and V_{in} into several different gain regions, each having its own minimum gain G_{min}. For the designed converter with three gains, 1/2, 2/3 and 1, the gain regions are shown in Figure 4.3. There are totally three gain regions, which are divided by two lines

$$Vout = \frac{1}{2} * Vin \text{ and } Vout = \frac{2}{3} * Vin.$$

Figure 4.3. Gain regions

For each gain region, as shown in Table 4.1, there are two gains that can be used, one is the minimum gain G_{min} and the other one is a higher gain denoted by G_{max}. For the g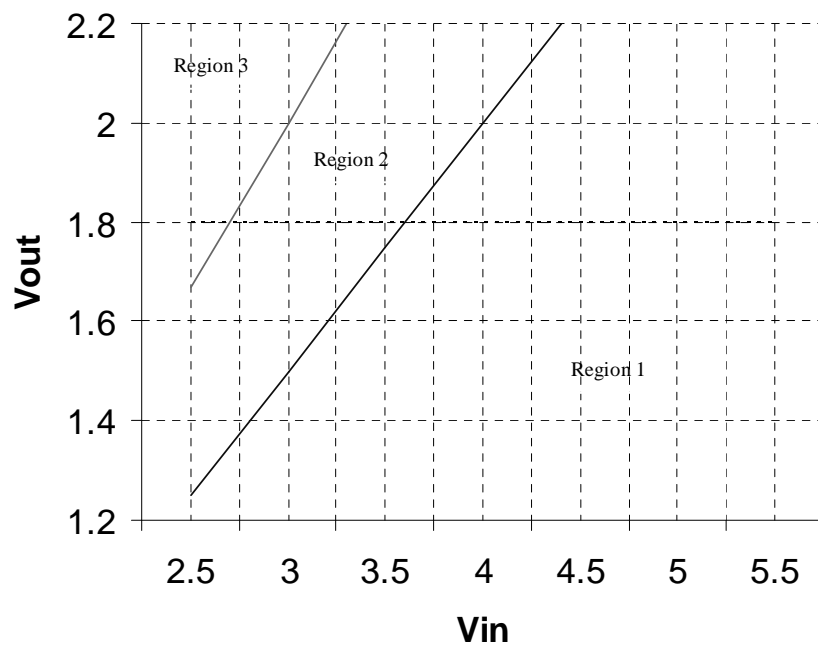ain region 1, theoretically, the maximum gain can be 1, but it is limited to 2/3 in our design because of the efficiency issue. If the gain of 1 is used in the region 1, the efficiency will be very low. As discussed before, the efficiency can be approximated as $Eff = \dfrac{Vdesired}{Gsc*Vin}$. For example, if the input voltage is 4V and the desired output voltage is 1.8V, the efficiency will be 67.5% for the gain of 2/3 and 45% for the gain of 1. So, the efficiency of the gain of 1 is 22.5% less than that of the gain of 2/3. In order to improve the efficiency, the gain configuration of 2/3 is designed to support the highest load current for the desired output voltage in the gain region 1 so that the gain of 1 doesn't have to be used.

Regions	G_{min}	G_{max}
1	1/2	2/3
2	2/3	1
3	1	1

Table 4.1. Gain options for gain regions

For each gain region, as mentioned before, the *hop* signal is used to decide which gain (G_{min} or G_{max}) to use. The hopping voltage V_{hop} is set to 1.48V, 1.78V and 1.98V for output options 1.5V, 1.8V and 2.0V, respectively. The gain control logic is shown in Table 4.2.

	$V_{out} > V_{desired}$	$V_{hop} < V_{out} < V_{desired}$	$V_{out} < V_{hop}$
Skip	high	low	low
Hop	Low	low	high
Gain	G_{min}	G_{min}	G_{max}

Table 4.2. Gain control logic

In order to protect the circuits from being destroyed by the large current during the time of start-up, the converter gradually raises the output voltage from zero to the desired output voltage rather than raise the output voltage as fast as possible. This is referred to as soft-start. In our design, it takes about 600 microseconds for the converter to raise the output voltage from zero to the desired output voltage.

4.5. Design of the Switched Capacitor Array

The switched capacitor array is one of the most important circuits in the converter. It dominates the performance, such as efficiency, ripple, load current capability and chip area.

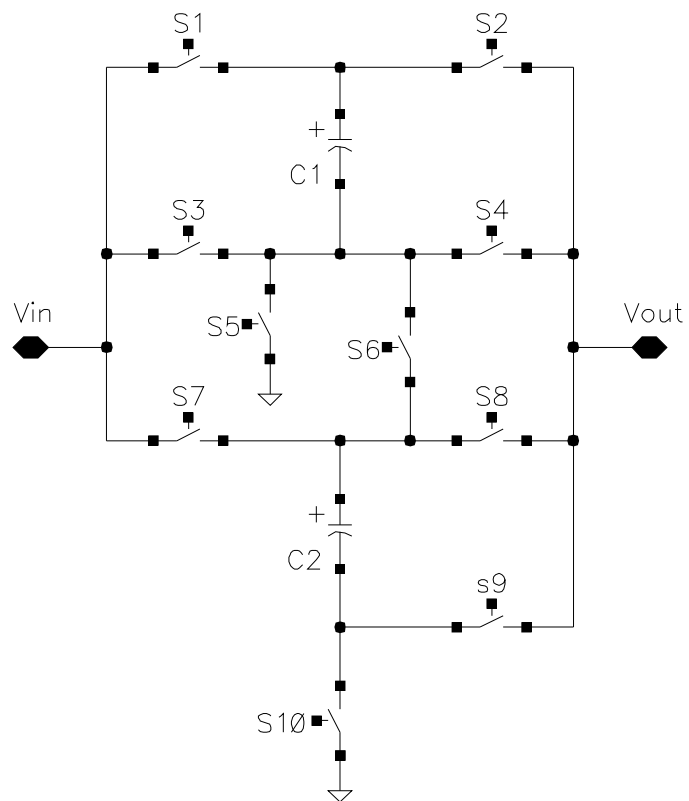### 4.5.1. Structure of the Switched Capacitor Array

Figure 4.4. Switched capacitor array

Figure 4.4 shows the switched capacitor array of the designed converter. It is composed of ten switches S1 through S10, and two 1μF external flying capacitors C1 and C2.
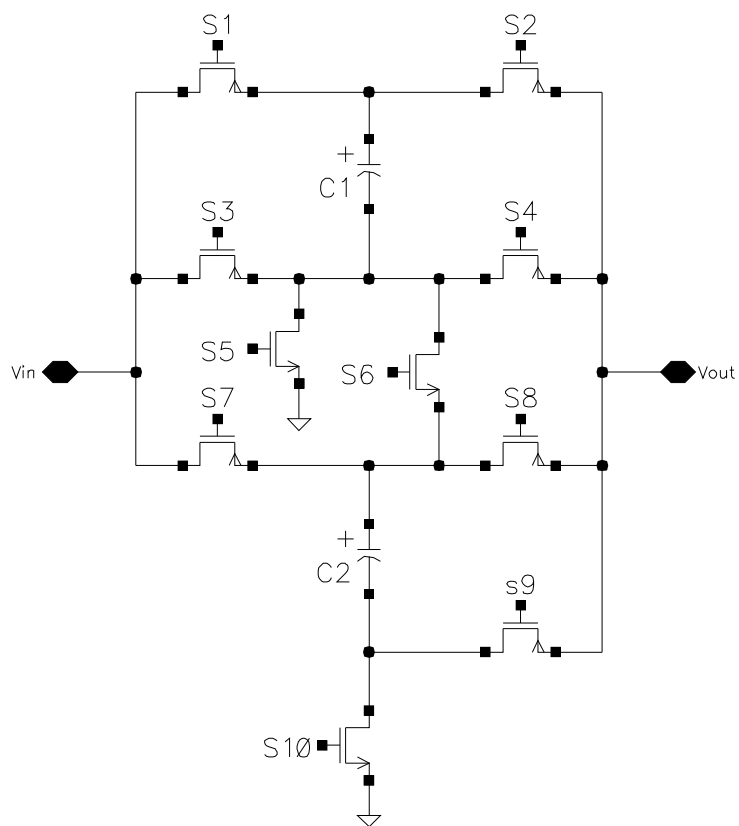
Figure 4.5 Implementation of the switched capacitor array

Generally, the switches which operate near ground level are implemented in the integrated circuit using NMOS transistors, and the switches which operate at more positive voltages are implemented with PMOS transistors. In some conditions, if the switch voltage falls within a very wide range, the switches are implemented by the use of N type and P type transistors connected in parallel and driven by complementary drive signals.

The embodiment of the designed switched capacitor array is shown in Figure 4.5. The switches S5, S6 and S10 use NMOS transistors and the other ones use PMOS transistors.

4.5.2. Gain Configurations
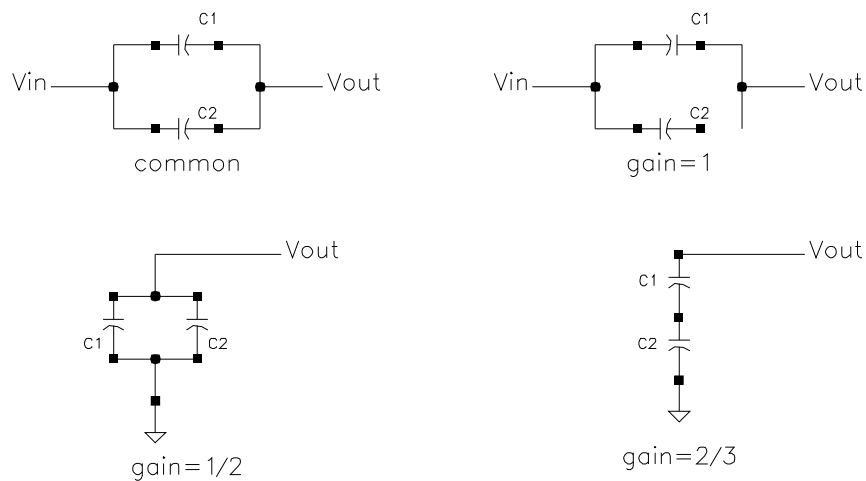
Figure 4.6. Configurations of the common and gain phases

For the output voltage options 1.5V, 1.8V and 2.0V, the switched capacitor array can provide three gains 1/2, 2/3 and 1. The configurations of the common phase and the gain phases are shown in Figure 4.6.

Switch	Common Phase	Gain Phase		
		G=1/2	G=2/3	G=1
S1	1	0	0	0
S2	0	1	1	1
S3	0	0	0	1
S4	1	0	0	0
S5	0	1	0	0
S6	0	0	1	0
S7	1	0	0	1
S8	0	1	0	0
S9	1	0	0	0
S10	0	1	1	0

Table 4.3. Switch states of different phases

The switch states in each configuration are shown in Table 4.3, which describes the connection of two capacitors through switches. In this table, "1" means that the switch turns on, i.e. it is closed, and "0" means that the switch turns off, i.e. it is open.

As mentioned before, when the charge pump is clocked, the switched capacitor array is switched between the common phase and one of the gain phases to deliver charges to the output. The implementation of different gains is explained as follows.

For the gain phase of gain of 1/2 shown in Figure 4.6, the external capacitors C1 and C2 are charged to V_{out} as described in the equation below

$$Vc1 = Vc2 = Vout \qquad (4.1)$$

In the common phase, C1 and C2 are connected in series between V_{in} and V_{out}. The voltages of C1 and C2 are now given by

$$Vc1 = Vc2 = Vin - Vout \qquad (4.2)$$

In steady state, both relations will hold. Combining Equation (4.1) with (4.2) results in:

$$\frac{Vout}{Vin} = Gsc = \frac{1}{2} \qquad (4.3)$$

For the gain phase of gain of 2/3 shown in Figure 4.6, the capacitors C1 and C2 are connected in series between the output and the ground. By inspection, the voltages of C1 and C2 are

$$Vc1 = Vc2 = \frac{1}{2} * Vout \qquad (4.4)$$

Combining Equation (4.4) with (4.2) results in:

$$\frac{Vout}{Vin} = Gsc = \frac{2}{3} \qquad (4.5)$$

As shown in Figure 4.6, the gain of 1 is achieved by reversing the polarity of one of the capacitors. The capacitor C1 is charged and discharged between V_{in} and V_{out}, and the capacitor C2 is disconnected from the output in the gain phase so that the noise feeding back to the input is reduced. In the gain phase, by inspection, the voltage of C1 is

$$Vc1 = Vout - Vin \qquad (4.6)$$

Combining Equation (4.6) and (4.2) results in

$$\frac{Vout}{Vin} = Gsc = 1 \qquad (4.7)$$

The reason why only one of the two capacitors is used to implement the configuration with unit gain is that our circuit simulations show that one capacitor has enough capability to support the load current of the design specification. This saves a switch, which means saving a large chip area since the switches in the charge pump are very big.

4.5.3. Voltage Management Issue
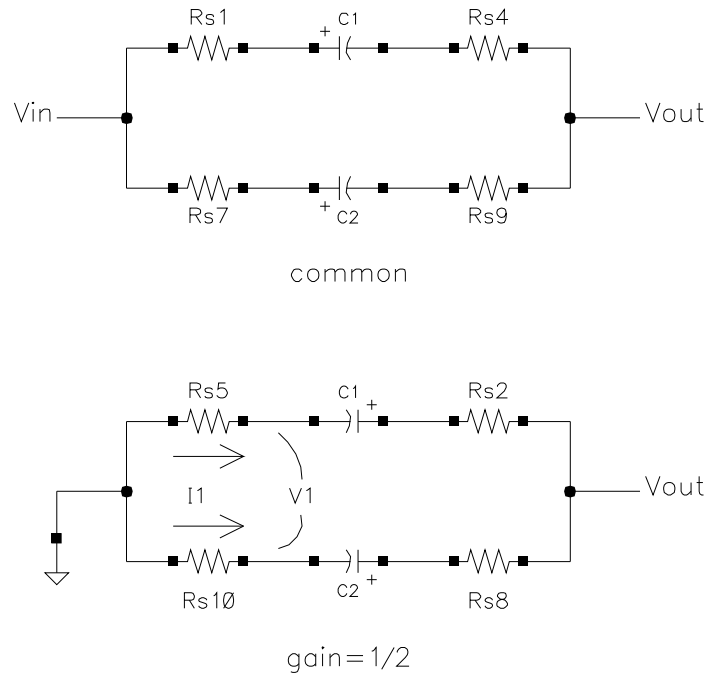
Figure 4.7 Configuration with gain of 1/2

For the application of our converter, there are a wide range of input and output voltages. When the switched capacitor array is switched between the common phase and gain phases, the voltages produced at some nodes in the switched capacitor circuit may fall outside a desired range and cause a large substrate current. To illustrate this problem, the configuration with gain of 1/2 is redrawn in Figure 4.7, in which the resistors represent the switch on-resistances.

By inspection of Figure 4.7, if V_{in}=5.5V and V_{out}=1.8V, the capacitors C1 and C2 are full charged to 3.7V in the common phase. When the switched capacitors array is switched from the common phase to the gain phase, it is possible that the voltage V1 will momentarily be at –1.9V before the discharge takes place. Since the switches S5 and S10 are NMOS transistors and 1.9V is more than a forward biased PN junction voltage drop of 0.7V, a large substrate current will be caused.

To solve this problem, the circuit of the switched capacitor array must be designed to satisfy the following two voltage management rules.

(1) No voltage in the switched capacitor array may exceed the greater of V_{in} by more than a forward biased PN junction voltage drop.

(2) No voltage in the switched capacitor array may fall below the ground by more than a forward biased PN junction voltage drop.

Usually, the forward biased PN junction voltage drop is assumed to be 0.7V. However, considering that the forward biasing voltage varies with temperature and process, 0.25V is set as the target value for the junction drop in our design.

To meet the voltage management rules given above, two techniques are used in our design. These are described below.

(1) Phase-shifted clock

As the switches are closed, rather than close them at the same time, some of them are closed first, followed by the closure of the others.

The relative closure timing of the switches is controlled by four phase-shifted clocks, not just two non-overlapping clocks [2]. The waveforms of the four phase-shifted clocks are shown in Figure 4.8.
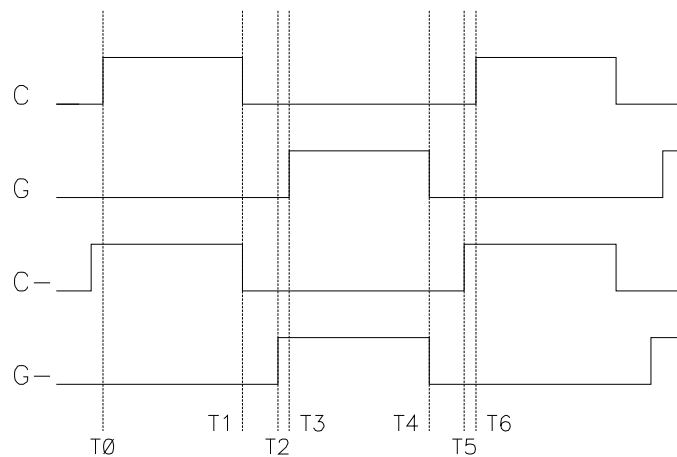

Figure 4.8 Waveform of four phase clocks

In our design, the clock frequency is 1 Megahertz. Clock C and clock G are two normal non-overlapping clocks, with clock C being high for 420 nanoseconds (T0 to T1), and with clock G being high for 420 nanoseconds (T3 to T4). The non-overlapping time period (T1 to T3 and T4 to T6) between clock C and clock G is 80

nanoseconds. Clock C– and clock G– are the advanced clocks. Their rising edge is advanced 20 nanoseconds with respect to clock C and clock G (T2 to T3 and T5 to T6), respectively. So the non-overlapping time periods of clock C and clock G– (T1 to T2) and clock G and clock C– (T4 to T5) are reduced from 80 nanoseconds to 60 nanoseconds.

Switch States (0=off; 1=on; C=common, G=gain)			
Switches	Gain Configuration		
	1/2	2/3	1
S1	C–	C–	C–
S2	G	G–	G–
S3	0	0	G
S4	C	C	C
S5	G–	0	0
S6	0	G	0
S7	C–	C–	1
S8	G	0	0
S9	C	C	C
S10	G–	G–	0

Table 4.4 Switch gate clocks in different gain configurations

The switch gate clocks of the three gain configurations are shown in Table 4.4. For example, in the gain configuration of 1/2, the closure of S5 and S10 is controlled by the advanced clock G– at time T2, and the closure of S2 and S8 is controlled by clock G at time T3. So, in the gain phase of the gain of 1/2, rather than close the switches S5, S10, S2 and S8 at the same time, switches S5 and S10 are closed first, followed by the closure of S2 and S8. This method causes the node voltage V1 be tied to the ground (0V) effectively, thereby limiting the ability of V1 to go below zero.

(2) Proportioning switch on-resistance

Although controlling the relative closure timing of selected switches will significantly reduce the instantaneous node voltages in the switched capacitor array, the voltage level may still not meet the voltage management rules. Returning to the example shown in Figure 4.7, when the capacitors C1 and C2 are discharged in the gain phase, there is an initial current I1 from the ground to the output, and the voltage V1 can be represented by the following equation:

$$V1 = -I1 * Rs5 \text{ or } V1 = -I1 * Rs10 \tag{4.8}$$

After the closure of S5 and S10, and prior to closure of switches S2 and S8, the switches S5 and S10 are low impedance and the switches S2 and S8 are very high impedance. So, the voltage that drops across S5 and S2 drops mainly across S2. When the switch S2 is closed, the magnitude of the initial current I1 is inversely proportional

to R_{S2}, the switch on-resistance of S2. The same thing happens to the switches S10 and S8. Considering Equation (4.8), V1 is proportional to $\dfrac{Rs5}{Rs2}$ or $\dfrac{Rs10}{Rs8}$. Thus, V1 can be minimized by proportioning the two switch on-resistances as given below:

$$R_{S5} \ll R_{S2} \text{ and } R_{S10} \ll R_{S8}.$$

4.5.4. Simulation for Metal Resistance

For the transistors used as switches in the switched capacitor array, the ratio of the gate width to the gate length $\dfrac{W}{L}$ is very large, so the switch on-resistances are very small [2][3]. Typically their values are about 1 ohm, which is comparable to the metal resistance of wires connected to the switches. Actually, it is possible that the metal resistance is greater than the switch on-resistance. Thus, the metal resistances have to be considered when designing the switched capacitor array.
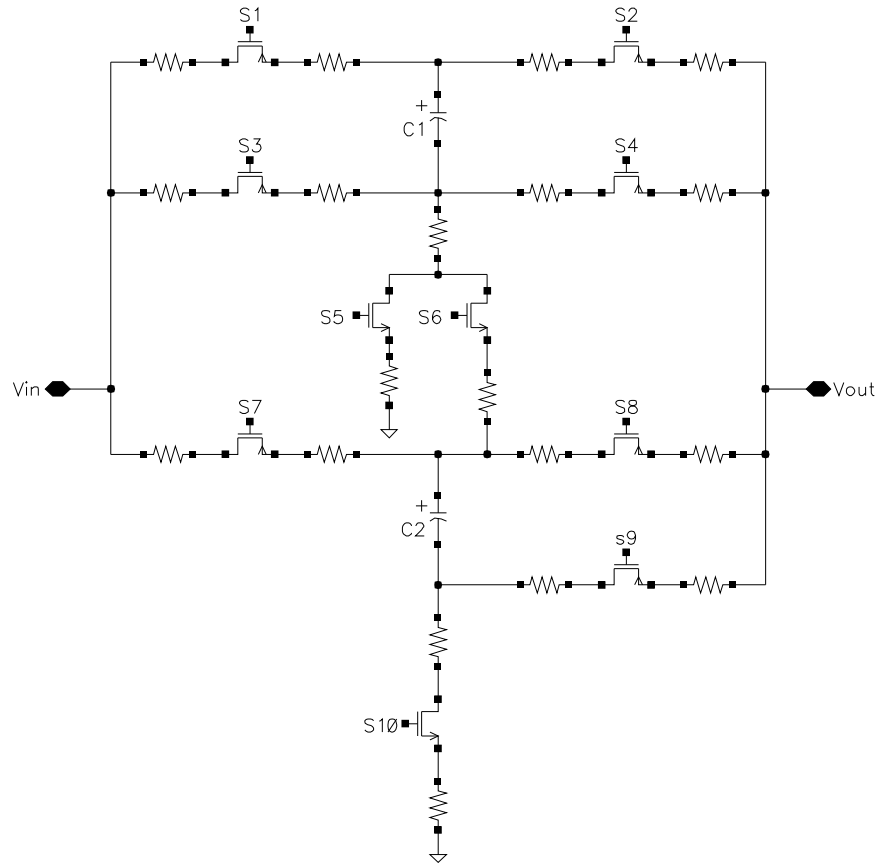
Figure 4.9 Switched capacitor array with metal resistance

Although the exact metal resistance value of each wire is unknown before the layout of the switched capacitor array is done, an estimated value can be used for simulations at the beginning of design. As shown in Figure 4.9, the resistors connected to the nodes of transistors are used for the simulation for the wire metal resistance.

In our design, before the layout is done, all the metal resistances have the same estimated values, 100 mΩ. After the layout of the switched capacitor array is done, the more accurate value of metal resistances can be estimated from the layout. These new values are used to replace the old ones to re-simulate the circuits. The circuits and layout may be redesigned for several times until all the specs and voltage management rules are met.

4.6. Circuit Design and Simulation

The circuit of the converter was implemented in a 0.5μm CMOS process through National Semiconductor Corporation. In our design, first, all the circuits were designed for a fixed output 1.8V, and then, the circuits were changed for the output options 1.5V and 2.0V. Actually, the change in the circuits is only the ratio of resistors in the two resistor strings connected to the output and the input, which are used to produce the desired output voltage and hopping voltage.

The circuit simulation of the whole chip takes a lot of time, so it was impossible for the simulations to cover all the process corners, since the time for our design was limited. The strategy of our simulations was running simulations with the typical process model and room temperature for a higher load current than the specification. For example, the load current in the specification is 200mA. In our

simulations, 240mA load current with typical process model and room temperature was used to check if the circuit works.

For the converter with the output voltage 1.8V, Figure 4.10, Figure 4.11 and Figure 4.12 show the simulation results for load currents 10mA, 120mA and 240mA, respectively. The x-axis represents the input voltages 2.7V to 5.5V.

The top plot in each figure shows gain settings at different input voltages. The numbers 1, 2 and 3 in y-axis denote the gain of 1/2, 2/3 and 1, respectively. For example, in Figure 4.10, the gain settings of the converter are number 2 and number 3 when the input voltage is from 2.7V to 2.9V. This means that the gain of the converter hops between the gain of 2/3 and 1 when the input voltage is 2.7V to 2.9V.

The second plot shows the average output voltage and the third plot shows the output ripple, which is a maximum peak-peak value of output voltage. By inspection of Figure 4.10, 4.11 and 4.12, the total output voltage variation is less than 50mV, i.e. 2.8%.

The bottom plot shows the conversion efficiency, which is calculated from simulation results by the equation below:
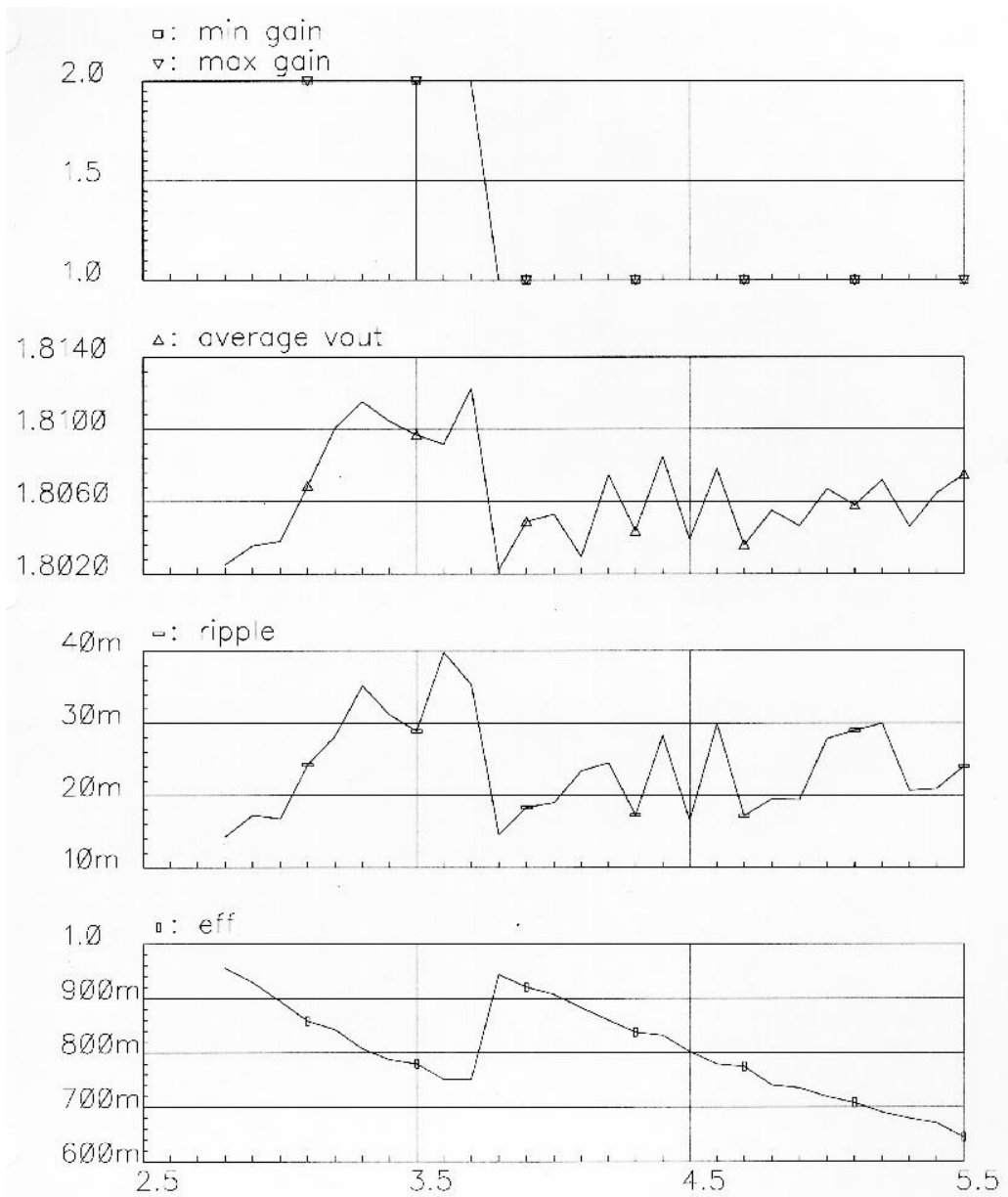
$$Eff = \frac{Vout * Iout}{Vin * Iin} \tag{4.9}$$

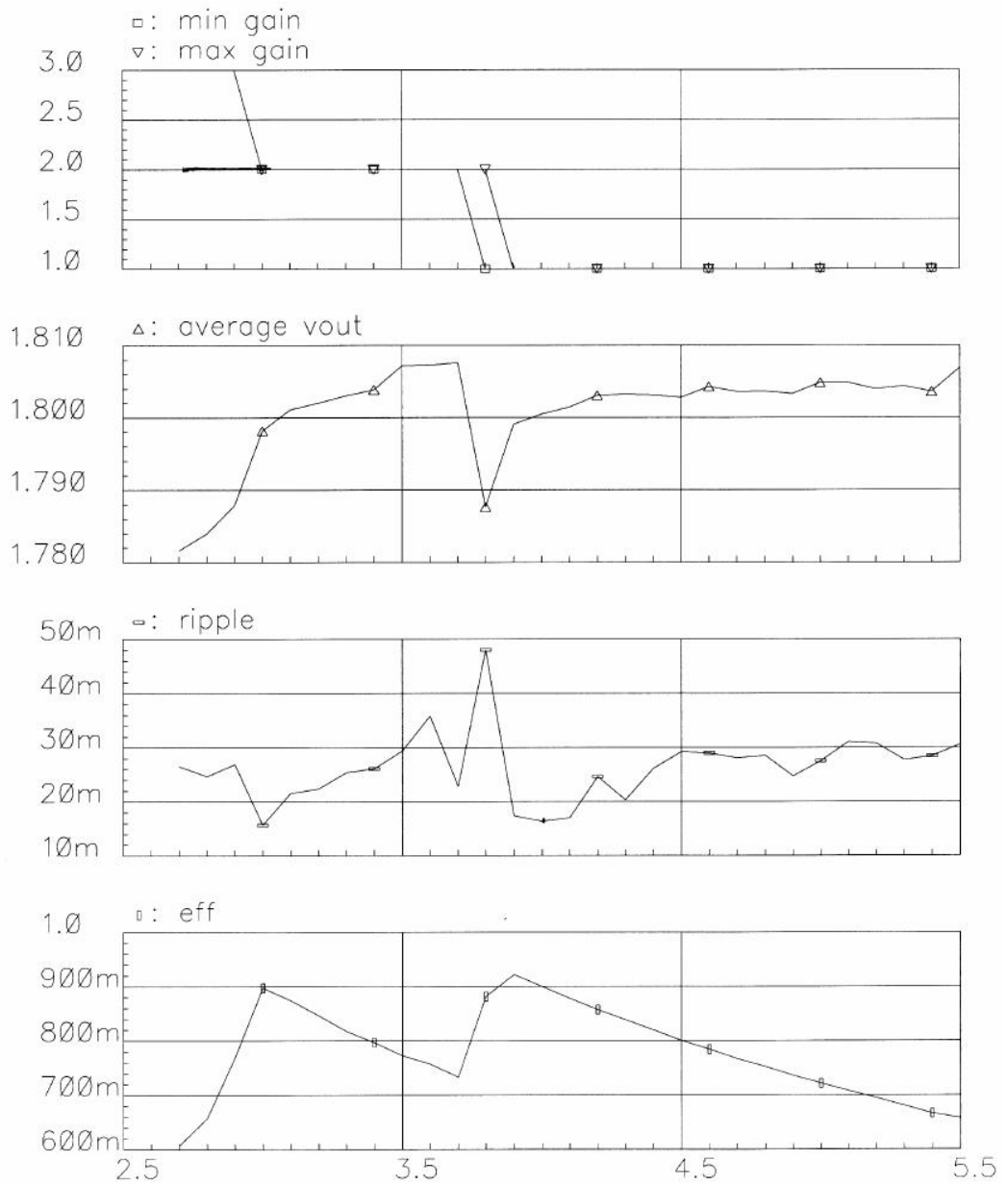Figure 4.10. Simulation results for V_{out}=1.8V and I_{load}=10mA

Figure 4.11. Simulation results for V_{out}=1.8V and I_{load}=120mA
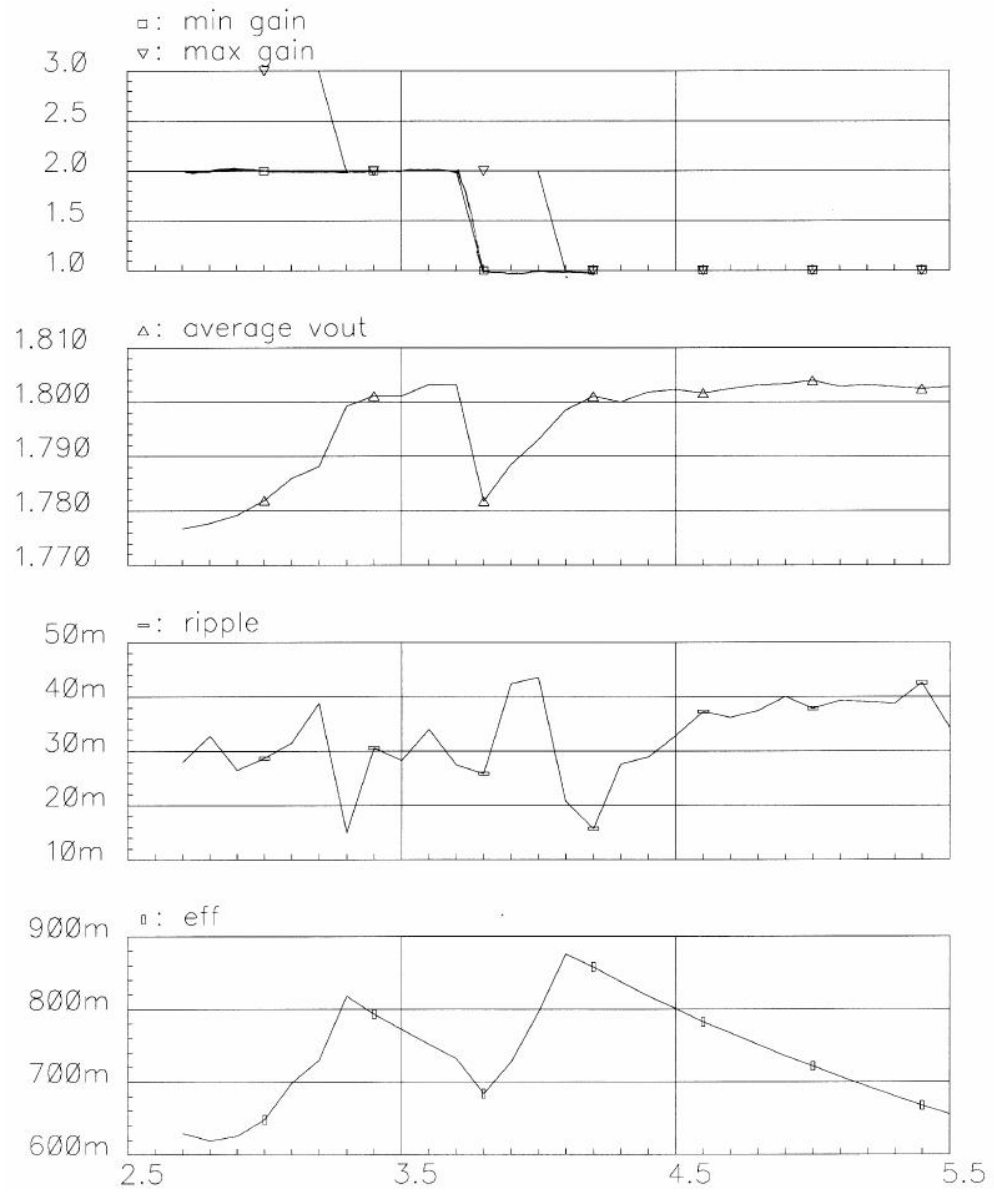
Figure 4.12. Simulation results for V_{out}=1.8V, I_{load}=240mA

In order to compare the efficiency of simulations with the theoretical value

from Equation (3.1) $Eff = \dfrac{Vout}{Gain * Vin}$, the theoretical efficiency for V_{out}=1.8V and

I_{load}=240mA without gain hopping is calculated and plotted in Figure 4.13 below.
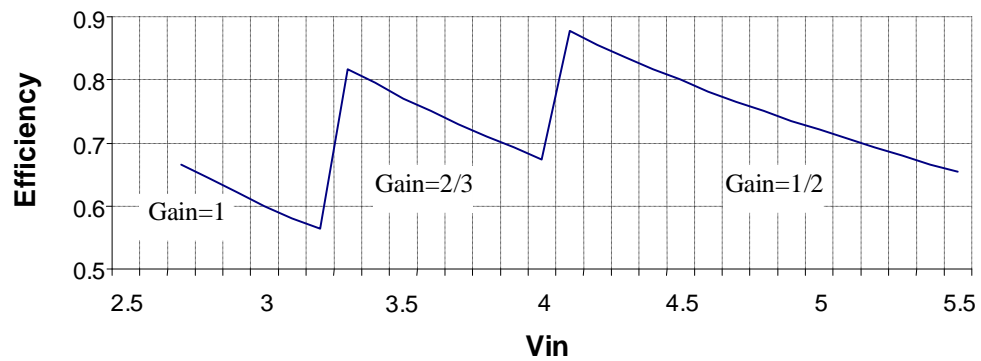

Figure 4.13. Theoretical efficiency for V_{out}=1.8V and I_{load}=240mA

Comparing Figure 4.12 and Figure 4.13, when the input voltage is 3.0V to

3.7V or 4.1V to 5.5V, the converter works without gain hopping and the efficiency of

the simulation is the same as the theoretical value. This result shows that the circuits

of our converter work fine. When the input voltage is 2.7V to 3.0V or 3.8V to 4.0V,

the converter works with gain hopping and the efficiency of the simulation are better

than the theoretical value at most of the input voltages. This shows that gain hopping

can improve the efficiency. However, at the input voltage 2.7V and 3.8V, the

efficiency of the simulation is a little lower than the theoretical value. This is because that some charges flow back to the switched capacitor array from the output when the gain hops at these input voltages.

More simulation results for the output options 1.5V and 2.0V with load current 240mA are shown in Figure 4.14 and Figure 4.15, respectively.
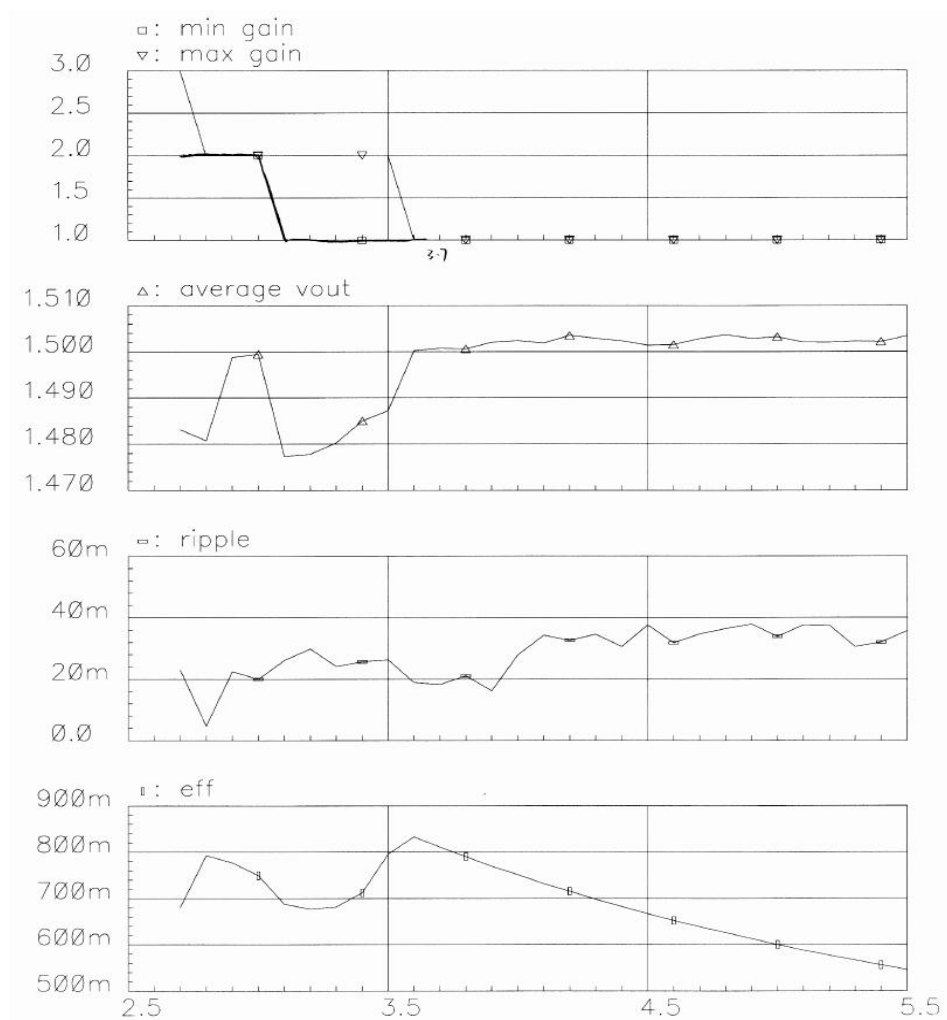

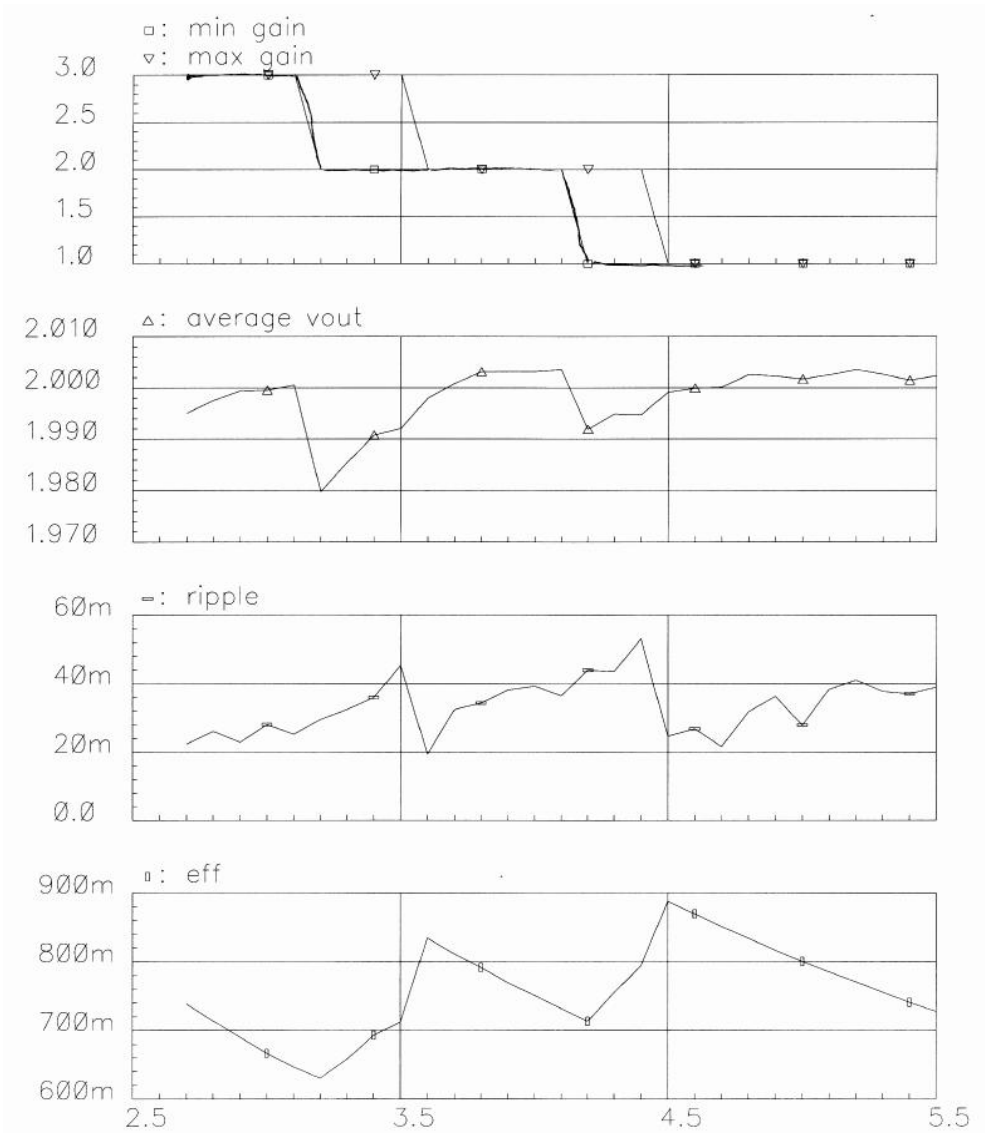Figure 4.14. Simulation results for V_{out}=1.5V and I_{load}=240mA

Figure 4.15. Simulation results for $V_{out}=2.0V$ and $I_{load}=240mA$

Based on the simulation results, the performance parameters are summarized in Table 4.5 below.

Output Options	1.5V	1.8V	2.0V
Input Voltage	2.7V~5.5V	2.7V~5.5V	2.7V~5.5V
Load Capability	200mA	200mA	200mA
Variation of Average Output	1.48V~1.51V	1.78V~1.81V	1.98V~2.02V
Ripple of Output	40mV	50mV	50mV
Efficiency	55%~92%	62%~95%	62%~97%

Table 4.5. Date of performance

Figure 4.16 on the next page shows the layout of the complete circuit of the designed converter. This layout is designed by the power management group of National Semiconductor Corporation.
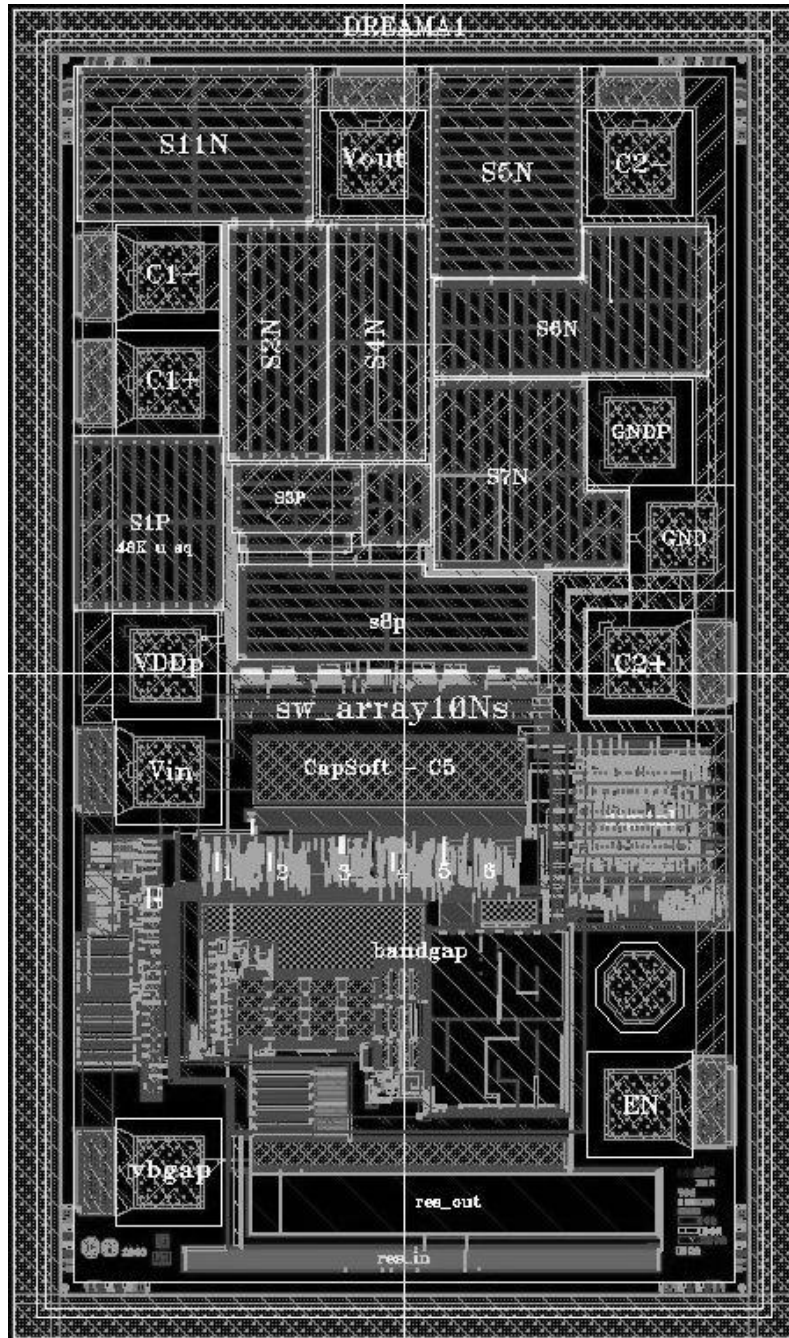
Figure 4.16. Layout of converter

5. INVESTIGATION FOR DESIGN OF A CONVERTER

WITH OUTPUT 1.2V

Based on the converter designed in Chapter 4, a DC/DC converter with the output 1.2V is designed in this chapter. A gain configuration with the gain of 1/3 is implemented with the switched capacitor array designed in Chapter 4 and the design issues are investigated.

5.1. Motivation

The power supply voltage of electronics devices is getting lower and lower. Although the converter designed in Chapter 4 covers the application with power supply voltage 1.5V, 1.8V and 2.0V, now is a time to look at how to design a DC/DC converter with a lower power supply voltage.

Based on the circuits already done in Chapter 4, a converter with the output voltage 1.2V and the input voltages 2.7V to 5.5V is designed. A new gain configuration with the gain of 1/3 is implemented to improve the conversion efficiency. Since this design is to investigate the design process and issues to accumulate design experience, there is no required specification for this converter.

5.2. Converter Architecture and Gain Mapping

The architecture of the converter with an output voltage 1.2V is the same as shown in Figure 4.1, and it also employs two important techniques, pulse frequency modulation (PFM) and gain hopping. The same switched capacitor array shown in Figure 4.5 is also used in this converter, but the gain configurations and the gain mapping are different from that of Chapter 4.

The gain regions are shown in Figure 5.1. There are two gain regions divided by the line $Vout = \frac{1}{3} * Vin$.
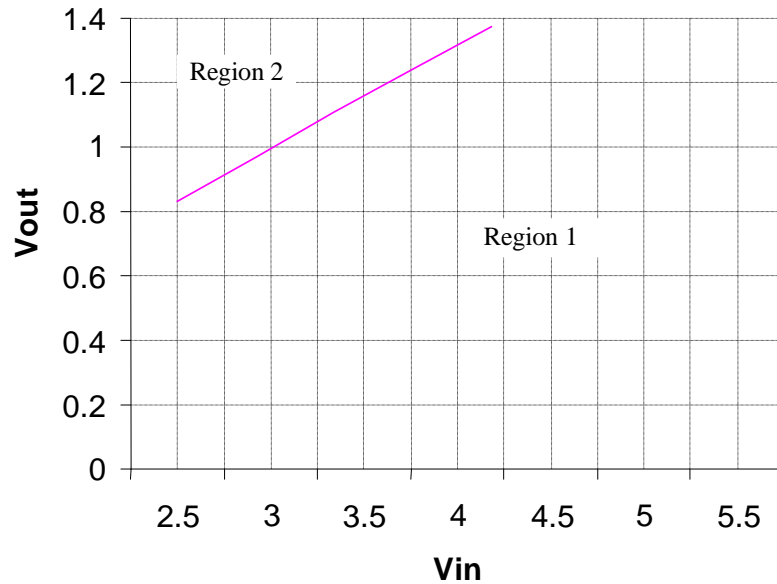

Figure 5.1. Gain regions

The gain mapping of each gain region is shown in Table 5.1. There are two gain configurations that can be chosen in each gain region. Compared to the converter in Chapter 4, this converter does not use the gain of 1 but a gain of 1/3. Gain hopping is also employed in this converter. When the required minimum gain G_{min} can not support the load current at the desired output voltage 1.2V, the converter will hop to a higher gain G_{max}. Since the output voltage of this converter is 1.2V, the hopping voltage is set to 1.18V. The gain control logic is shown in Table 5.2:

Gain Regions	G_{min}	G_{max}
1	1/3	1/2
2	1/2	2/3

Table 5.1. Gain mapping for gain regions

	$V_{out}>1.2V$	$1.18V<V_{out}<1.2V$	$V_{out}<1.18V$
Skip	high	low	low
Hop	low	low	high
Gain	G_{min}	G_{min}	G_{max}

Table 5.2. Gain control logic

5.3. Gain Configurations

Gain configurations in this converter are provided by the same switched capacitor array designed in Chapter 4 shown in Figure 4.5. However, the gate clocks of the switches are changed to provide different gain configurations. A new gain configuration with gain of 1/3 is shown in Figure 5.2.
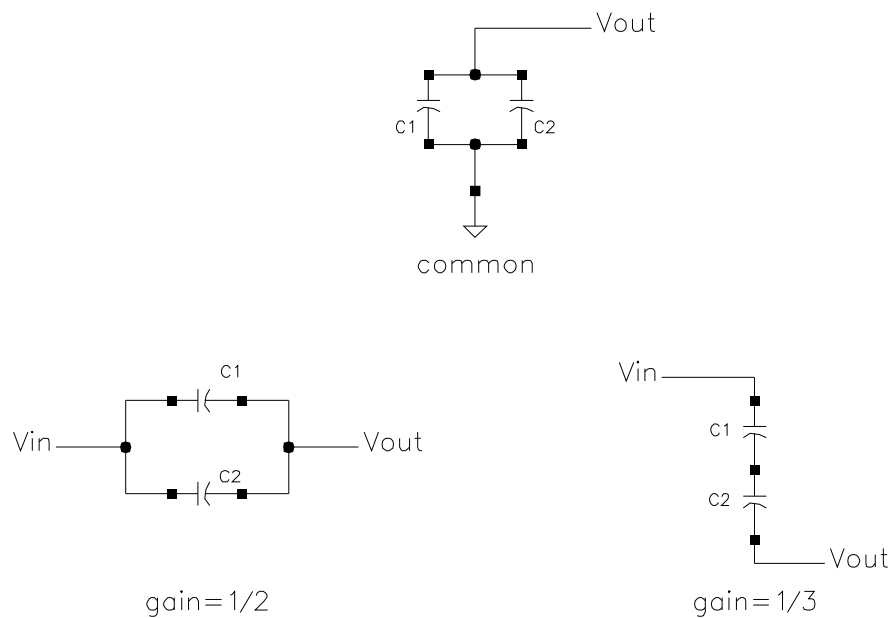

Figure 5.2. Gain configurations for gain region 1

Compared to the converter in Chapter 4, this converter has no single common phase which can be shared by all the three gain configurations with gains of 1/3, 1/2

and 2/3. So, two different common phases are used in the two different gain regions, respectively. In the gain region 1, one common phase, shown in Figure 5.2, is shared by the two gain configurations with gains of 1/3 and 1/2. In the gain region 2, the other common phase, shown in Figure 5.3, is shared by the two gain configurations with gains of 1/2 and 2/3.

As shown in Figure 5.2, the circuit of gain configuration of 1/2 is the same as that in Chapter 4, but the definition of gain phase and common phase are exchanged. In the common phase, both C1 and C2 are connected between the output and the ground. Actually, this common phase is the gain phase with a gain of 1/2 in the converter designed in Chapter 4.

As shown in Figure 5.2, for the gain of 1/3, it can be seen that the voltages of the capacitors C1 and C2 are equal to V_{out} in the common phase:

$$Vc1 = Vc2 = Vout \tag{5.1}$$

In the gain phase, by inspection, the voltages of the capacitors C1 and C2 are

$$Vc1 = Vc2 = \frac{1}{2} * (Vin - Vout) \tag{5.2}$$

Combining Equation (5.1) with (5.2) results in

$$\frac{Vout}{Vin} = Gsc = \frac{1}{3} \tag{5.3}$$

In the gain region 2 of Figure 5.1, the two gain configurations with gains of 1/2 and 2/3 are shown in Figure 5.3. The circuits and the phase definitions of these two configurations are the same as those of Chapter 4 shown in Figure 4.6.

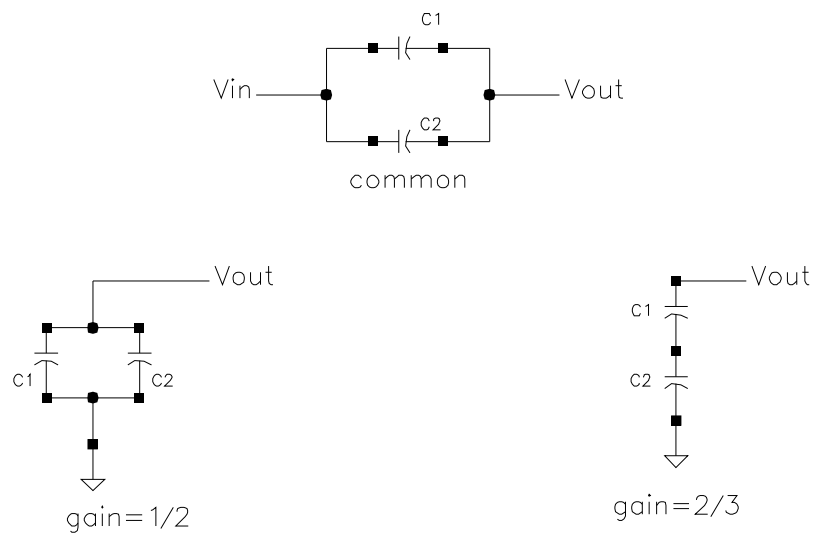

Figure 5.3. Gain configurations for gain region 2

Table 5.3 shows the switch states of different phases. As mentioned before, in this table, "1" means that the switch is on, i.e. closed, and "0" means that the switch is off, i.e. open.

Switch	Gain Region 1			Gain Region 2		
	Common Phase	Gain Phase		Common Phase	Gain Phase	
		1/3	1/2		1/2	2/3
S1	0	1	1	1	0	0
S2	1	0	0	0	1	1
S3	0	0	0	0	0	0
S4	0	0	1	1	0	0
S5	1	0	0	0	1	0
S6	0	1	0	0	0	1
S7	0	0	1	1	0	0
S8	1	0	0	0	1	0
S9	0	1	1	1	0	0
S10	1	0	0	0	1	1

Table 5.3 Switch states in different phases

To solve the voltage management problems in this converter, as mentioned in Chapter 4, the switches in the switched capacitors array are also controlled by four phase-shifted clocks C, C–, G and G–, shown in Figure 4.8. The gate clocks of switches in different gain configurations are shown in Table 5.4.

Switch Gate Clocks (0=off; 1=on; C, C- = common, G, G- =gain)				
Switch	Gain Region 1 Gain Configuration		Gain Region 2 Gain Configuration	
	1/3	1/2	1/2	2/3
S1	G–	G–	C–	C–
S2	C	C	G	G–
S3	1	1	0	0
S4	1	G	C	C
S5	C–	C–	G	0
S6	G	0	0	G
S7	1	G–	C–	C–
S8	C	C	G	0
S9	G–	G	C	C
S10	C–	C–	G–	G–

Table 5.4. Switch gate clocks of the gain configurations

5.4. Simulation Results

Based on the circuits designed in Chapter 4, the circuits of this converter were also implemented in a 0.5μm CMOS process through National Semiconductor Corporation. Some circuit simulation results are shown in Figure 5.4 below.
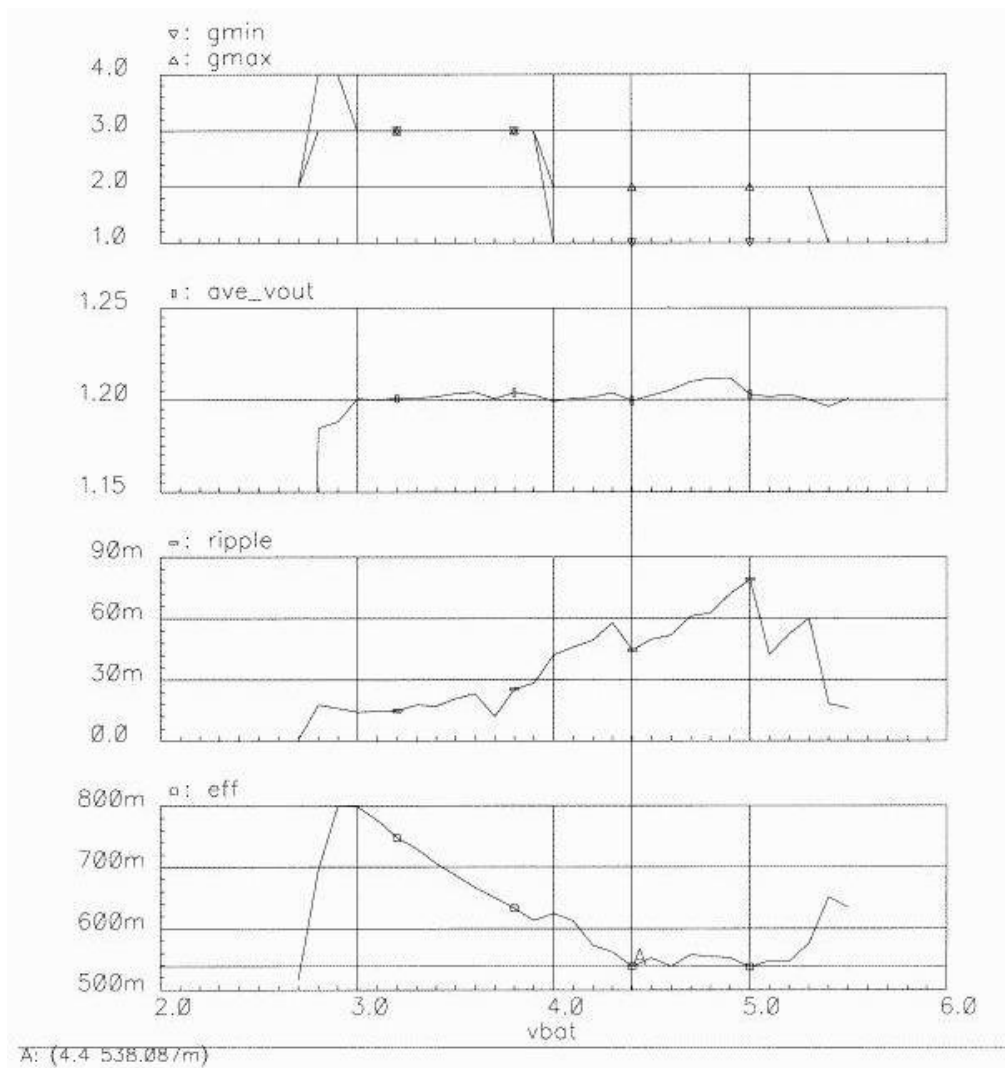

Figure 5.4. Simulation result for Vout=1.2V and I_{load}=120mA

The conditions of this simulation are listed below:

- Desired output voltage 1.2V

- Input voltage ranging from 2.7V to 5.5V

- load current 120mA

- Temperature 27°C

- Process model: typical

In Figure 5.4, the input voltage is shown in the x-axis. The top plot shows the gain settings used in the converter at different input voltages. In the y-axis, the number 1 and number 2 denote the gains of 1/3 and 1/2 in the gain region 1, respectively; and the number 3 and number 4 denote the gains of 1/2 and 2/3 in the gain region 2, respectively. The second plot shows the average output voltage. The third plot shows the ripple of output voltage. The bottom plot shows the conversion efficiency.

By inspection of Figure 5.4, it can be seen that the converter cannot support a 120mA load current when the input voltage is 2.7V, since the average output voltage drops a lot below the desired output voltage 1.2V. Considering the variation caused by temperature and process, a conservative estimate of the largest load current would be 100mA for input voltages 2.8V to 5.5V.
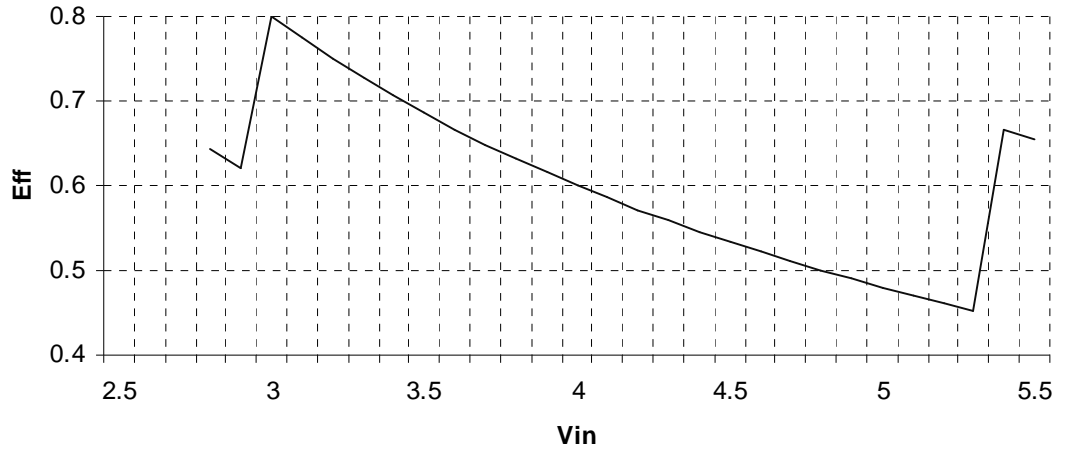
Figure 5.5. Theoretical efficiency for V_{out}=1.2V and I_{load}=120mA

The theoretical efficiency without gain hopping is calculated by Equation (3.1) as $Eff = \dfrac{Vdesired}{Gsc * Vin}$, and it is plotted in Figure 5.5. Comparing Figure 5.4 and 5.5, it can be seen that the gain hopping always increases the efficiency when the input voltage is 2.8V to 2.9V and 4.0V to 5.3V. When the input voltage is 3.0V to 3.9V and 5.4V to 5.5V, the converter works using a single gain, and the efficiency is the same as the theoretical value.

The performance parameters are listed in Table 5.5 below.

Input Voltage	2.8V~5.5V
Load Capability	100mA
Variation of Average Output	1.185V~1.215V
Ripple of Output	80mV
Efficiency	54%~80%

Table 5.5. Data of Performance of the converter with the output 1.2V

6. CONCLUSION

This thesis presented a switched capacitor array, which can be used to implement four gain configurations with gains of 1/3, 1/2, 2/3 and 1. Using this switched capacitor array, two step-down switched capacitor DC/DC converters were designed. One converter has the fixed output options 1.5V, 1.8V and 2.0V, and the other one has the output 1.2V. The circuit designs of the two converters were completed, and both of them were verified by the circuit-level simulations.

BIBLIOGRAPHY

[1]   J. Kotowski, W. J. McIntyre, J. P. Parry, United States Patent 6,055,168, Apr.25, 2000.

[2]   D. Johns, K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc. 1997.

[3]   P. R. Gray, P. J. Hurst, S. H. Lewis, R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, Inc. 2001.

[4]   A. Rao, "An efficient switched capacitor buck-boost voltage regulator using delta-sigma control loop", MS thesis, Oregon State University, Apr.29, 2002.