A Fully Digital Technique for the Estimation and Correction of the DAC Error in Multi-bit Delta Sigma ADCs.

by

Xuesheng Wang

A DISSERTATION

submitted to

Oregon State University

in partial fulfillment of
the requirement for the
degree of

Doctor of Philosophy

Completed December 1, 2003

Commencement June 2004

ACKNOWLEDGEMENTS

I wish to express my sincere appreciation to my major professor Dr. Gabor C. Temes. I have been very honored and privileged to have worked under his supervision. I have benefited greatly from his deep intuition for circuits and systems, from his emphasis on clarity in presentation, and from his insistence on high technical and professional standards.

I would like to thank my co-major professor Dr. Un-Ku Moon for making critical suggestions and comments throughout the course of my project, especially on the design of the test chip.

I also want to thank Prof. Kartikeya Mayaram, Prof. Huaping Liu, Prof. Zhongfeng Wang and Prof. Shoichi Kimura for serving in my committee.

Thanks to Jose' Silva for his helping on numerous technical problems in my project, and for he letting me reuse many of his drawings in this dissertation. Thanks also to Yuhua Guo, who designed and laid out the quantizer part of the test chip of this project.

I extend thanks to all my colleagues and ex-colleagues in analog and mixed signal circuits group. My earliest days in U.S. could have been much tougher if there was no generous and thoughtful help from Peter Kiss and Jipeng Li. I have benefited much from the discussion with Pavan Hanumolu, Gil-cho Ann and

Mustafa Keskin. The practical help that I received from Ying Xiao and Mengzhe Ma was significant.

I would like to thank Dr. Yunteng Huang at Silicon Labs for a fruitful summer internship.

Thanks to the NSF Center for Design of Analog and Digital Integrated Circuits (CDADIC) and Analog Devices Inc. for funding this project.

Finally, I am very grateful to my wife Huifen for her genuine care and understanding. And my heartfelt appreciation goes to my beloved parents and sister for their unconditional love and support throughout my life.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF FIGURES (Continued)

LIST OF TABLES

TABLE Page

A Fully Digital Technique for the Estimation and Correction of the DAC Error in Multi-bit Delta Sigma ADCs

Chapter 1 Introduction

Multi-bit delta sigma ADCs are designed to meet the requirement of high speed, high resolution conversions in contemporary applications. But the output error of the internal DAC can directly limit the overall performance of the ADC. The structure of the DAC error is indicated through a simple model for unit-element based DACs. The impact of the DAC error on the performance of ADC is then analyzed. Various techniques dealing with the DAC error are described and their drawbacks are pointed out. Based on the nature of the error and the surrounding signals, a fully digital method to estimate the error from the ADC output and remove it is proposed. Simulation results are shown to support the effectiveness of the method. Simulations also show that the proposed technique can work together with the technique of adaptive compensation for quantization noise leakage in cascaded delta sigma (MASH) ADC cases. These two techniques are the foundation for the design of high speed, high resolution delta sigma ADCs with relaxed requirements on the analog circuits.

To verify the proposed technique, an experimental MASH ADC was built, including the design and fabrication of a chip of a second-order multi-bit delta

sigma ADC in a 1.6μm CMOS technology. The measured results show that the proposed DAC correction technique is highly effective.

1.1 Motivation

Traditionally, delta sigma ADCs are used for low cost, high-resolution conversion of narrow-band signals, such as voice (0-3 kHz) and audio (0-20 kHz) signals [1] [2]. In such cases, a single-bit quantization is often preferred because of the theoretically perfect linearity of the quantizer and the feedback DAC. Although the total power of the quantization noise is large, with a large (>64) over-sample ratio (OSR) and noise shaping, the power remaining in the signal band can be shaped to drop under the desired level.

Nowadays, applications like video capture and xDSL require much broader signal bandwidth (several MHz) with high resolution. Because of their advantages such as high resolution, insensitivity to circuit non-idealities and low cost, delta sigma ADCs remain a strong candidate for such applications. But in these cases, large OSRs are unlikely to be practical because the circuits have to work too fast to be implementable. But with low OSRs, the noise shaping is weak. If high resolution is still desired, the in-band power of the quantization noise should be reduced by other means.

Naturally, delta sigma ADCs with multi-bit quantizers are considered. As a matter of fact, multi-bit quantizers help to improve the resolution in two ways.

First, of course, they reduce the total power as well as the in-band power of the quantization noise. Second, they improve the stability of delta sigma ADCs, thus more aggressive shaping can be adopted, again reducing the in-band quantization noise. So it is not surprising that multi-bit quantizers are used in many state-of-the-art delta sigma ADCs [3] [4] [5], even in some high quality audio ADCs [6].

1.2 DAC error in multi-bit delta sigma ADC

Nevertheless, the use of multi-bit quantizers causes a key problem: how to deal with the inherent nonlinearity of the feedback DAC. The nonlinearity can be seen as an additive error to the ideal output of the DAC. This error travels the same way as the input signal, thus may directly limit the overall resolution and linearity achievable by the ADC. For instance, if 15-bit resolution is expected from the ADC, the in-band power of the DAC error should be about 90dB below the power of a full scale signal. If a quantizer and a DAC with 5 bits are used, the RMS of the DAC error should be at least 54 dB below the V_{LSB} under an OSR of 4. That is not unachievable in the state-of-art technology but requires very careful layout and maybe special processes which add to the cost [3].

Various techniques have been proposed to deal with the DAC error. One extensively used technique is dynamic element matching (DEM). It is proposed for a very common DAC structure which is built from unit elements. Using DEM, the bits in the thermometer-coded output of the quantizer are rearranged following

certain rules by a digital process before it is inputted to the DAC. This rearrangement does not affect the data value, but it changes the priority on the selecting of the unit elements in the DAC, which can result in two effects. The first: the DAC error becomes uncorrelated with the DAC input, eliminating the signal dependent tones that will appear in the ADC output otherwise. The second, so-called mismatch shaping, is moving the error power from low frequencies to high frequencies. DEM has many versions of implementation [7] [8] [9], using different rules for bit rearranging. Some of them have both effects, some only have one.

Shaping can help to relieve the impact of the DAC error but only to a certain extent, because its result depends on the OSR. In very high speed conversions where the OSR may have to be pushed down to as low as 4, the error shaping from DEM is too weak for high resolution requirements.

In addition to DEM, other techniques have also been developed. Self-calibrated DACs continually calibrate their unit-elements with a reference element [10]. Extra circuitry is needed to make all unit elements adjustable and a fine reference is needed. A foreground calibration scheme runs built-in measurements during special clock cycles for calibration and gets the error information of the DAC [11]. After the ADC enters the normal operation, the error information is used to correct the ADC output in the digital domain. This scheme has to interrupt the normal operation from time to time for the sake of error measurements. People have modified the scheme into a background one [12]. But then a dual port DAC is

needed so the measurement can be carried on simultaneously with the normal operation. The digital correction technique of [13] needs an extra DAC unit element and a modified delta sigma loop which sacrifices some of the in-band dynamic range and increases the design difficulty.

1.3 Purpose of this work

The purpose of this research was to find a novel technique for the detection and correction of DAC error. The desired technique should have three major features. First, it should require no extra analog circuitry. Digital circuits have been enjoying the scaling down in both area and power with the application of more and more advanced technologies, while analog circuits benefit much less. Although analog circuits will always have their realm, it is the trend to let digital circuits take over more functions [14]. Second, the desired technique should run in the background. The reason has been pointed out before. Third, the desired technique should work under very low OSRs (as low as 4). This may be the most important feature because it meets the requirement of broadband conversions in contemporary applications, and will set the desired technique apart from the existing DEM techniques.

1.4 Dissertation structure

Chapter 2 serves as a background introduction to delta sigma ADCs. The concepts of quantization and signal to noise ratio (SNR) are briefly reviewed. The

effect of oversampling and the delta sigma modulation to the quantization noise is analyzed. The necessity of multi-bit quantization in delta sigma ADCs in the context of broadband, high resolution conversion is pointed out. Finally, the problems with the use of a multi-bit DAC are described.

Chapter 3 gives a model of the output error of a multi-bit DAC. Two effects of the error are shown through the model. The impact of the error on the overall performance of the ADC is analyzed. Various available techniques dealing with the DAC error are introduced and their drawbacks are pointed out. Finally, the target of this research is presented and the challenge is discussed.

Chapter 4 proposes a fully digital technique for the detection and estimation of the DAC error. The core of the proposed technique is a correlation operation. A scrambler is used to decorrelate the error and the input signal, followed by a corresponding post-processing. A high-pass filter is used to suppress the input signal in order to accelerate the correlation convergence. Simulation results are shown to verify the technique. The simulations are done with a MASH ADC with a multi-bit delta sigma ADC as its first stage. So the principle of MASH ADCs is introduced.

Chapter 5 reviews an adaptive compensation technique dealing with the noise leakage in MASH ADCs. A MASH ADC is simulated with the DAC correction and the adaptive compensation both applied. Results show that the two

can work together, which paves the road to build high performance delta sigma ADCs with relaxed requirements on the analog circuits.

Chapter 6 shows an experimental system, including a second-order 3-bit delta sigma ADC with a low-distortion structure fabricated in a 1.6 μm CMOS technology. The system is basically a 2-0 MASH ADC, built to verify the proposed technique. The diagram of the whole system is presented, followed by the detailed circuit design of the second-order sigma delta ADC. Measurement results are also shown.

Chapter 7 summarizes the dissertation and plans for future work.

Chapter 2 Oversampling delta sigma ADCs: Background

Although the initial idea was brought up decades ago, delta sigma modulation had not become a popular technique in integrated circuit design until large-scale digital circuits were implementable on chip, because it involves a lot of digital signal processing [15] [16]. Based on the concepts of oversampling and noise shaping, trading speed for accuracy, delta sigma modulation makes it possible to achieve high-resolution data conversions with relatively coarse circuit components. Actually, delta sigma data converters dominate in low-cost, low-speed and high-resolution, high-linearity designs. But recent applications are demanding delta sigma converters for higher speed conversions, while allowing no loss in resolution. In this chapter, the basic principles of delta sigma modulation are reviewed, the reason to adopt multi-bit quantization is shown, and the problem arising from multi-bit quantization is briefly mentioned.

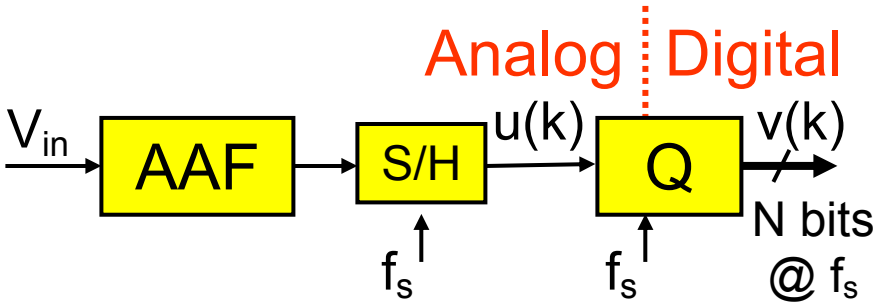


Figure 2-1 Analog-to-digital conversion.

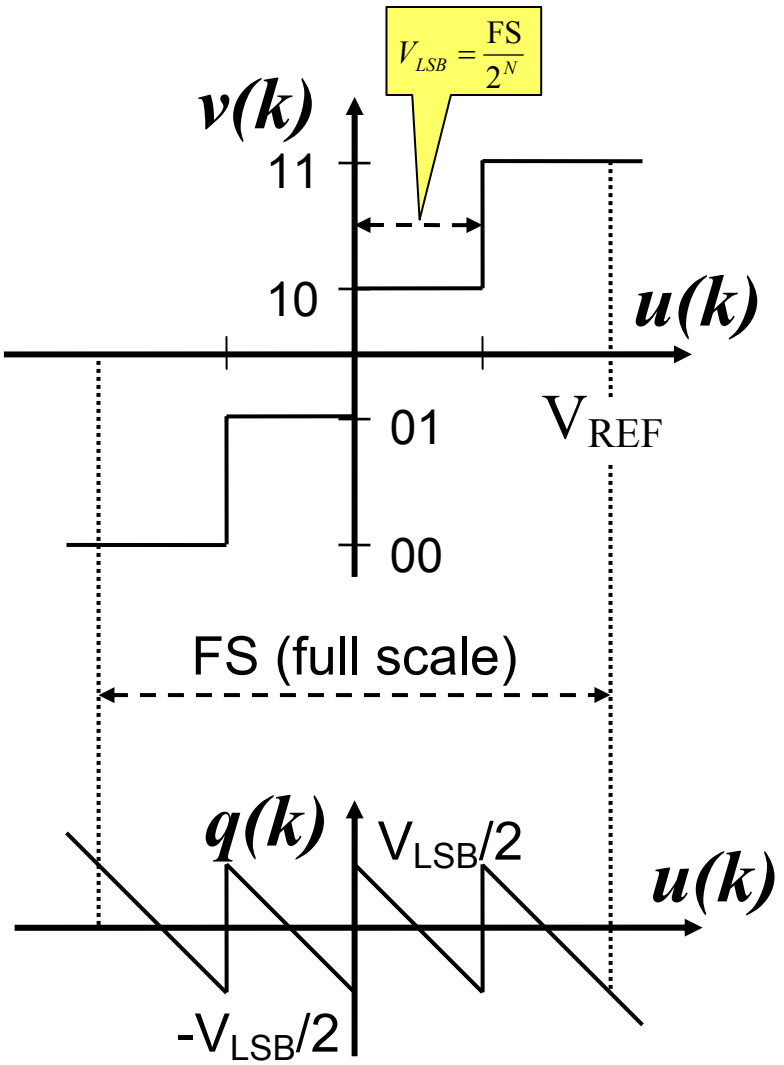


Figure 2-2 Quantization noise.

2.1 Sampling and quantization

Analog-to-digital conversion (See Figure 2-1) is a process to find a digital representation of the analog signal being converted. A digital signal is discrete in time and amplitude while an analog signal is continuous in both. So in a

conversion the analog signal usually needs to be sampled by a sample-and-hold (S/H) circuit. According to the sampling theorem[17], as long as an analog signal is sampled at a frequency f_s that is at least twice the signal bandwidth f_B, which is called Nyquist rate, the signal can be completely represented by and recoverable from the sampled values. On the other hand, any signal components that have frequencies higher than half of the sampling frequency f_s will cause aliasing during the sampling. So an anti-aliasing filter (AAF) is used to filter out those components first.

The sampled values $u(k)$, where k is an integer that represents time, need to be quantized before they can be made digital. In Figure 2-1, the block Q represents the quantizer. Quantization inevitably introduces an error, i.e., a noise. Figure 2-2 shows the transfer function of a quantizer and the relationship between the quantization noise and the input signal. It can be observed that the quantization noise $q(k)$ is evenly distributed between - V_{LSB} /2 and V_{LSB}/2 as long as the sampled values $u(k)$ are evenly distributed between $-V_{REF}$ and V_{REF}, where V_{LSB} is the quantization step and V_{REF} is the reference voltage. It can be calculated that the quantization noise $q(k)$ has a power of $V_{LSB}^2/12$ [15]. If the quantizer has N bits, which means the full scale is from $-2^{N-1}V_{LSB}$ to $2^{N-1}V_{LSB}$, a signal of a sine wave with the maximum amplitude that would not overload the quantizer has a power of $2^{2N-3}V_{LSB}^2$. Because the quantization noise is in the same band as the signal under a

sampling frequency equal to the Nyquist rate, the maximum signal to noise ratio (SNR) without consideration of other noise sources is $1.5 \cdot 2^{2N}$, which in dBs is

$$\mathrm{SNR}_{\mathrm{MAX}} = 6N + 1.76 \quad \text{(dB)}. \tag{2-1}$$

Another important assumption, often used in analyses and simulations of delta sigma modulations, is that the quantization noise is white in spectrum and is uncorrelated with the converted signal. The conditions under which this assumption holds are discussed in [15]. Figure 2-3 shows the power spectrum of the quantization noise under this assumption and under a sampling at Nyquist rate, which means $f_s/2=f_B$.

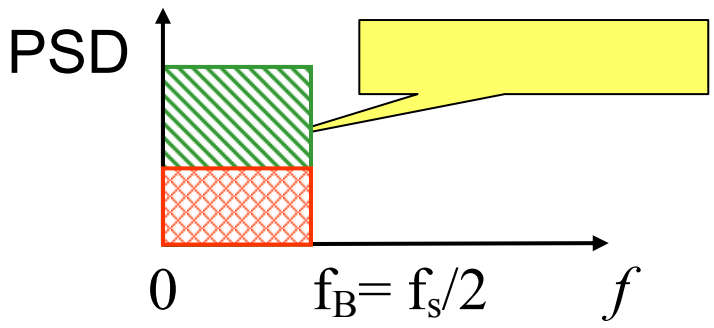


Figure 2-3 Quantization noise under Nyquist rate sampling.

2.2 Oversampling and noise shaping

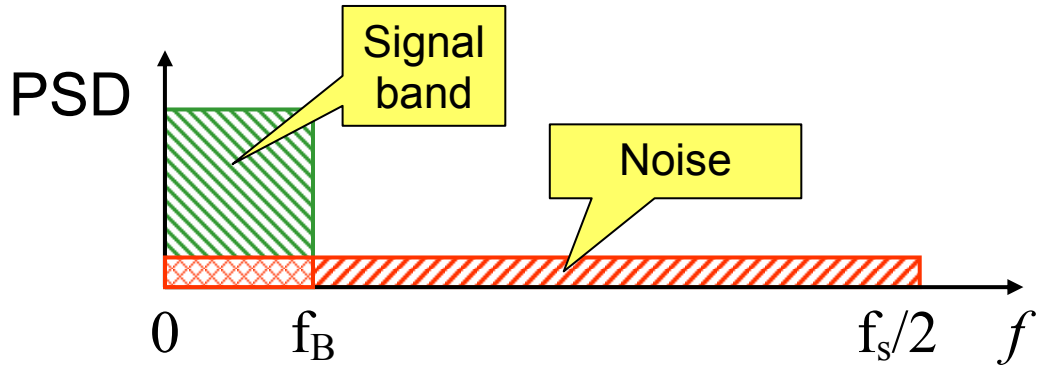


Figure 2-4 Quantization noise under oversampling.

The sampling frequency f_s can be increased beyond the Nyquist rate, which is called oversampling. Then the quantization noise $q(k)$ has a part of its power out of the signal band while the total power remains unchanged, as shown in Figure 2-4. When SNR is calculated, only the noise power in the signal band counts since the out-of-and noise can be removed by a post filter. So under the oversampling condition, the maximum SNR is improved compared to that under the Nyquist rate sampling. The ratio of the sampling frequency to the Nyquist rate is called the oversampling ratio (OSR). With the assumption that the quantization noise is white, the maximum SNR now becomes:

$$\mathrm{SNR}_{\mathrm{MAX}} = 6N + 1.76 + 20\log_{10} OSR\,(\mathrm{dB}), \qquad \textbf{(2-2)}$$

which means the SNR will be improved by 3 dB/octave with the increase of the OSR.

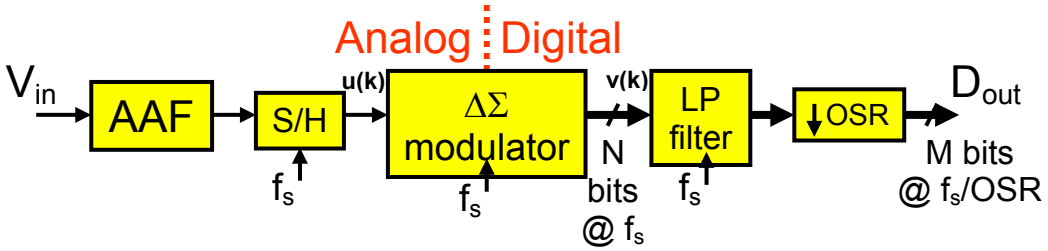


Figure 2-5 Oversampling delta sigma ADC.

A complete oversampling and noise-shaping delta sigma ADC is shown in Figure 2-5. Here the quantizer Q is not seen because it is a part of the delta sigma modulator. The delta sigma ADC works under the oversampling condition. Usually the digital output of the delta sigma modulator is processed by a decimation filter, which filters out the out-of-band noise and down-samples the output at the Nyquist rate. Because of oversampling, the requirement on the AAF is relaxed. The sample and hold circuit usually is integrated in the delta sigma modulator. The core of a delta sigma ADC is the modulator. For convenience, in the following part of this dissertation, the term "delta sigma ADC" only refers to the delta sigma modulator.

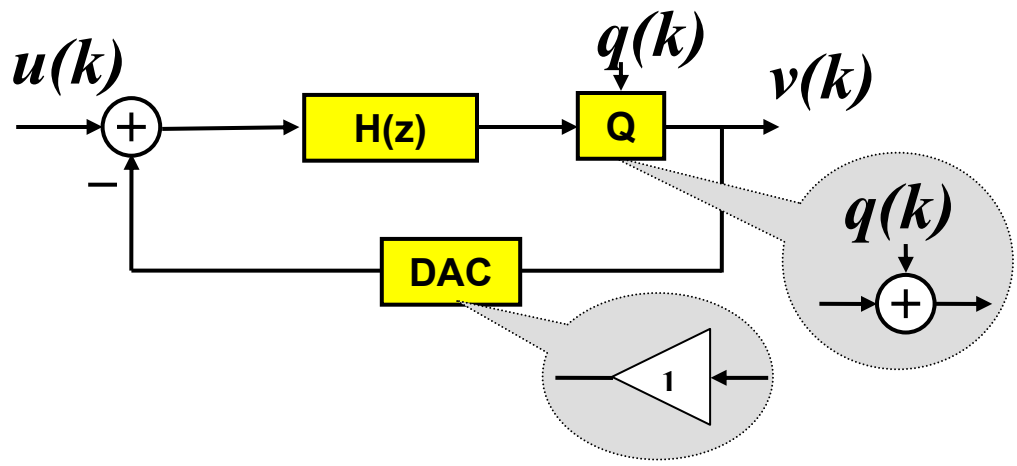


Figure 2-6 General diagram for delta sigma ADC (modulator)

In the delta sigma ADC, the quantizer Q is embedded in a delta sigma loop as in Figure 2-6, where the sampled values of the input signal, $u(k)$, no longer go into the quantizer Q directly. The quantizer output, which is also the output of the delta sigma ADC, is converted to the analog domain by a digital-to-analog converter (DAC) and fed back to the input. Ideally, the output step of the DAC equals to the quantization step of the quantizer. So the DAC is just a unity gain block. The quantization noise will pass through a noise transfer function (*NTF*) before appearing in the ADC output. The *NTF* is

$$NTF = \frac{V(z)}{Q(z)} = \frac{1}{1+H(z)}, \tag{2-3}$$

where $H(z)$ is a low-pass transfer function. In the simplest case, $H(z)$ is just a transfer function of an integrator:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}, \quad NTF = 1 - z^{-1}. \tag{2-4}$$

Then *NTF* has one zero at DC and the delta sigma ADC is first order.

Meanwhile, the sampled values, or the input signal $u(k)$ goes through a different signal transfer function (*STF*). Here,

$$\begin{aligned} STF &= \frac{V(z)}{Q(z)} = \frac{H(z)}{1 + H(z)} \\ &= z^{-1}, \text{when } H(z) = \frac{z^{-1}}{1 - z^{-1}} \end{aligned} \tag{2-5}$$

which is only a delay in the first-order case.

The ADC output is

$$v(k) = stf(k) * u(k) + ntf(k) * q(k), \tag{2-6}$$

where $stf(k)$ and $ntf(k)$ are the impulse response of *STF* and *NTF*. Here "*" denotes the discrete convolution. The output power spectrum is shown in Figure 2-7. It can be seen that the noise power at low frequencies, i.e., in the signal band[1], is attenuated while that at high frequencies is amplified. This effect is called *noise shaping*.

[1] In this dissertation, the signal band is always assumed to be at low frequencies starting from DC.

By changing the $H(z)$ and creating more zeros in the *NTF*, higher order delta sigma ADCs can be built, resulting in more effective noise shaping while still only causing delays to the signal.

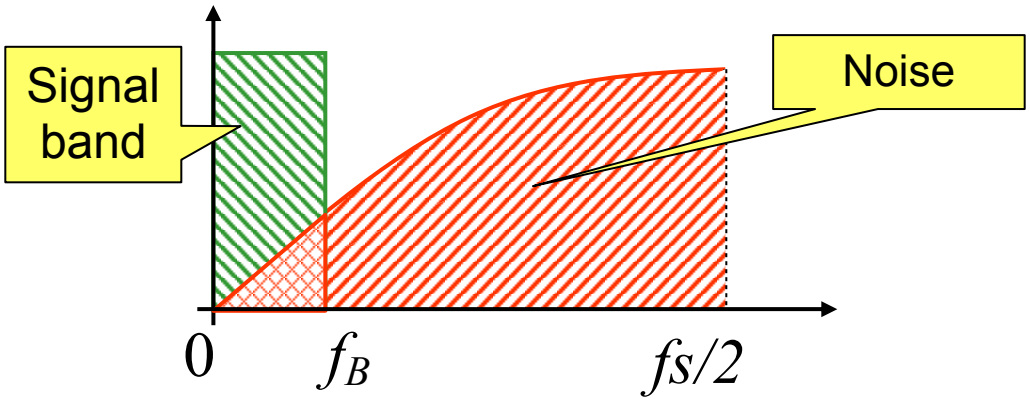


Figure 2-7 Quantization noise under oversampling and noise shaping.

Because of the quantization noise attenuation in the signal band, shaping improves the SNR under the oversampling condition. The out-of-band noise is filtered out by the decimation filter and is not folded into the signal band during the down-sampling. Assuming that OSR>>1, calculations indicate that the maximum SNR is now:

$$\mathrm{SNR}_{\mathrm{MAX}} = 6.02N + 1.76 + (20L + 10)\log_{10} OSR - 10\log_{10}\frac{\pi^{2L}}{2L+1}\ (\mathrm{dB}), \qquad \textbf{Eq. 2-7}$$

where L is the order of the delta sigma ADC. In the case of a second-order ADC, the SNR will be improved by 15 dB/octave with the increase of the OSR.

2.3 Single-bit vs. multi-bit quantization

Contemporary applications, such as xDSL and video capture, are requiring broad-band as well as high resolution conversions. High conversion resolution is the main feature of the delta sigma ADC. This makes it a potential candidate for such applications. There are three ways to achieve high resolution: a high OSR, a high-order loop and a multi-bit quantizer. Let us examine their feasibilities in the context of broadband conversions.

In traditional narrow-band designs, high OSRs are practical. In broad-band conversions, high OSRs are difficult to implement. For instance, to convert a signal with a bandwidth of 10 MHz using an OSR of 64, which is a typical number for delta sigma ADCs for audio applications, the clock driving the ADC needs to be at 1.28 GHz. If the ADC is to be implemented by switched capacitor circuits, the opamps have to have a unit-gain-bandwidth of at least 6.4GHz. This demands the use of advanced technologies and puts a lot of pressure on the power consumption.

Generally, without high OSRs, the advantage of high-order shaping becomes less obvious. Besides, a single-loop high-order ADC is difficult to design. Simply introducing more zeros to the NTF appears to lead to more attenuation of the in-band noise. But this is at the expense of more amplification of the out-of-band noise, which will finally overload the quantizer and cause instability. The

quantizer is essentially a nonlinear block, and its being embedded into a loop makes the analysis even more difficult. In practice, many simulations and experiments need to done to verify the high-order designs. Cascaded delta sigma ADCs can solve the problem. They will be discussed later.

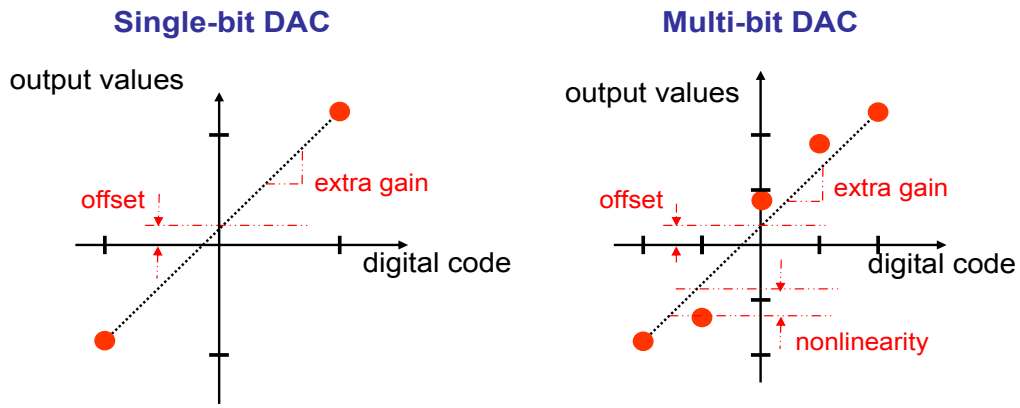


Figure 2-8 Linearity: a single-bit DAC vs. a multi-bit DAC.

Increasing the resolution of the quantizer lowers the total power of the quantization noise, which benefits the ADC resolution in two ways. First, it lowers the in-band noise power. Second, it allows more aggressive NTF before the ADC becomes instable, i.e., more attenuation of the in-band noise and more amplification of the out-of-band noise, which improves the SNR further.

Nevertheless, multi-bit quantizers do cause a problem. A single-bit quantizer goes with a single-bit DAC in the feedback path while a multi-bit quantizer goes with a multi-bit DAC. The error of the DAC is not shaped by the delta sigma loop and may directly limit the resolution and linearity of the ADC.

Fortunately, the error of a single-bit DAC can always be decomposed into an extra gain plus an offset, which usually do not significantly affect the ADC performance. In other words, a single-bit DAC has perfect linearity. But the error of a multi-bit DAC is not so simple and has the potential to seriously degrade the ADC performance. This will be analyzed in detail in next chapter.

Chapter 3 Error of multi-bit DAC and earlier techniques to deal with it

In this chapter, a model of the output error of the multi-bit DAC is first given. Based on the model, the impact of the error on the overall performance of the multi-bit delta sigma ADC is analyzed. Several existing techniques dealing with the DAC error are introduced. They fall into four categories: 1.) DAC error shaping; 2.) Self-calibrated DAC; 3.) Direct measurement of the unit element errors and digital correction; 4.) Detection or estimation of the DAC error and digital correction. The drawbacks of these techniques are pointed out. The motivation for a fully digital technique for the estimation and correction of the DAC error is indicated. Finally the challenge of inventing such a technique is evaluated.

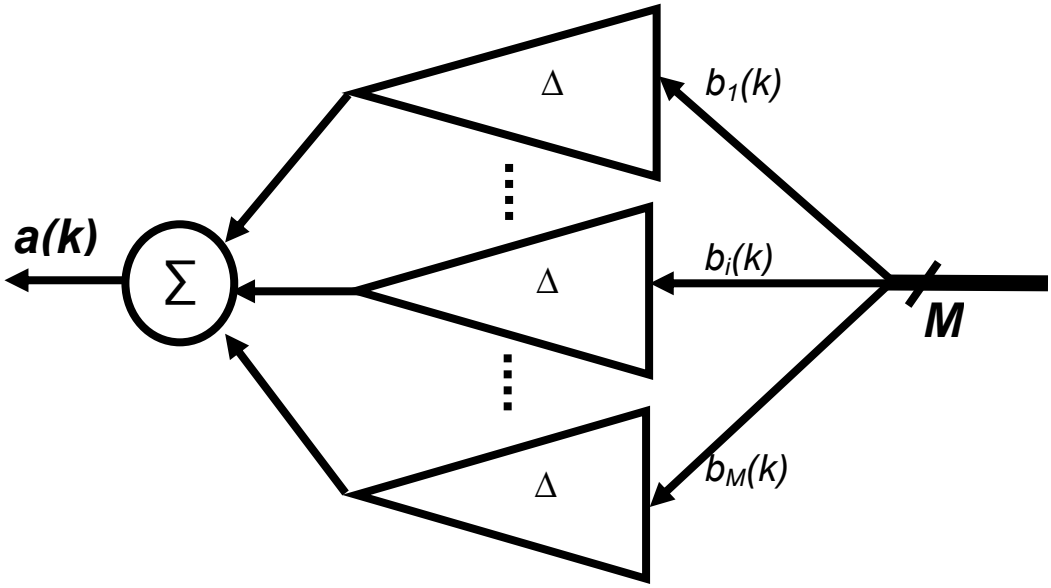


Figure 3-1 DAC structure built from unit elements.

3.1 Model of multi-bit unit-element based DAC

Although there are many structures to build a multi-bit DAC, the one built from unit elements is commonly used. All the discussions here are based on this kind of structure, which is shown in Figure 3-1.

A DAC with M+1 output levels consists of M unit elements, which output the same nominal value Δ when turned on. Δ equals the quantization step. The DAC input consists of the same number of bits as the number of the unit elements. Each unit element is controlled by one of the bits, $b_i(k)$ (i=1,2,…M). The $b_i(k)$=1 turns on (selects) and $b_i(k)$=0 turns off (deselects) the ith unit element at time k. $b_i(k)$ (i=1,2,…M) are referred to as **the selecting signals**. The output of the DAC is the sum of the outputs of all unit elements:

$$a_{ideal}(k) = \Delta \cdot \sum_{i=1}^{M} b_i(k). \quad \textbf{(3-1)}$$

At the circuit level, unit elements can be capacitors in a switched-capacitor DAC or they can be current sources in a current-steering DAC.

3.1.1 Extra gain and the DAC error

In practice, the outputs of the unit elements deviate from the nominal. The mean value of the unit-element outputs is unlikely to be exactly Δ. Suppose it equals $\alpha \cdot \Delta$, and individually the unit-element outputs are $\alpha \cdot \Delta \cdot (1+e_i)$ (i=1,2,…M). Here, e_i (i=1,2,…M) are the values of the normalized deviations of the unit-element outputs from their mean value, and they are referred to as **the unit-element errors**.

The output deviations of the unit elements have physical reasons behind them. In this research, only those reasons that are static or change much slower than the clock rate are considered, such as manufacturing variance of the components and drift effects due to environmental changes. So α and the unit-element errors are assumed to be constants. It is obvious that:

$$\sum_{i=1}^{M} e_i = 0. \qquad \textbf{(3-2)}$$

With the output deviations of the unit elements, the DAC output becomes:

$$a(k) = \alpha \cdot \Delta \cdot \sum_{i=1}^{M} b_i(k) + \alpha \cdot \Delta \cdot \sum_{i=1}^{M} \left[b_i(k) \cdot e_i \right]. \qquad \textbf{(3-3)}$$

Notice that the expression in **(3-3**) is artificially arranged so that an insight into the effects of the output deviations of the unit elements can be got. It can be observed that there are two changes compared to the ideal case in). First, α appears as an extra gain to the DAC. Second, an error (the second term at the right side of **(3-3**)) is introduced into the DAC output. It is a scaled mix of M signals, which are the unit-element errors modulated by their corresponding selecting signals. This term is referred to as **the DAC error**. A model including these two effects is shown in Figure 3-2.

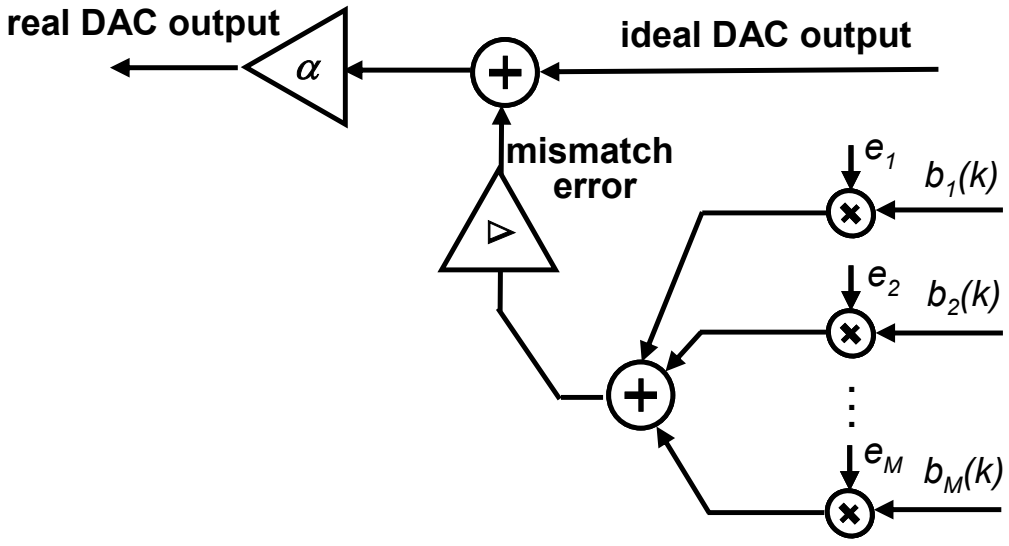


Figure 3-2 Model of effect of DAC error

3.1.2 Impact on the ADC output

In a multi-bit delta sigma ADC, the output of the quantizer is usually binary coded, which means different bits in the code have different weights. But a unit-element based DAC needs its input to be in a code where all the bits have the same weight. The thermometer code has this feature. So when the DAC is embedded into the delta sigma ADC, a binary-to-thermometer code converter (BTCC) is inserted between the quantizer and the DAC, as shown in Figure 3-3.

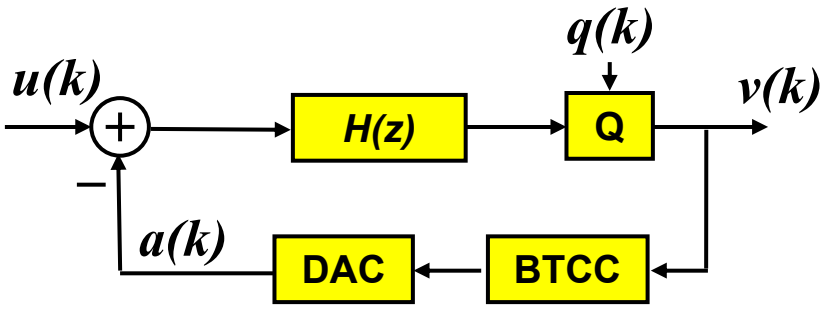


Figure 3-3 Multi-bit delta sigma ADC.

The model given in 3.1.1 is used to analyze the impact of the output deviations of the unit elements on the performance of the ADC in Figure 3-3. The ADC output is now:

$$v(k) = u'(k) + q'(k) + \sum_{i=1}^{M} [b_i'(k) \cdot e_i], \tag{3-4}$$

where

$$u'(k) = stf(k) * u(k),\ q'(k) = ntf(k) * q(k),\ b'_i(k) = etf(k) * b_i(k). \tag{3-5}$$

etf(*k*) is the impulse response of the error transfer function (*ETF*), which describes what the DAC error goes through before appearing in the ADC output. Note that

the quantization step Δ does not appear in the expression because it is cancelled by the factor of 1/Δ in the quantizer which is not shown.

In **(3-5)**, the *STF* and *NTF* are different from those in **(2-6)** due to the extra gain α:

$$STF = \frac{H}{1+\alpha \cdot H} = \left.\frac{z^{-1}}{1-(1-\alpha)\cdot z^{-1}}\right|_{\text{1st-order case}}, \qquad \textbf{(3-6)}$$

$$NTF = \frac{1}{1+\alpha \cdot H} = \left.\frac{1-z^{-1}}{1-(1-\alpha)\cdot z^{-1}}\right|_{\text{1st-order case}} \qquad \textbf{(3-7)}$$

Take the first-order case as an example. The pole of the *STF* is moved away from the origin, causing two effects to the amplitude frequency response of the *STF*, as shown in Figure 3-4. First, the DC gain of the *STF* becomes $1/\alpha$ instead of one. Fortunately, in most applications, this is acceptable. Second, the amplitude frequency response is no longer strictly flat in the signal band. Since $\alpha \ll 1$, the ripple is usually very small and negligible for most applications. The *NTF* has the same pole as the *STF*, but as shown in Figure 3-5, the amplitude frequency response of the *NTF* is even less affected by α than that of the *STF* is. Although only the first-order case is analyzed here, it can be easily verified that the extra gain α will not be a problem in the cases of higher orders either.

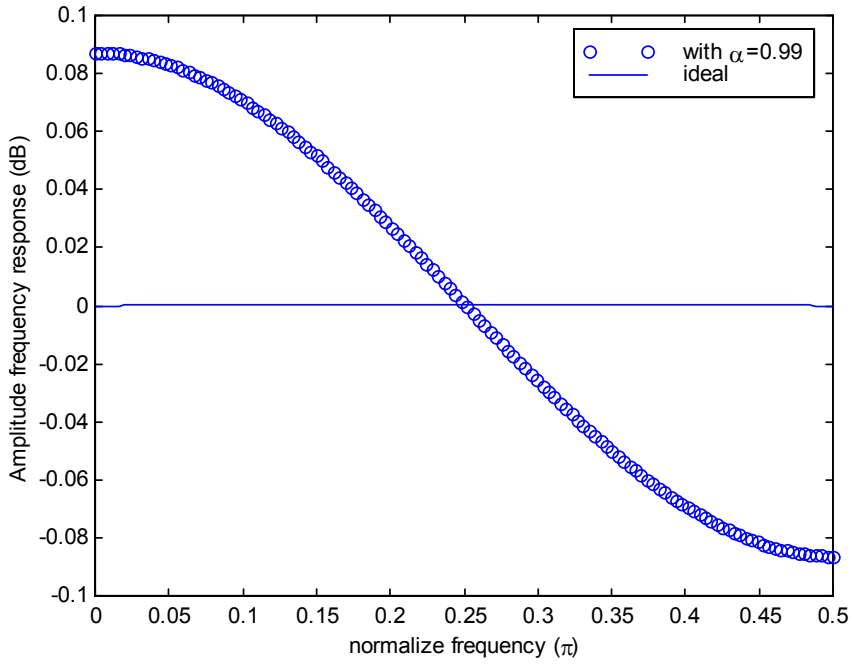


Figure 3-4 *STF* affected by α (α=0.99).

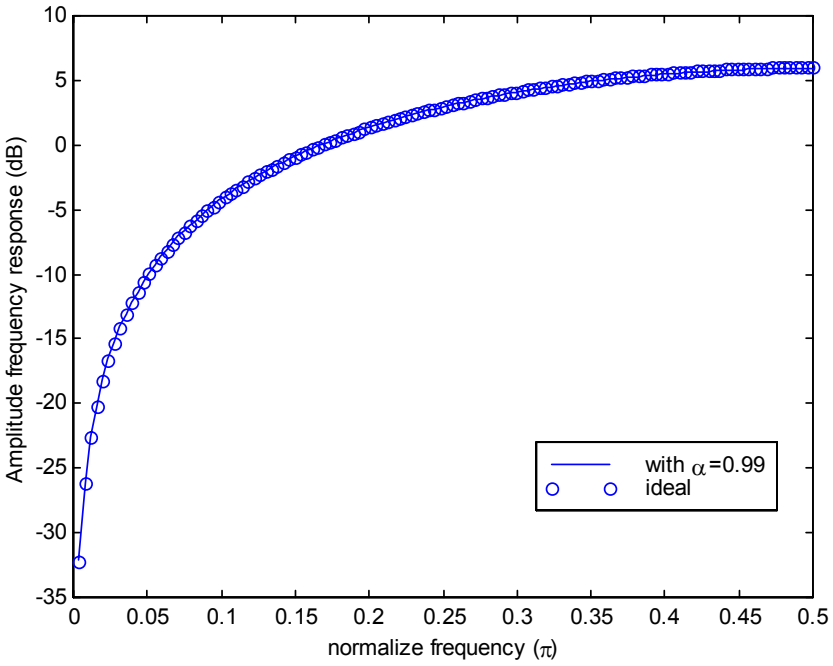


Figure 3-5 *NTF* under α=0.99.

In the circuit of Figure 3-3, the DAC error is filtered by the *ETF* when appearing in the ADC output, as shown in **(3-4**). Because here

$$ETF = STF, \qquad \textbf{(3-8)}$$

the DAC error is not shaped by the delta sigma loop like the quantization noise. So it directly limits the performance of the ADC. This is a serious problem with multi-bit delta sigma ADCs.

As mentioned in 3.1.1, the DAC error is the scaled mix of *M* signals, which are the unit-element errors modulated by the selecting signals. So the spectral

characteristic of the DAC error depends on two aspects: the amplitudes of the unit-element errors and the spectral characteristic of the selecting signals.

Note that the DAC model described in this section has not included the offset of the DAC because it has no significant effect on the ADC performance.

3.2 Dynamic element matching (DEM)

The multi-bit delta sigma ADC in Figure 3-3 suffers from an unfavorable DAC error. Table 3-1 shows an instance of the 8-bit thermo-meter coded input to the DAC, assuming that the DAC has 8 unit elements. Here k is the time, and $b_i(k)$ (i=1,2,…8) are the selecting signals. The bottom row in the table shows the input value at each time.

The problem with the thermometer code is that there is a fixed priority on the selection of unit elements. The one controlled by $b_1(k)$ always has the highest priority while the one controlled by $b_8(k)$ always has the lowest. This results in two effects. First, the selecting signals controlling the unit elements with highest or lowest priorities have large power at low frequencies, where the signal band is, which degrades the resolution of the ADC. Second, the selecting signals are strongly correlated to the DAC input, i.e. the ADC output, which contains the input signal. So the selecting signals contain input-signal-dependent tones, some of which are in the signal band and degrade the ADC linearity.

Table 3-1 Thermometer code input to the DAC.

	K=1	k=2	k=3	k=4	…
$B_1(k)$	1	1	1	1	…
$B_2(1)$	1	1	1	0	…
$B_3(k)$	1	0	1	0	…
$B_4(k)$	1	0	1	0	…
$B_5(k)$	0	0	1	0	…
$B_6(k)$	0	0	1	0	…
$B_7(k)$	0	0	0	0	…
$B_8(k)$	0	0	0	0	…
input value	4	2	6	1	…

Dynamic element matching (DEM) is a commonly used technique to deal with the DAC error. Between the thermometer-coded output of the quantizer and the input of the DAC a scrambler (SCR) is inserted. SCR is a digital rearranging process, as shown in Figure 3-6, where the BTCC is integrated with the SCR. In each clock period, SCR rearranges the bits in the thermometer code without changing its total value, so the priority of the unit-element selection becomes dynamic. Depending on the specific rearranging algorithm is used, DEM has different versions.

Table 3-2 Data weighted averaging (DWA).

	k=1	k=2	k=3	k=4	…
$B_1(k)$	1	0	1	0	…

$B_2(1)$	1	0	1	0	…
$B_3(k)$	1	0	1	0	…
$B_4(k)$	1	0	1	0	…
$B_5(k)$	0	1	0	1	…
$B_6(k)$	0	1	0	0	…
$B_7(k)$	0	0	1	0	…
$B_8(k)$	0	0	1	0	…
A(k)	4	2	6	1	…

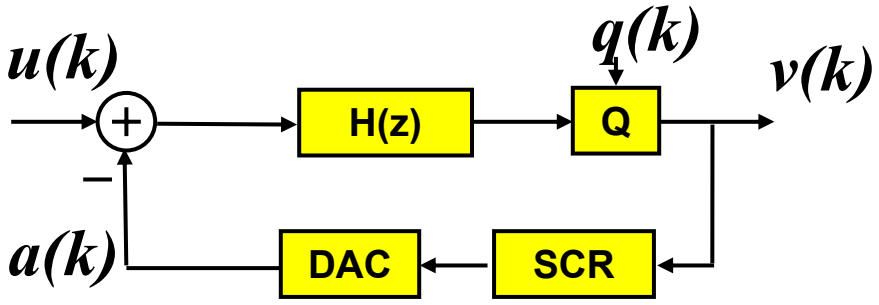


Figure 3-6 Delta sigma ADC with DEM.

Date weighted averaging (DWA) is a well known realization of DEM. Because of its simplicity and effectiveness, it is widely used. Table 3-2 shows the rearranging algorithm for DWA. DWA makes the unit-element selecting priority rotated, resulting in a first-order shaping of the selecting signals. The power of the DAC error is moved from low frequencies to high frequencies. But the signal-dependent tones are still there.

Table 3-3 Randomization

	k=1	k=2	k=3	k=4	…
$B_1(k)$	0	1	1	0	…
$B_2(1)$	1	0	0	1	…
$B_3(k)$	0	0	1	0	…
$B_4(k)$	1	0	1	0	…
$B_5(k)$	0	0	1	0	…
$B_6(k)$	1	1	0	0	…
$B_7(k)$	1	0	1	0	…
$B_8(k)$	0	0	1	0	…
A(k)	4	2	6	1	…

Zero-order randomization is another DEM technique. It rearranges the bits in the thermometer code randomly, similar to what is shown in Table 3-3. The selecting signals are decorrelated with the DAC input, which means they are decorrelated with the input signal, eliminating the signal-dependent tones in the DAC error. But since there is no shaping, the resolution of the ADC is still degraded by the error power in the signal band.

There are also many other versions of DEM. Some of them can achieve higher-order shaping of the DAC error, some of them mix randomization with shaping (which usually result in degraded shaping effect). As long as there is randomization involved, the signal-dependent tones can always be removed, resulting in good ADC linearity. But the degradation of resolution can only be solved conditionally because the total power of the DAC error is never reduced in

any versions of DEM. The effectiveness of the shaping depends on the amplitude of the unit element errors, the order of the shaping and the OSR. The unit element errors can be made small by using advanced processes, but at the expense of raised manufacturing costs. High-order shaping algorithms are difficult to design, and often complicated to implement. More important, under the circumstances of broadband conversion, high OSRs are not practical and the shaping will no longer be effective for high-resolution requirement with low OSRs.

3.3 Correction techniques

To get over the limitation of OSR, instead of manipulating the selecting signals and shaping the DAC error, correction techniques that reduce the amplitude of the unit element errors with circuit-level schemes have been proposed.

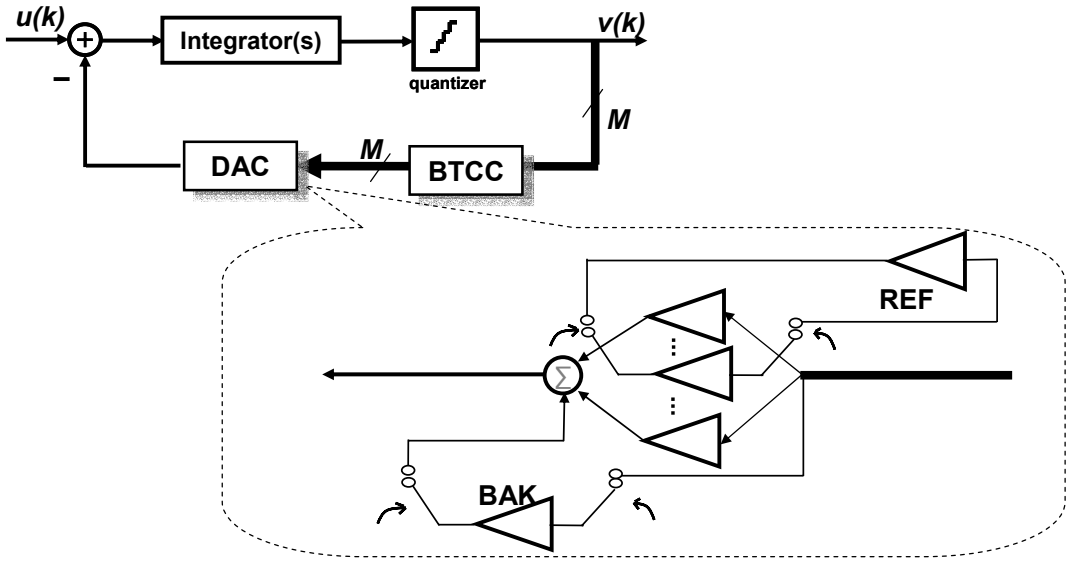


Figure 3-7 Self-calibrated DAC.

A self-calibrated DAC has been proposed in [10]. One at a time, the outputs of the unit elements are compared to that of a standard one, and based on the comparison results the unit elements are adjusted to compensate for the deviation. An extra unit element acts as a backup to the one that is currently being calibrated, as shown in Figure 3-7. This calibration process runs in the background throughout the time when the system is on. Simulations show that it is very effective on improving the accuracy of the unit elements. But extra analog circuitry has to be added in each unit element to make it adjustable and two extra unit elements are required.

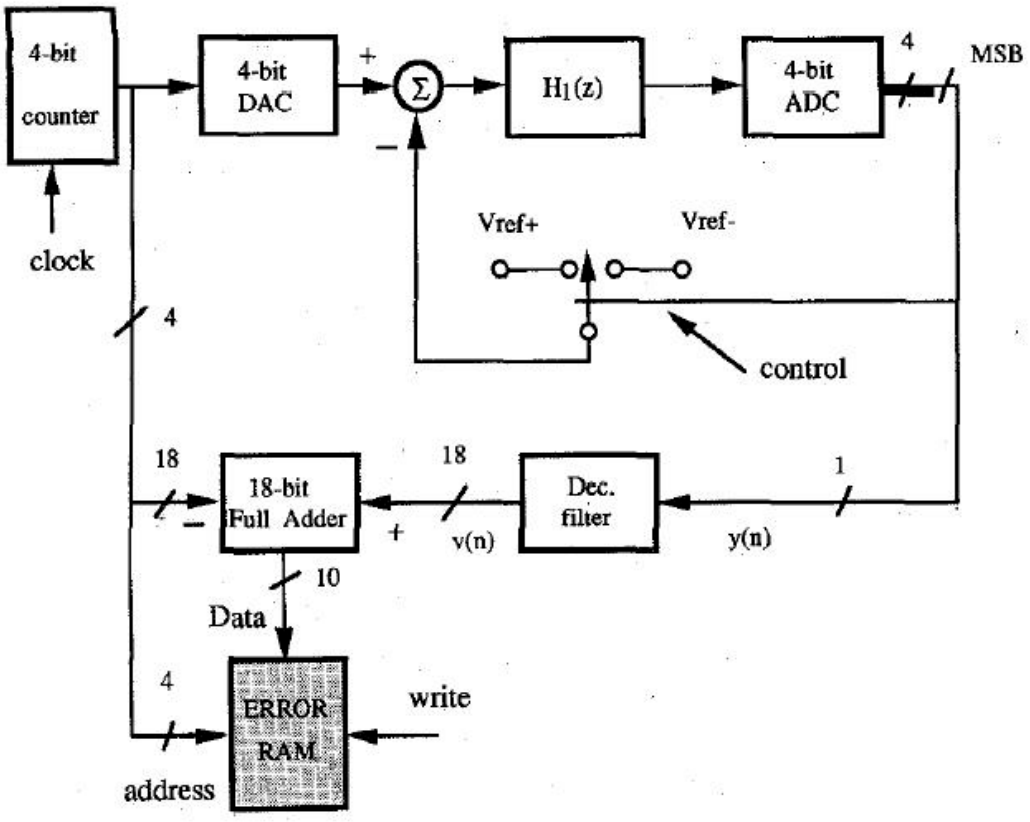


Figure 3-8 Direct measurement and digital correction.

A technique that directly measures the deviation of every output level of the DAC and performs digital correction at the ADC output according to the measured results was proposed, and a successful implementation was presented in [11]. Using this technique, the multi-bit delta sigma ADC is reconfigured into a single-bit one during the calibration process, when the output deviations of the multi-bit DAC are measured by the single-bit delta sigma ADC and stored in a RAM, as shown in Figure 3-8. The main drawback of this technique is that it runs

in the foreground and needs to interrupt the normal operation to carry on the calibration.

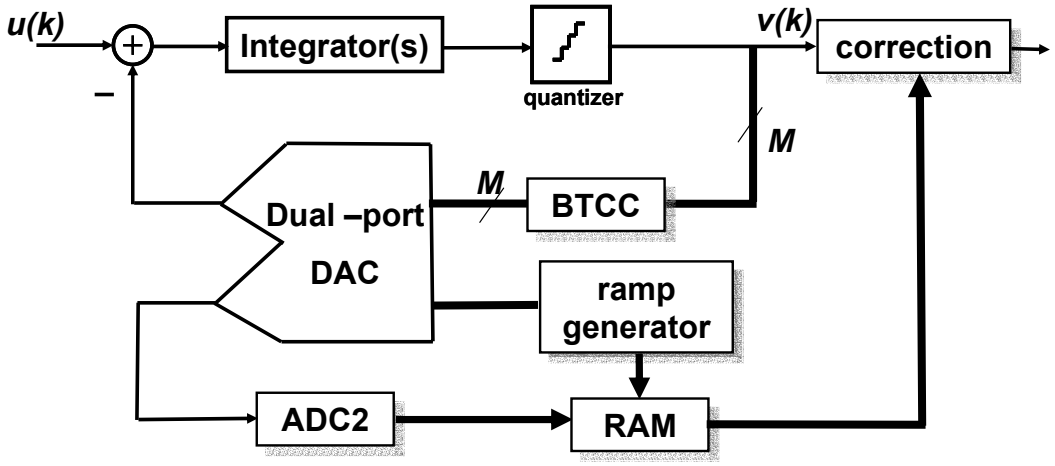


Figure 3-9 Direct measurement based on a dual port DAC.

In [12], the digital correction technique of [11] is modified. During each clock, unused unit-elements are measured by a second delta sigma ADC through the extra input and output ports, as shown in Figure 3-9. The errors are also stored in a RAM for the digital correction. Since the error measurement is in the background, normal operation is going on continuously. But a dual-port DAC is complicated in design and an extra delta sigma ADC is needed.

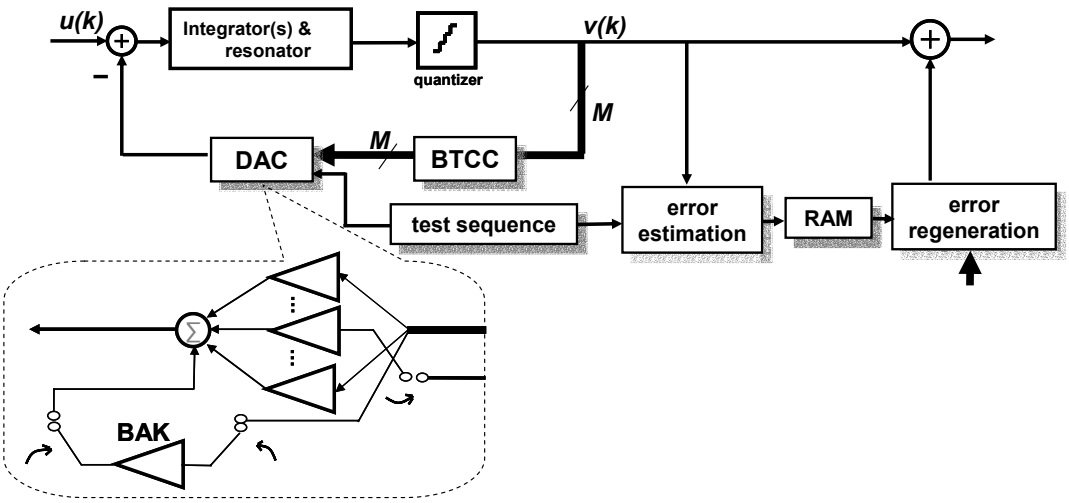


Figure 3-10 DAC error estimation with test sequence and digital correction

In [13], another background digital correction technique is reported. Here, instead of direct measurement, the unit element errors are detected from the ADC output. The *NTF* of the delta sigma ADC is changed, creating a zero at $f_s/2$. At and near this zero, there is no input signal and the quantization noise is shaped, leaving a clear space in the spectrum. One at a time, the unit elements are controlled by a special sequence with "1 -1 1-1…" pattern, generating a calibration tone at $f_s/2$, which contains the information of the error of the element being manipulated. The value of this specific error is then accurately recovered from the calibration tone after the input signal and the quantization noise are filtered out. After the errors of all unit elements are obtained, the correction is carried on, as shown in Figure 3-10. The drawback of this technique is obvious: the *NTF* needs to be changed by moving one of zeros to $f_s/2$, resulting in raised in-band quantization noise power. Besides, an extra unit-element is needed for backup in the DAC.

3.4 Fully digital DAC error detection and correction

The purpose of this research is to find a fully digital technique to deal with the DAC error in the ADC output. This technique is to distinguish the error and then remove it from the whole spectrum of the ADC output, including the signal band. The motivation of a fully digital technique is that it can take advantage of the scaling down of digital integrated circuits which means smaller die area, lower supply voltage and lower power. It can be easily transferred from one technology to another. Analog circuits do not benefit from the development of advanced technologies as much as digital circuits do. So the idea here is to use no extra analog circuitry and rely on digital signal processing to boost the circuit performance. The desired technique should not contain any separate measurement process that need to interrupt the normal operation of the DAC. It should work with low OSRs and conventional designs of the delta sigma loop.

There is an important challenge for inventing such a technique: the DAC error is mixed with the input signal and the quantization noise in the ADC output. All of them are at the same frequency range and the input signal may have much larger power than the DAC error. It will be difficult to distinguish the DAC error from such a background.

3.5 Conclusions

In this chapter, several important observations and conclusions which are fundamental to the later discussions were made.

The impact of the output deviations of the unit elements in the multi-bit feedback DAC on the ADC performance was analyzed, and two effects were found. While the extra gain is not significant, the DAC error directly limit the ADC performance. Several existing techniques dealing with the DAC error were introduced and their drawbacks were pointed out. Then the features of a desired new technique were listed and the challenge to come up with such a technique was presented.

Chapter 4 Fully digital estimation and correction of the DAC error

According to Eq.**(3-4)**, in the ADC output the DAC error turns out to be the sum of the unit-element errors modulated by corresponding selecting signals filtered by *ETF*. The selecting signals are known and so is the nominal *ETF*. If the unit-element errors can be estimated, the DAC error in the ADC output can be calculated and removed, as shown below:

$$\begin{aligned} v_c(k) &= v(k) - c(k) \\ &= u'(k) + q'(k) + \sum_{i=1}^{M} \left(e_i \cdot b'_i(k) \right) - \sum_{i=1}^{M} \left(\hat{e}_i \cdot b'_i(k) \right) \\ &= u'(k) + q'(k), \end{aligned} \qquad \textbf{(4-1)}$$

where $v_c(k)$ is the corrected ADC output, $c(k)$ is the correction term for the ADC output and $\hat{e}_i$ is the estimated value for e_i. The problem of estimating the DAC error now becomes estimating the unit-element errors from the ADC output.

One thing needs to be mention is that the actual *ETF* is slightly different from the nominal one because of the extra gain α. To know the actual *ETF*, α has to be estimated first, which is quite complicated. For convenience, α is not estimated and the nominal *ETF* is used in the calculation of the DAC error.

4.1 Correlation

Here, a correlation operation between two signals $x(k)$ an $y(k)$ is defined as

$$\mathrm{CORR}^K\left[y(k),x(k)\right]=\frac{\sum_{k=1}^{K}\left[y(k)\cdot x(k)\right]}{\sum_{k=1}^{K}x^2(k)}, \qquad \textbf{(4-2)}$$

where $x(k)$ and $y(k)$ are the two signals involved in the correlation. Note that in this definition, the correlation is an operation based on a block of K consecutive samples of the signals and $y(k)$ and $x(k)$ are not interchangeable. It is not difficult to verify the results that the correlation will give under the conditions listed in Table 4-1.

Table 4-1 Correlation results under various conditions.

	Results	Conditions:
1.	$\mathrm{CORR}^K\left[y(k),x(k)\right]=\beta$	$y(k)=\beta\cdot x(k)$ and β is a constant
2.	$\mathrm{CORR}^K\left[y(k),x(k)\right]\to 0$	$y(k)$ is uncorrelated with $x(k)$ and $K\to+\infty$
3.	$\mathrm{CORR}^K\left[y(k),x(k)\right]\to\beta$	$y(k)=\beta\cdot x(k)+z(k)$ where $z(k)$ is uncorrelated with $x(k)$, and $K\to+\infty$

It can be seen that if a constant or DC value is modulated by a signal, the correlation between the modulated DC value and the modulating signal can

recover it. If there are other uncorrelated interferences mixed with the modulated DC value, the accuracy of the recovery depends on the number of the samples involved in the correlation. It is known that the correlation can recover the DC value even when the modulating signal is in the same band as the uncorrelated interferences and has similar or even lower power compared to the interferences.

In the ADC output, the unit-element errors, which are DC values, are modulated by the filtered selecting signals $b'_i(k)$, as shown in Eq.**(3-4)**. So it is natural to expect that the correlation between the ADC output $v(k)$ and $b'_i(k)$ can recover the unit-element errors:

$$\begin{aligned} \mathrm{CORR}^K\left[v(k), b_i'(k)\right] &= \mathrm{CORR}^K\left[u'(k), b_i'(k)\right] + \mathrm{CORR}^K\left[q'(k), b_i'(k)\right] \\ &\quad + e_i + \sum_{j=1, j\neq i}^{M}\left\{e_j(k)\cdot \mathrm{CORR}^K\left[b_j'(k)\cdot b_i'(k)\right]\right\}, \\ i &= 1,2,...M \end{aligned} \qquad \textbf{(4-3)}$$

The ADC output also contains the input signal $u'(k)$ and the quantization noise $q'(k)$. During the correlation, they are interferences. So are other modulated unit-element errors e_j (j=1,2,…M and j≠i) during the estimation of a certain unit-element error e_i, as shown in Eq.**(4-3)**.

Unfortunately, neither the signal $u'(k)$ nor the quantization noise $q'(k)$ are uncorrelated with $b_i'(k)$. The sum of the selecting signals is exactly the ADC output if the quantization step Δ is omitted:

$$v(k) = \sum_{i=1}^{M} b_i(k). \qquad \textbf{(4-4)}$$

$b_i(k)$ (i=1,2…M) contain an inherent component that is a scaled version of $v(k)$, which contains $u'(k)$ and $q'(k)$. In other words, $b_i(k)$ are inherently correlated with $u'(k)$ and $q'(k)$. So are $b'_i(k)$, which are just filtered $b_i(k)$. No matter how large K is, the first and second term on the right side of Eq.**(4-3)** will not go to zero, so the correlation will not converge to the wanted unit-element error e_i.

4.2 Decorrelating and scrambling

Two operations are performed to decorrelate $b'_i(k)$ with $u'(k)$ and $q'(k)$ before the correlation. First, before filtering $b_i(k)$ with the nominal *ETF* to obtain $b'_i(k)$, a scaled version of $v(k)$ is subtracted from $b_i(k)$ as shown in Eq.**(4-5)** to remove the inherent correlation between $b_i(k)$ and $v(k)$ previously mentioned [18]. Assuming that $b_1(k)$~ $b_M(k)$ contain same amount of $v(k)$ and taking into account Eq.**(4-4),** a scaling factor of 1/M is used**:**

$$n_i(k) = b_i(k) - \frac{1}{M}\sum_{i=1}^{M} v(k),\ i = 1,2,...M. \qquad \textbf{(4-5)}$$

$n_i(k)$ (i=1,2,…M) are decorrelated selecting signals, which are then filtered by the *ETF*, resulting in $n'_i(k)$, which is actually used in the correlation operation.

Combining Eq.**(3-2)**,Eq.**(3-3)** and Eq.**)**, a new expression of the DAC output $a(k)$ using $n_i(k)$ is obtained:

$$\begin{aligned} a(k) &= \alpha \cdot \Delta \cdot \sum_{i=1}^{M} b_i(k) + \frac{\alpha}{M} \cdot v(k) \cdot \left(\sum_{i=1}^{M} e_i \right) + \alpha \cdot \sum_{i=1}^{M} \left[n_i(k) \cdot e_i \right] \\ &= \alpha \cdot \Delta \cdot \sum_{i=1}^{M} b_i(k) + \alpha \cdot \sum_{i=1}^{M} \left[n_i(k) \cdot e_i \right]. \end{aligned} \tag{4-6}$$

Based on Eq.**(4-6)**, the ADC output $v(k)$can be expressed using $n_i'(k)$:

$$v(k) = u'(k) + q'(k) + \sum_{i=1}^{M} \left[n_i'(k) \cdot e_i \right], \tag{4-7}$$

So the correlation operation now becomes:

$$\begin{aligned} \mathrm{CORR}^K \left[v(k), n_i'(k) \right] &= \mathrm{CORR}^K \left[u'(k), n_i'(k) \right] + \mathrm{CORR}^K \left[q'(k), n_i'(k) \right] \\ &\quad + e_i + \sum_{j=1, j \neq i}^{M} \left\{ e_j(k) \cdot \mathrm{CORR}^K \left[n_j'(k) \cdot n_i'(k) \right] \right\} \\ i &= 1,2,...M \end{aligned} \tag{4-8}$$

Second, like in the randomization DEM technology described in **Section 3.2**, a scrambler SCR, which randomly rearrange the bits in the input to the DAC, is embedded in the delta-sigma loop as shown in Figure 4-1. By using the scrambler, $n_i(k)$ (i=1,2,…M) are made independent of the DAC input, thus $n_i'(k)$ are independent of $u'(k)$ and $q'(k)$.

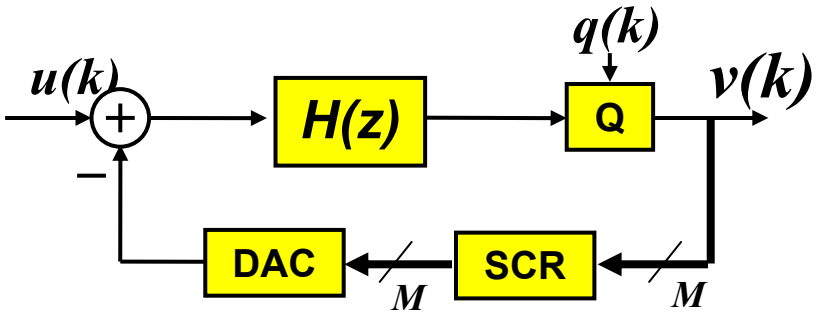


Figure 4-1 Scrambler.

4.3 Eliminating mutual interferences when recovering unit-element errors

With the two operations in **Section 4.2**, the first two terms on the right side of Eq.**(4-8)** will go to zero when K goes to infinity, but the third term will converge to a finite value because

$$\sum_{i=1}^{M} n_i'(k) = etf(k) * \sum_{i=1}^{M} n_i(k) = 0, \qquad \textbf{(4-9)}$$

which means $n_i'(k)$ (i=1,2…M) are correlated with each other. With the existence of the cross-correlations, each result of the correlation operation in **(4-8)** will be a linear combination of all unit-element errors:

$$\begin{bmatrix} \mathrm{CORR}^K[v(k), n_1'(k)] \\ \mathrm{CORR}^K[v(k), n_2'(k)] \\ \vdots \\ \mathrm{CORR}^K[v(k), n_M'(k)] \end{bmatrix} \rightarrow \mathbf{R} \times \begin{bmatrix} e_1 \\ e_2 \\ \vdots \\ e_M \end{bmatrix}, \qquad \textbf{(4-10)}$$

where

$$\mathbf{R} = \begin{bmatrix} 1 & \mathrm{CORR}^K[n_2'(k), n_1'(k)] & \cdots & \mathrm{CORR}^K[n_M'(k), n_1'(k)] \\ \mathrm{CORR}^K[n_1'(k), n_2'(k)] & 1 & \cdots & \mathrm{CORR}^K[n_M'(k), n_2'(k)] \\ \vdots & \vdots & \ddots & \vdots \\ \mathrm{CORR}^K[n_1'(k), n_M'(k)] & \mathrm{CORR}^K[n_2'(k), n_M'(k)] & \cdots & 1 \end{bmatrix}.$$

The matrix **R**, which contains the cross-correlations between $n_i'(k)$ (i=1,2,…*M*), can be calculated. And e_i(*i*=1,2,…*M*) can be recovered from the results of the correlation operation with one more inversion process:

$$\begin{bmatrix} \hat{e}_1 \\ \hat{e}_2 \\ \vdots \\ \hat{e}_{M-1} \end{bmatrix} = (\mathbf{R}')^{-1} \times \begin{bmatrix} \mathrm{CORR}^K[v(k), n_1'(k)] \\ \mathrm{CORR}^K[v(k), n_2'(k)] \\ \vdots \\ \mathrm{CORR}^K[v(k), n_{M-1}'(k)] \end{bmatrix}. \qquad \textbf{(4-11)}$$

Note that **R** is singular, because the rows in it add up to zero vectors and so do the columns. So the inversion of **R** can not be obtained directly. First, the *M*-th

column and M-th row are removed from **R**, making a (M-1)×(M-1) nonsingular matrix **R'**:

$$\mathbf{R}'= \begin{bmatrix} 1 & \mathrm{CORR}^K[n_2'(k), n_1'(k)] & \cdots & \mathrm{CORR}^K[n_{M-1}'(k), n_1'(k)] \\ \mathrm{CORR}^K[n_1'(k), n_2'(k)] & 1 & \cdots & \mathrm{CORR}^K[n_{M-1}'(k), n_2'(k)] \\ \vdots & \vdots & \ddots & \vdots \\ \mathrm{CORR}^K[n_1'(k), n_{M-1}'(k)] & \mathrm{CORR}^K[n_2'(k), n_{M-1}'(k)] & \cdots & 1 \end{bmatrix} \quad \textbf{(4-12)}$$

And e_i (i=1,2,…,M-1) are recovered by **(4-13)**.

$$\begin{bmatrix} \hat{e}_1 \\ \hat{e}_2 \\ \vdots \\ \hat{e}_{M-1} \end{bmatrix} = (\mathbf{R}')^{-1} \times \begin{bmatrix} \mathrm{CORR}^K[v(k), n_1'(k)] \\ \mathrm{CORR}^K[v(k), n_2'(k)] \\ \vdots \\ \mathrm{CORR}^K[v(k), n_{M-1}'(k)] \end{bmatrix}. \quad \textbf{(4-13)}$$

Then e_M is obtained by

$$\hat{e}_M = -\sum_{i=1}^{M-1} \hat{e}_i. \quad \textbf{(4-14)}$$

As a matter of fact, the matrix **R** is very simple in the case of a scrambler adopting random rearranging algorithm. From **(4-9)**, it is known that for a certain $n_i'(k)$:

$$n_i'(k) = -\sum_{j=1, j\neq i}^{M} n_j'(k) \tag{4-15}$$

$n_j'(k)$ (j=1,2,…,M, $j\neq i$) on the right side of **(4-15)** have the same status. It is reasonable to get:

$$-\frac{1}{M-1} n'_i(k) + m_j(k) = n_j'(k), \quad j = 1,2,...,M, j \neq i \tag{4-16}$$

where $m_j(k)$ (j=1,2,…M, $j\neq i$) is the component in $n_j'(k)$ that is uncorrelated with $n_i'(k)$. So

$$\mathrm{CORR}^K\left[n_j'(k), n_i'(k)\right] = -\frac{1}{M-1}. \quad i = 1,2,...M, j = 1,2,...,M, i \neq j \tag{4-17}$$

Combining this with:

$$e_i = -\sum_{j=1, j\neq i}^{M} e_j\ , \tag{4-18}$$

it can be obtained that:

$$\mathbf{R} = \begin{bmatrix} 1 & -\frac{1}{M} & \cdots & -\frac{1}{M} \\ -\frac{1}{M} & 1 & \cdots & -\frac{1}{M} \\ \vdots & \cdots & \ddots & \vdots \\ -\frac{1}{M} & -\frac{1}{M} & \cdots & 1 \end{bmatrix}. \tag{4-19}$$

So

$$\mathbf{R}^{-1} = \begin{bmatrix} \frac{M-1}{M} & 0 & \cdots & 0 \\ 0 & \frac{M-1}{M} & \cdots & 0 \\ \vdots & \cdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{M-1}{M} \end{bmatrix}, \tag{4-20}$$

which means

$$\hat{e}_i = \frac{M-1}{M} \cdot \mathrm{CORR}^K\left[v(k), n_i'(k)\right]. \tag{4-21}$$

4.4 High-pass filter to suppress the input signal

Although $n_i'(k)$ are uncorrelated with the input signal $u'(k)$ and the quantization noise $q'(k)$ now, enough samples are still needed in the correlation to suppress the two interferences. To this point, a quantitative theory on the

relationship of the desired accuracy and the number of samples needed has not been found, a known fact is that in the correlation, the suppression of the interferences is increased by 3 dB by doubling the number of samples. This is not efficient enough for high resolution designs. For an interference suppression of 100 dB, some 2^{33} samples need to be involved in the correlation. That is equivalent to 1 minute 26 seconds in real circuit time even with a clock rate of 100 MHz.

In broadband (low OSR), high resolution designs, in order to meet the resolution requirement without much help from the noise shaping, the total power of the quantization noise is reduced by adopting multi-bit quantizer and using cascaded delta sigma ADC structures. So the suppression needed for it is relatively small and will not need too many samples. But to suppress the input signal, which in worst case is $\pm Vref$ peak to peak, the correlation could take an unacceptable time if no special preprocessing is used. Actually, in some earlier tries of this research, the correlation got stuck and failed to converge to desired accuracy within a reasonable time of computer simulations.

A high-pass FIR filter (HPF) is therefore used to filter the ADC output $v(k)$ before it is used to correlate with $n_i'(k)$ [19]. This is based on the knowledge that the signal band is at the low frequencies so a high-pass filter suppresses the input signal. An FIR filter is chosen because of its guaranteed stability and linear phase response.

In the output of the HPF $v'(k)$, the input signal is suppressed, but the DAC error is also filtered. Thus, a corresponding operation needs to be performed to synchronize $n_i'(k)$ with the DAC error in $v'(k)$ before the correlation is performed. This operation could also be the HPF, which is not economical. Or it can be simply a delay. $v'(k)$ is the sum of multiple versions of $v(k)$, which are delayed by different number of clock periods and multiplied by corresponding HPF coefficients. Each of these versions of $v(k)$ contains the DAC error and can be individually picked as the object for the correlation. In practice, the version that is multiplied by the largest HPF coefficient is picked because it has the largest power. Correspondingly, a delay of l clock periods is applied to $n_i'(k)$ (i=1,2,…M), where l is the number of the delay of the picked version of $v(k)$, resulting in $n_i'(k\text{-}l)$ (i=1,2,…M), which are actually used for the correlation. Note that the DAC error in the picked version of $v(k)$ is multiplied by the largest HPF coefficient $h_{HPF}(l)$, so the results given by the correlation need to be divided by $h_{HPF}(l)$.

Thanks again to the randomization performed by the scrambler to the input bits of the DAC, the DAC error is white in spectrum, which means it has an autocorrelation function similar to δ–function. So, during the correlation between $n_i'(k\text{-}l)$ and $v'(k)$, the interferences caused by the DAC errors in $v(k)$ versions with delays other than l in $v'(k)$ will get negligible when the number of samples involved in the correlation K becomes large enough.

4.5 Complete block diagram of the proposed technique

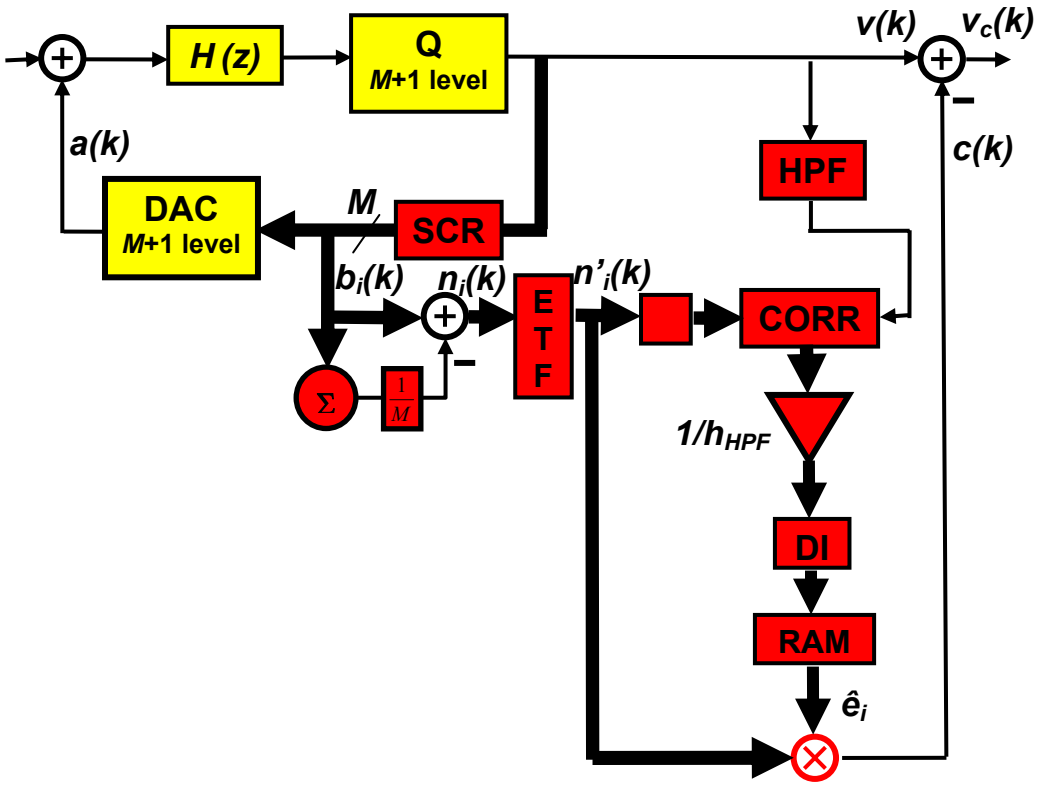


Figure 4-2 Complete diagram of the proposed technique

Figure 4-2 shows the complete block diagram of the proposed technique. As a summary, the error detection and correction process is briefly reviewed:

1). The scrambler SCR performs a random rearrangement of the input bits to the DAC in every clock.

2). $\frac{v(k)}{M}$ is subtracted from each selecting signal $b_i(k)$ (i=1,2,…M), resulting in the $n_i(k)$ (i=1,2,…M).

3). $n_i'(k)$ (i=1,2,…M) are obtained by filtering $n_i(k)$ (i=1,2,…M) with a digital filter ETF, emulating the nominal *ETF* (just delays in most cases, the difference between the actual and nominal *ETF* is ignored).

4). The ADC output $v(k)$ is filtered by the high-pass FIR filter HPF, resulting in $v'(k)$. A delay block D (= z^{-l}) is inserted between the ETF block and the CORR block to synchronize $n_i'(k)$ with $v'(k)$ before the correlation is performed. l is the number of the delays associated with the largest HPF coefficient $h_{HPF}(l)$.

5). The $n_i'(k\text{-}l)$ (i=1,2,…M) are correlated with $v'(k)$ in block CORR, and the result is processed by the inversed cross-correlation matrix $\mathbf{R}^{-1}$ to give the estimate of the unit-element errors $\hat{\boldsymbol{e}}_i$.

6). The results are stored in the RAM. The correction term for the DAC error, $c(k)$, is regenerated by multiplying the estimated unit-element errors with corresponding $n_i'(k)$ and is subtracted from the ADC output $v(k)$.

Note that the K samples of $v(k)$ and $n_i'(k)$ involved in the correlation have started K clocks ago until the current time. The correlation can be done every clock cycle, based on the data in a moving window of a length of K and get the estimated

error update every clock period, or it can be done once in K clock periods so the estimated error will be updated every K clock cycles. M unit-element errors can be estimated one at a time or estimated simultaneously.

4.6 Simulations

4.6.1 2-0 MASH ADC

Cascaded delta sigma ADCs (or MASH ADCs) are used for building equivalent high-order delta-sigma ADCs without the risk of instability [15]. Figure 4-3 shows a MASH ADC. It consists of 2 stages, ADC1 and ADC2, which are both single-loop delta-sigma ADCs. There is an inter-stage gain g_1. The input signal $u(k)$ is fed into the first stage. The second stage takes as its input the quantization noise of the first stage, $q_1(k)$. So

$$\begin{aligned} v_1(k) &= stf_1(k) * u(k) + ntf_1(k) * q_1(k), \\ v_2(k) &= stf_2(k) * \left[g_1 \cdot q_1(k)\right] + ntf_2(k) * q_2(k). \end{aligned} \quad \textbf{(4-22)}$$

The outputs, $v_1(k)$ and $v_2(k)$, enter an error-cancellation logic, where the quantization noise of the first stage is cancelled as long as the digital transfer function $DNTF_1$ perfectly matches the noise transfer function of the first stage, NTF_1, as shown in Eq.**(4-23)**.

$$
\begin{aligned}
v(k) &= stf_2(k) * v_1(k) - dntf_1(k) * \frac{v_2(k)}{g_1} \\
&= stf_1(k) * stf_2(k) * u(k) + stf_2 * ntf_1(k) * q_1(k) \\
&\quad - dntf_1(k) * stf_2(k) * q_1(k) - dntf_1(k) * ntf_2(k) * \frac{q_2(k)}{g_1}. \\
&= \underbrace{stf_1(k) * stf_2(k)}_{stf(k)} * u(k) - \underbrace{dntf_1(k) * ntf_2(k)}_{ntf(k)} * \underbrace{\frac{q_2(k)}{g_1}}_{q(k)}
\end{aligned}
\qquad \textbf{(4-23)}
$$

Shown in Eq.**(4-23)**, the MASH ADC in Figure 4-3 is actually equivalent to a single-loop delta sigma ADC with an $STF = STF_1 \cdot STF_2$, an $NTF = -DNTF_1 \cdot NTF_2$ and a quantization noise $q(k) = q_2(k)/g_1$. The equivalent single-loop delta sigma ADC is with an order that equals the sum of the orders of both stages in the MASH ADC, resulting in a high order system. The equivalent number of bits of its quantizer is increased by the inter-stage gain g_1. This is more economic and practical than directly building a single quantizer with many bits.

Another major advantage of MASH ADC over a single-loop one is that, since the stages are only using low-order (lower than 2) delta sigma ADCs, their stability can be guaranteed.

One thing needs to mention is that for the inter-stage gain g_1 (>1) to be possible, a multi-bit quantizer in the first stage is necessary. Otherwise, the quantization noise $q_1(k)$ will overload the second stage after it is amplified by g_1. For this reason, although $q_1(k)$ is going to be cancelled eventually, multi-bit or single-bit for the quantizer still makes a difference.

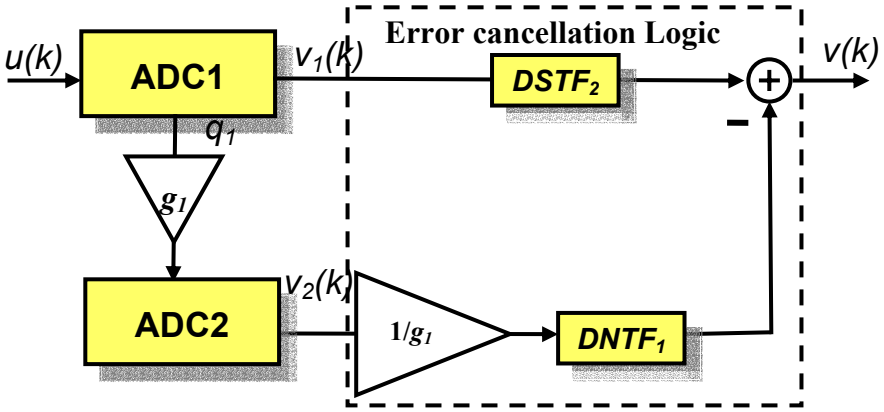


Figure 4-3 MASH ADC (2 stages)

4.6.2 Simulation results

In all simulations to verify the proposed technique of **Chapter 4**, a two-stage MASH ADC as shown in Figure 4-4 was used. The first stage is a second-order multi-bit delta sigma ADC with a novel low-distortion architecture [20]. The second stage Q_2 is simply a 10-bit quantizer, which can be seen as a zero-order delta sigma ADC. All simulations were done using Simulink and the Schreier Toolbox for Delta Sigma Modulators [21].

First, a set of simulations was performed using the parameters listed in Eq.**(4-24)** The clock rate was assumed to be 100 MHz and the OSR was 4.

$$M = 32,\ \ \gamma_1 = \frac{1}{4},\ \gamma_2 = \frac{1}{16},\ \gamma_3 = \frac{1}{16},\ \ H_1(z) = \frac{8 \cdot z^{-1}}{1 - z^{-1}},\ \ H_2(z) = \frac{2 \cdot z^{-1}}{1 - z^{-1}}. \quad \textbf{(4-24)}$$

.

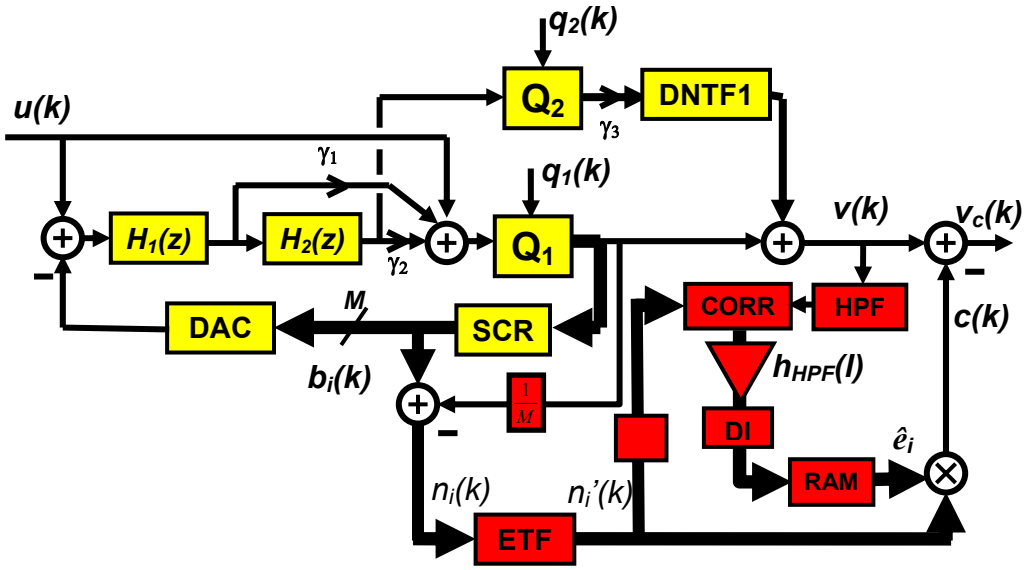


Figure 4-4 2-0 MASH ADC for simulation

Figure 4-5 shows the output spectrum of the MASH ADC using an ideal DAC. With a 1.56 MHz and -0.92 dB sine-wave input, the output SNDR was 102.6 dB.

Figure 4-6 shows the output spectrum when the DAC was with 0.1% RMS unit-element errors and no DEM, calibration or correction technologies were applied. The SNDR dropped to 76.2 dB, and large harmonic spurs appeared. The impact of the DAC error in a MASH structure is very serious. This is one of

reasons the proposed technique was simulated in a MASH ADC. Observing the spectrum in Figure 4-6, the analysis about the effect of thermometer coded DAC input in **3.2** is verified. The noise floor went up and there were strong input-signal-dependent tones in the signal band.

The simulation results of two dynamic element matching algorithms under the same conditions are shown. Data-weighted averaging lowered the noise floor, but still caused strong signal-dependent tones and only achieved an SNDR of 85.2 dB, as shown in Figure 4-7. Zero-order randomization only caused a 3.1 dB improvement in the SNDR, since it raised the noise floor, although it removed the tones, as shown in Figure 4-8 .

Using the same real DAC, the proposed technique raised the output SNDR to 101.5 dB under the same conditions after a correction process lasting 131,072 clock periods. The output spectrum is shown in Figure 4-9.

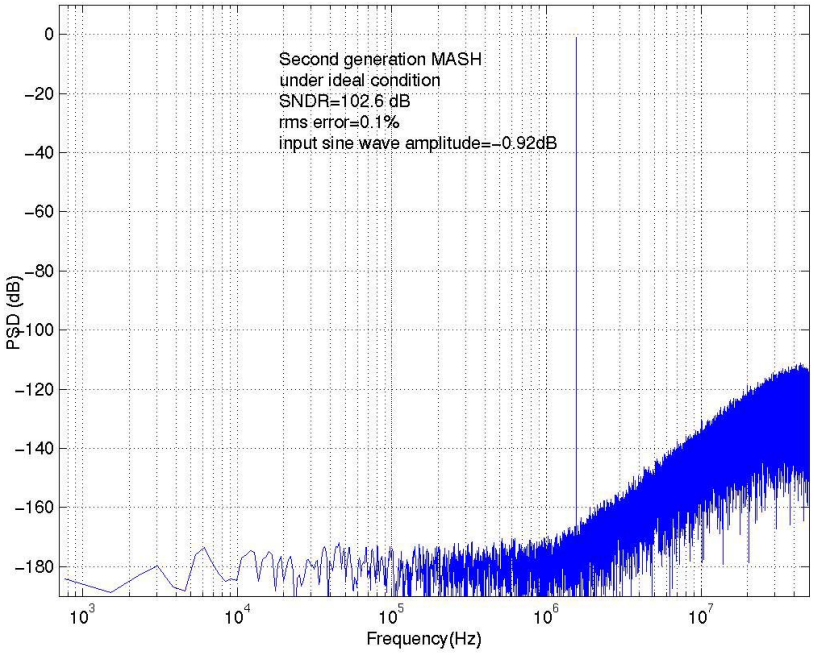


Figure 4-5 5-bit DAC simulation result: Ideal case

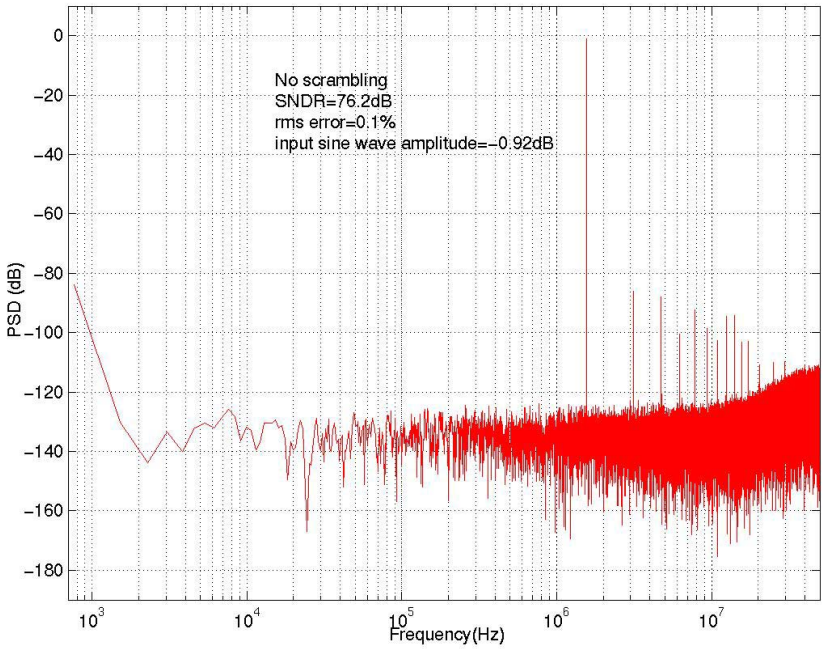


Figure 4-6 5-bit DAC simulation result: Impact of the DAC error

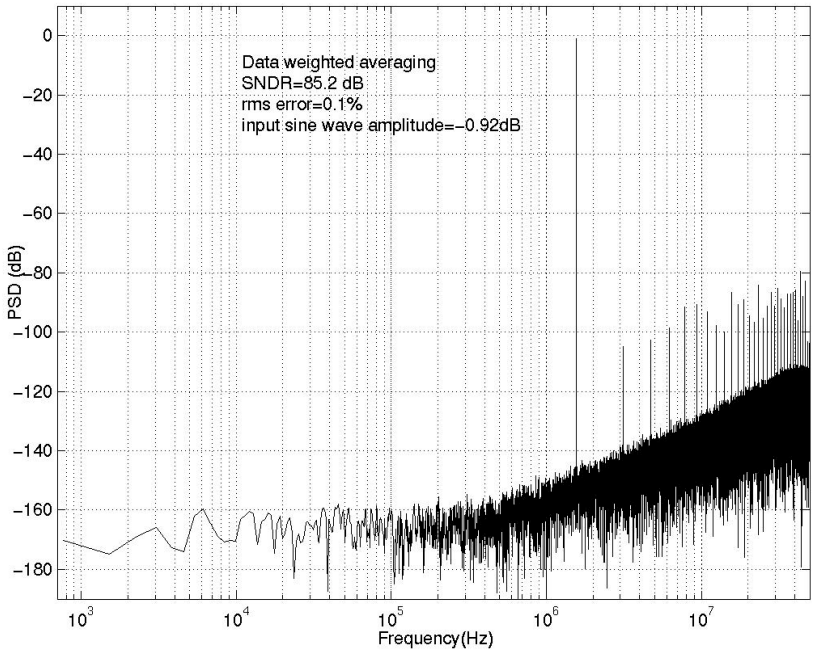


Figure 4-7 5-bit DAC simulation result: DWA

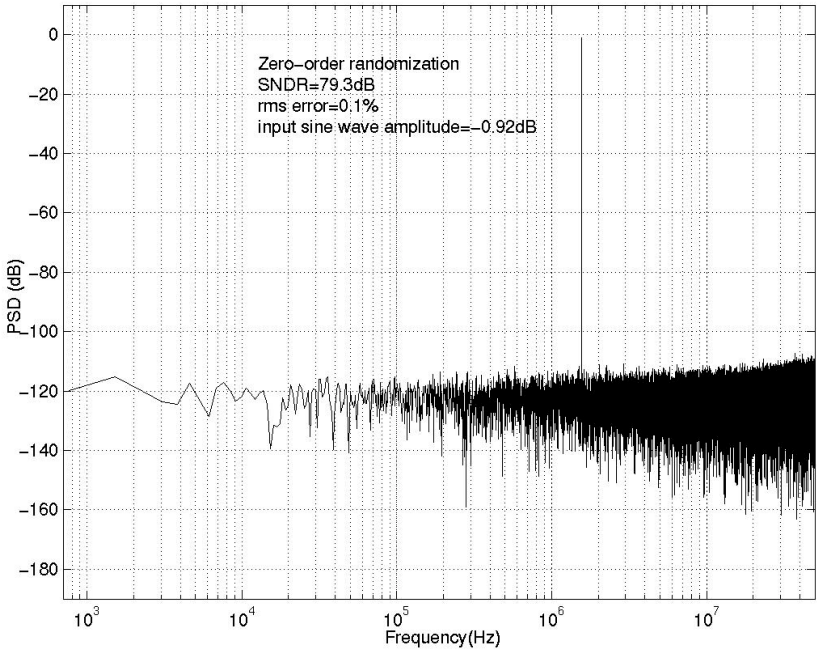


Figure 4-8 5-bit DAC simulation result: randomization

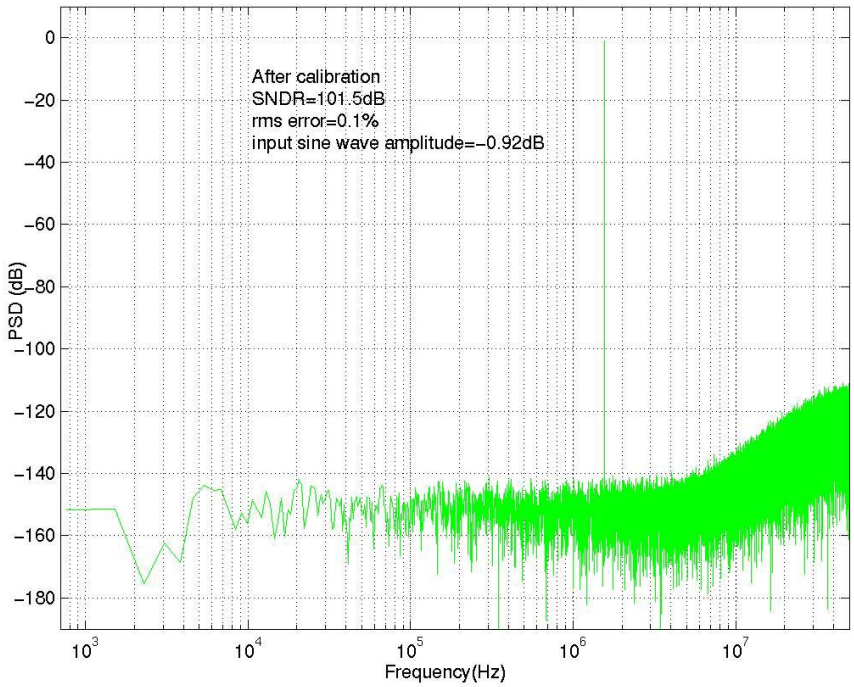


Figure 4-9 5-bit DAC simulation result: proposed correction

Another set of simulations with the parameters listed in Eq.**(4-25)** was also performed for the preparation of the design of the experimental ADC described in **Chapter 6**. The clock rate was assumed to be 100 kHz and the OSR was 4. And in the nonideal cases, 0.1% RMS errors were assigned to the unit-elements.

$$M = 8,\ \ \gamma_1 = 1,\ \gamma_2 = \frac{1}{4},\ \gamma_3 = \frac{1}{4},\ \ H_1(z) = \frac{2 \cdot z^{-1}}{1 - z^{-1}},\ \ H_2(z) = \frac{2 \cdot z^{-1}}{1 - z^{-1}}.. \qquad \textbf{(4-25)}$$

Figure 4-10~Figure 4-15 show the simulation results. They are the output spectrums of the ADC with ideal DAC, nonideal DAC, nonideal DAC but with DWA, bi-DWA[3], 1st-order mismatch shaping and the proposed correction. It can

be seen again that the proposed correction technique is superior to DEM technologies for low OSR values.

4.7 Conclusion

The fully digital DAC correction technique was introduced in detail. First, based on the knowledge of the structure of the DAC error, a correlation operation was suggested to estimate the unit-element errors from the ADC output. The interferences from the input signal and the quantization noise during the correlation were analyzed, resulting in the introduction of a decorrelating process and a scrambler. The mutual interference between the selecting signals was then analyzed and one more inversion operation was added to the estimation process. To accelerate the convergence, a high-pass filter was used to filter the ADC output before the correlation, and corresponding operation was performed on the selecting signals. Finally, a complete diagram of the proposed technique was shown.

Simulations have been done with MASH ADCs. The basic principle of MASH ADCs was introduced. According to the simulations, the proposed technique can improve the SNDR of the ADC output to close to that of the ideal case with 0.1% RMS error applied to the unit-elements in the DAC of the first stage and an OSR of 4. The proposed technique was proven to be effective and superior to DEM technologies.

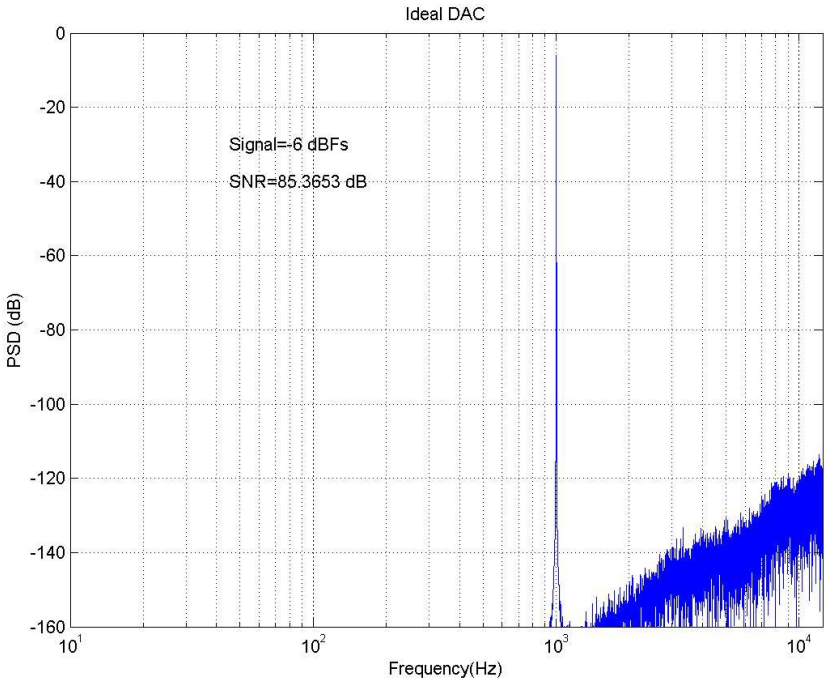


Figure 4-10 3-bit DAC simulation result: Ideal

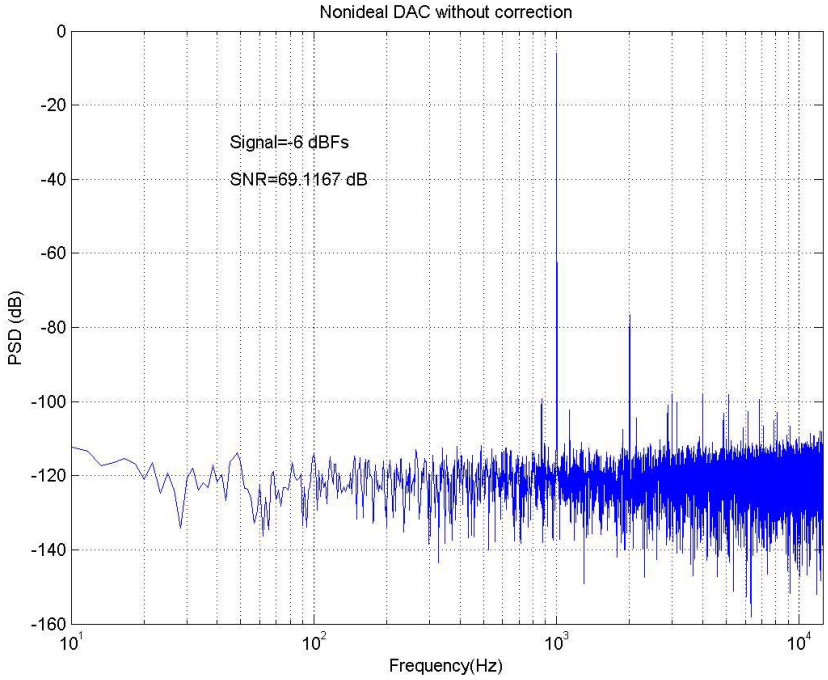


Figure 4-11 3-bit DAC simulation result: Nonideal

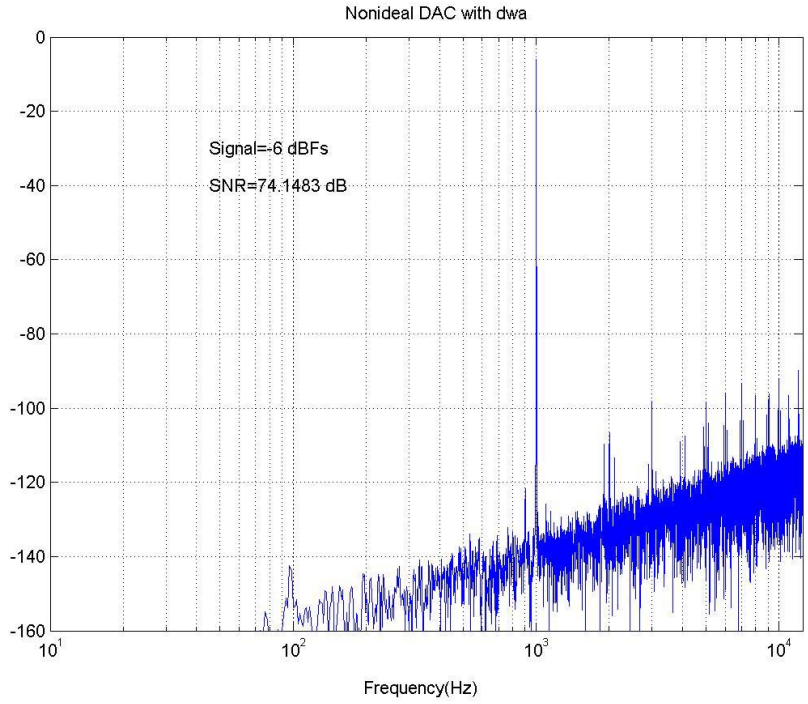


Figure 4-12 3-bit DAC simlation result: DWA

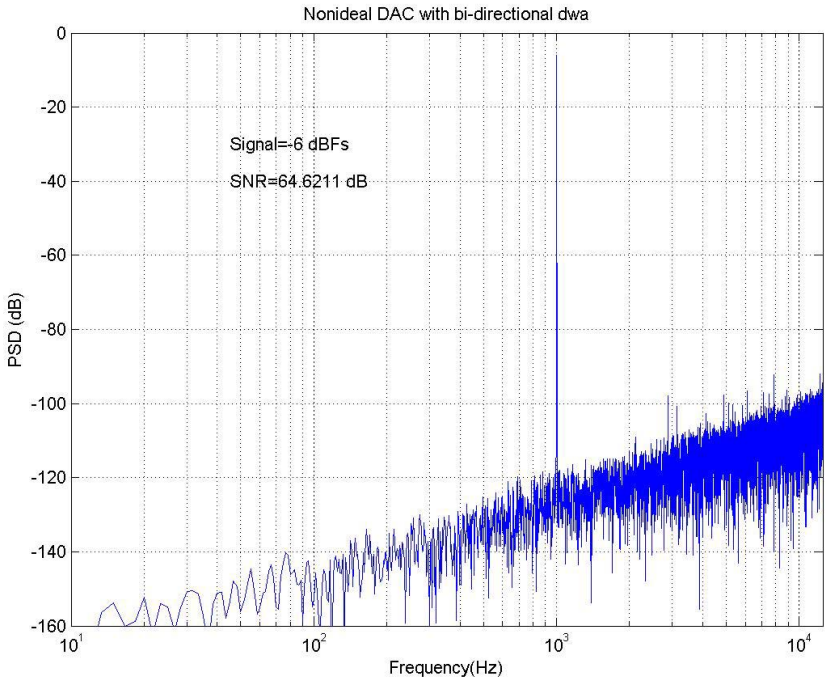


Figure 4-13 3-bit DAC simulation result: Bi-DWA

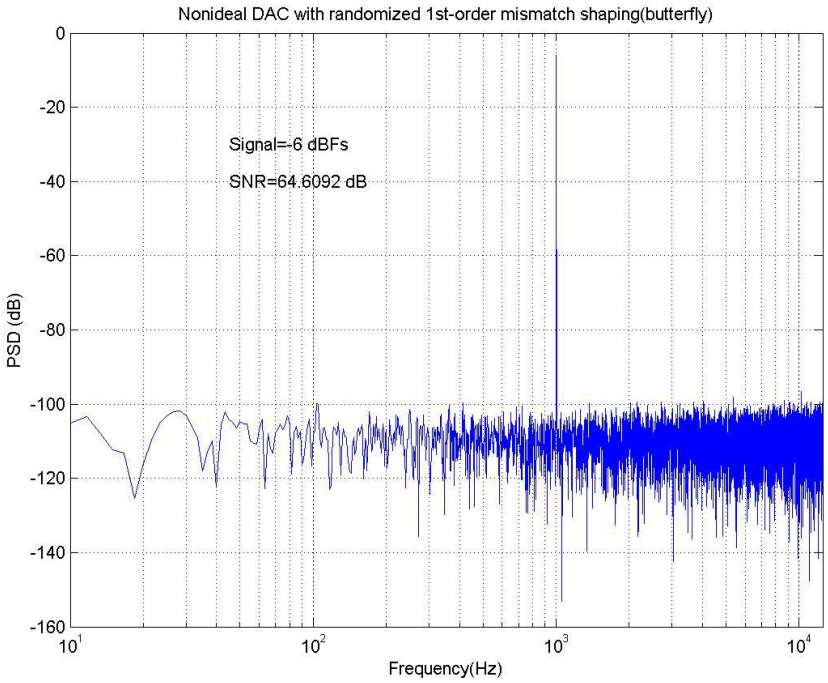


Figure 4-14 3-bit DAC simulation result: 1-st order shaping

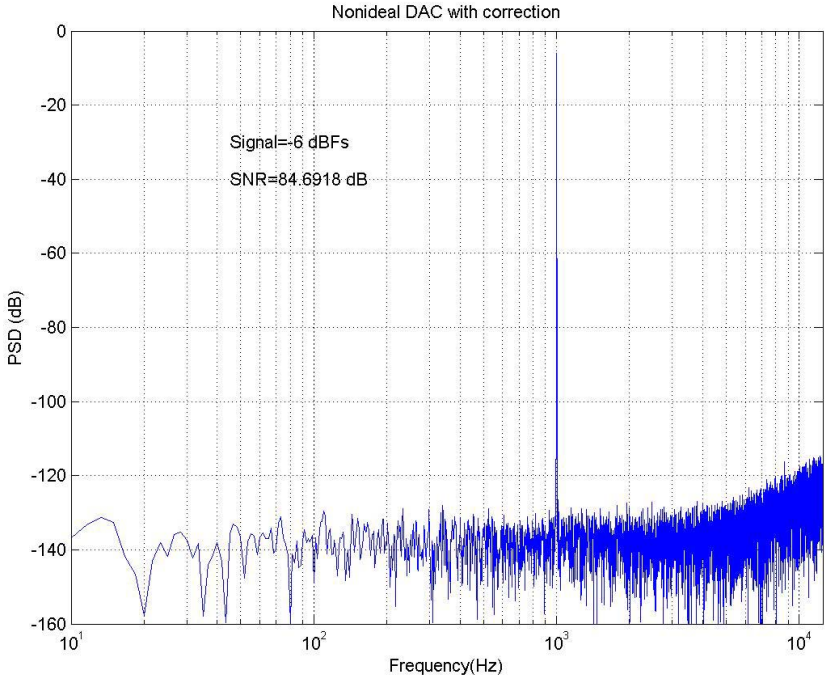


Figure 4-15 3-bit DAC simulation result: proposed correction

Chapter 5 Working with adaptive compensation for noise leakage

5.1 MASH structure and noise leakage

As shown in 4.6.1, in a 2-stage MASH ADC, the complete cancellation of the quantization noise of the first stage relies on the perfect match between the NTF_1 and the digital transfer function $DNTF_1$. The former is implemented by analog circuits, which always have non-idealities, while the latter is accurate and is designed to match the nominal NTF_1. Thus the mismatch between NTF_1 and $DNTF_1$ is inevitable, which means that there will always be some noise leakage.

If NTF_1 is implemented using switched-capacitor circuits, which is most common way to build delta sigma ADCs, the factors that play a critical role in deviate NTF_1 from its nominal expression are capacitor mismatch and finite opamp gain and bandwidth [22]. So the traditional way to minimize the leakage is to carefully lay out the capacitors and design opamps with enough gain and bandwidth. Although improving the capacitor matching becomes easier in advanced technologies, boosting opamp gain becomes even more difficult because the supply voltage is going down. Correlated double sampling (CDS) [23] is a scheme especially for switched-capacitor circuits to enhance the equivalent opamp DC gain. CDS can also cancel low-frequency noise as well as the offset. But CDS requires more switches and capacitors and is basically an analog technique.

5.2 Adaptive compensation for noise leakage

In [24], a novel digital technique compensating for the noise leakage is discussed. It is available for any MASH ADCs, but the description below is based on the 2-stage case. The basic idea is to adaptively adjust $DNTF_1$ to match NTF_1. The adaptation of $DNTF_1$ starts with $DNTF_1$ equals the nominal NTF_1. The noise leakage in the ADC output is detected by a correlation operation. $DNTF_1$ is adapted towards the direction that reduces the noise leakage. The adaptation can be done either every clock cycle or once in a number of clocks and it runs in the background all the time the ADC is on. Eventually *DNTF*1 reaches and stays at the point where the noise leakage is small enough that the adaptation just moves back and forth.

Since the detection of noise leakage is base on a correlation, the impact of the interferences that is correlated with the noise needs to be considered. So a binary random signal, which is called the *test signal*, is injected to the input of the quantizer in the first stage, as shown in Figure 5-1. The detection and adaptation is actually aiming at the test signal instead of the noise itself. Because the test signal goes to the ADC output through exactly the same path as the quantization noise $q_1(k)$, minimizing the test signal in the ADC output is equivalent to minimizing the noise leakage. Since the test signal is uncorrelated with all the interferences, the correlation always gives the right direction for adaptation.

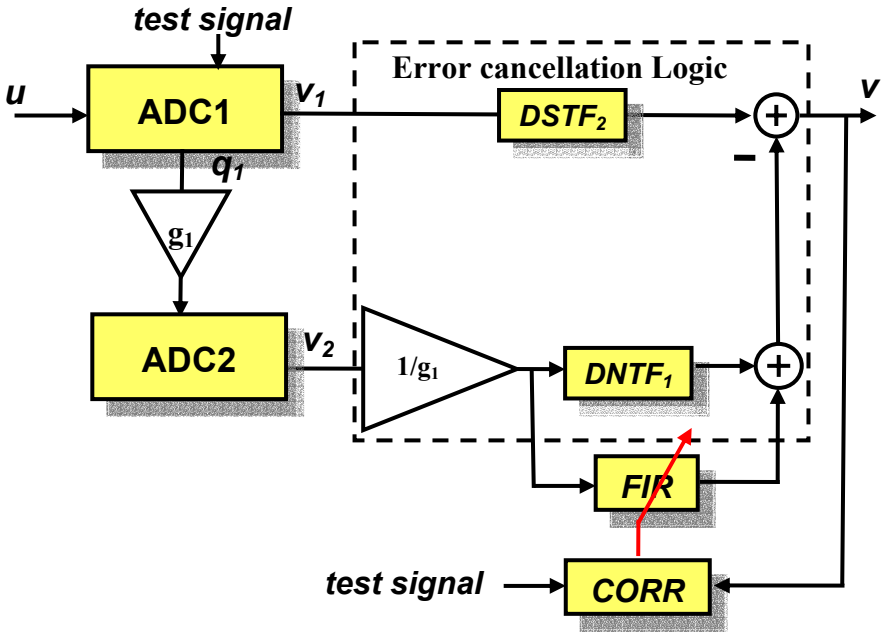


Figure 5-1 Adaptive compensation for noise leakage

5.3 Digital DAC correction working with adaptive compensation

In the simulations of **Chapter 4**, the proposed technique was used in the context of MASH ADCs. Actually, the proposed technique shows its advantage more in MASH ADCs than in single-loop delta sigma ADC. It is of great interest whether the digital DAC correction can work together with the adaptive compensation for noise leakage, which is necessary for high performance MASH ADCs.

Simulations were done to examine the possibility. The same system as in Figure 4-4 are used, except that opamps with 40 dB gain were assumed, resulting

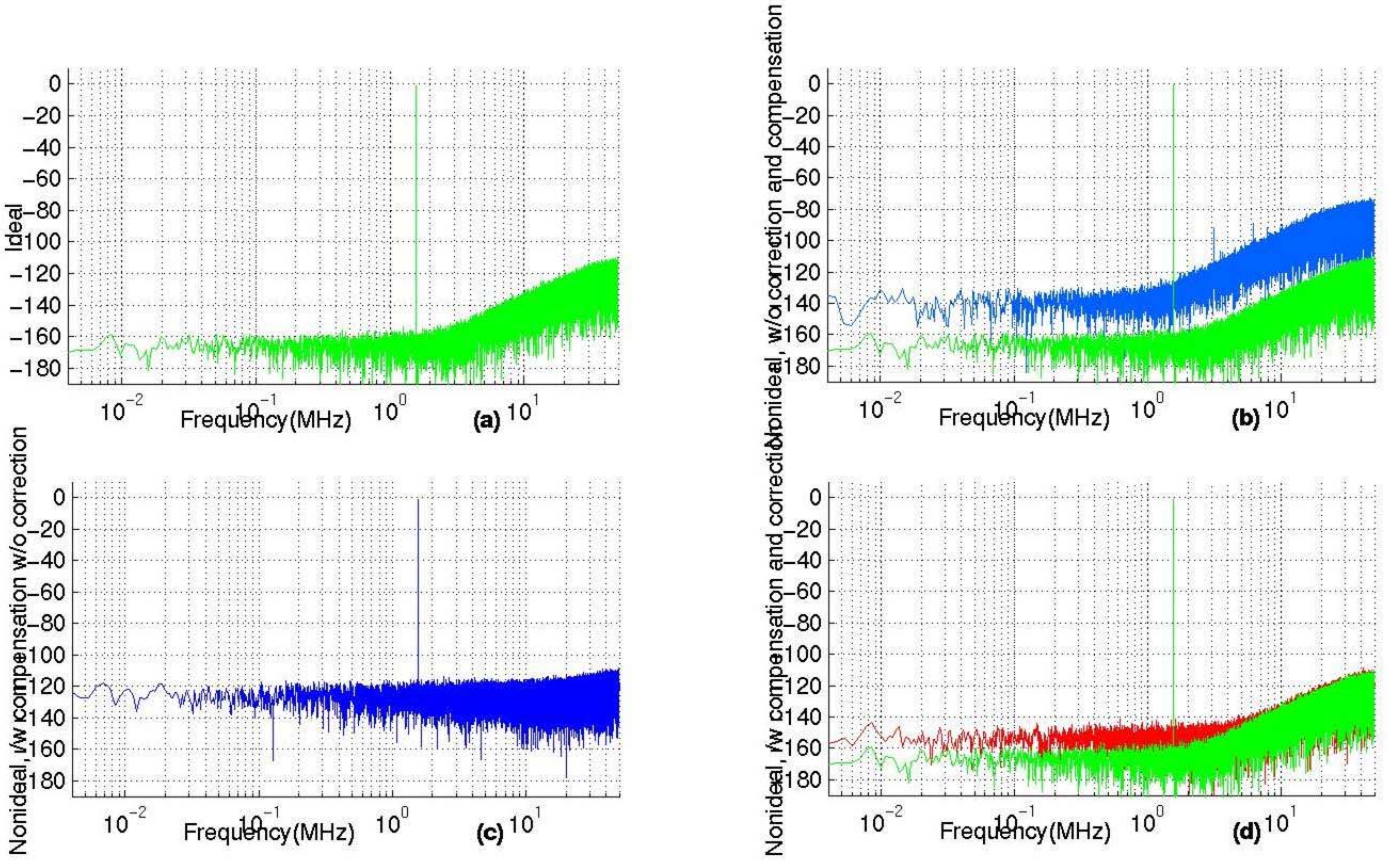
in modified transfer functions. With a 1.56 MHz and -0.92 dB sine-wave input, the output SNDR drops from 101.8 dB in the ideal case (Figure 5-2(a)) to 62.3 dB in the non-ideal case (See Figure 5-2(b), where both the quantization noise leakage and DAC errors were present). After 8 blocks of adaptation, in which each block contained 131,072 clock periods, the leakage was perfectly compensated but the DAC errors were still there (Figure 5-2(c)), resulting in a SNDR of 82.6 dB. A correction process, lasting 131,072 clock periods following the adaptation process, removed the DAC errors and brought the SNDR up to 100.9 dB (Figure 5-2(f)) which is very close to that of the ideal case (also shown). In practice, the adaptation process and the correction process are continuously repeated to track the changing of parameters.

5.4 Conclusion

The possibility of the proposed technique working with the adaptive compensation for the noise leakage was checked.

The principles of adaptive compensation technique were briefly introduced. Then, simulation results were shown to confirm the feasibility of two techniques working together.

Figure 5-2 Simulation results: two techniques work together



Chapter 6 An experimental ADC

6.1 Design motivation and design goals

In addition to computer simulations, hardware verification for the proposed technique needs to be done. So an experimental ADC exploiting the technique was built and tested.

Table 6-1 Specifications for the experimental ADC

Power supply	5 V
OSR	4
Dynamic Range	80 dB
Peak SNDR	74 dB

As long as the technique shows its effectiveness on removing the DAC error and improving the resolution of the experimental ADC under low OSRs, it does not matter what specific speed the ADC is running at and what specific resolution is achieved. Although the proposed technique is eventually designated for high-speed and high-resolution designs, the verification can be done under relatively relaxed specifications.

Based on this motivation, the specifications of the experimental ADC were decided, and are listed in Table 6-1.

6.2 System architecture

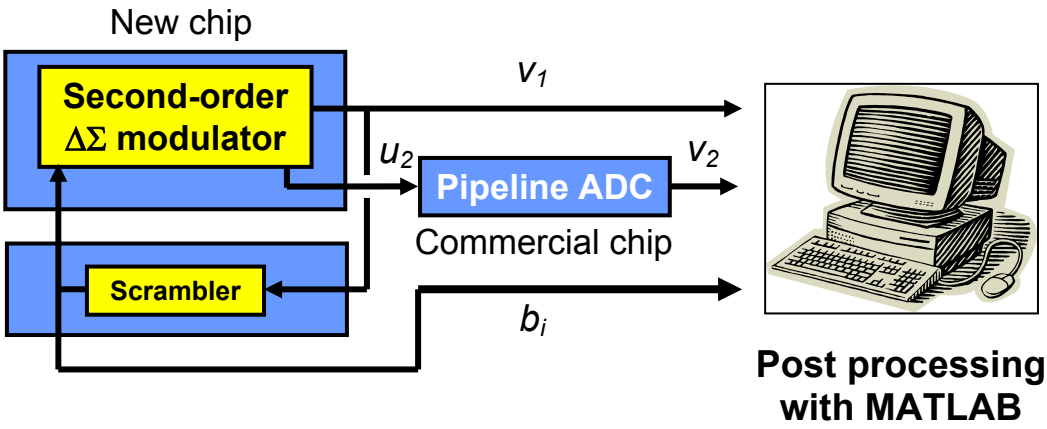


Figure 6-1 Experimental ADC

The experimental ADC is also a 2-0 MASH ADC, similar to the one in Figure 4-4. The inter-stage gain is 4 and the quantizer in the first stage has 9 levels (3 bit). In order to have a flexible realization which can be used to test various versions of the correction technique, instead of a single chip realization, a multi-chip system was built. The first stage was designed and fabricated on one chip using AMIS 1.6 μm CMOS technology. The second stage was not custom designed. A commercial chip from ADI (AD9221) was used. The scrambler, which performs real-time digital processing which can not be done off-line, was built with the butterfly structure [25] shown in Figure 6-2 and was implemented by a group of electronic switches (74LS157). The random number sequences that the scrambler needs were generated by the external arbitrary waveform generator AWG 420 from Tektronix. All other digital processing that was after the output of the two stages, including the error-cancellation logic of the MASH ADC, the

adaptive compensation for noise leakage and the DAC error detection and correction were implemented using MATLAB programs.

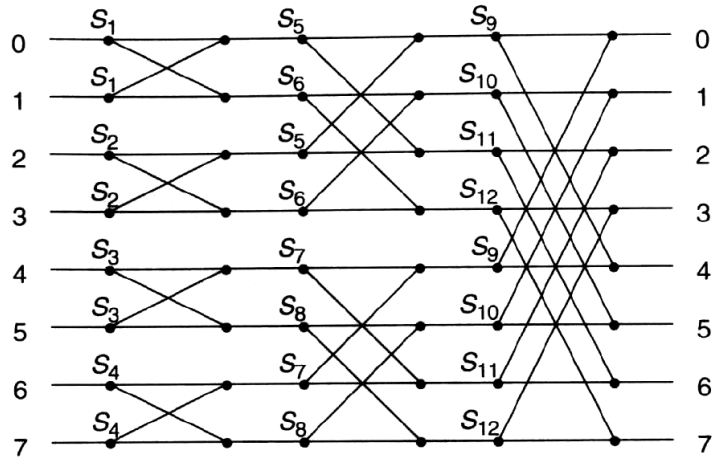


Figure 6-2 Butterfly structure.

6.3 Circuit design

In this section, the circuit details of the first stage are presented. The second-order delta sigma ADC was implemented with switched-capacitor circuits shown in Figure 6-3. Although Figure 6-3 only shows a single ended version, the circuits were actually in fully-differential configuration, which is very common in the circuit design for delta sigma ADCs. Fully-differential circuits are less sensitive to environmental noises because the two halves of the circuit will receive similar noises, and the differential signal is noise-free. Fully-differential circuits can also cancel even harmonics.

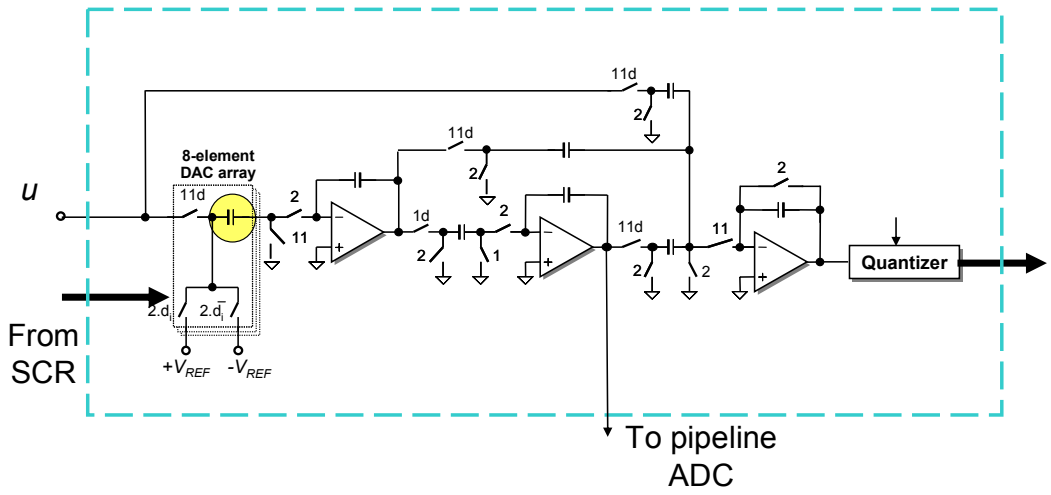


Figure 6-3 Switched capacitor circuits for the 1st stage.

6.3.1 Design of opamps

There are three opamps in the circuit. Two are used in the first integrator and second integrator. The third is used to implement the summing node right before the input of the quantizer.

Table 6-2 Sizes of transistors in opamps

Transistor(s)	Size (W/L in μm)
M1, M2	20/1.6
M3, M4	89.6/1.6
M5, M6	44.8/1.6
M7, M9, M10, M12, M13, M15	224/1.6
M8, M11, M14	448/1.6
MB0, MB1, MB2, MB5	112/1.6
MB3	14.4/1.6
MB4, MB6, MB7, MB8, MB9, MB11	22.4/1.6
MB10	8.8/3.2
MC2, MC3	51.2/1.6
MC1, MC4	12.8/1.6

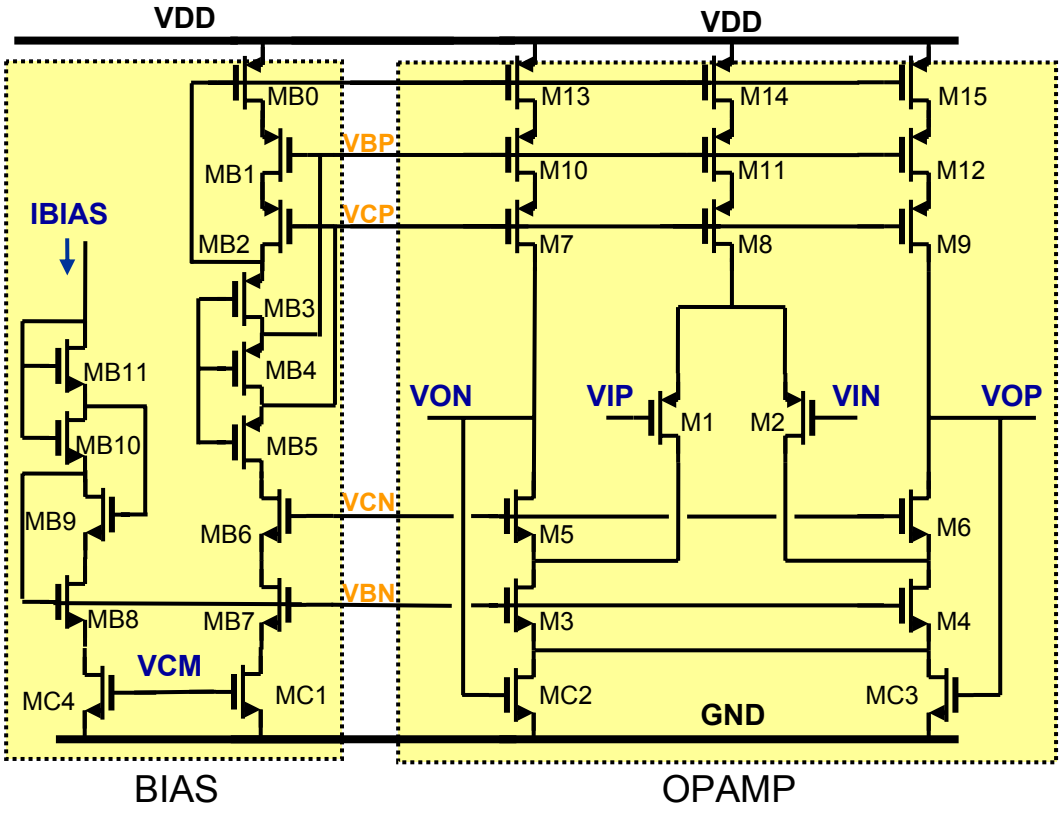


Figure 6-4 Circuit of opamps.

Table 6-3 Simulated specifications of opamps.

DC gain	56.21 dB
Unit gain bandwidth	29.59 MHz
Phase margin	80.54º

All three opamps share the same circuit that is shown in Figure 6-4, no individual scaling for each opamp has been done. A folded-cascode structure was used. The bias voltages were generated by the Sooch circuit. The simulated

frequency response of the opamps is shown in Figure 6-5 and the specifications are listed in Table 6-3.

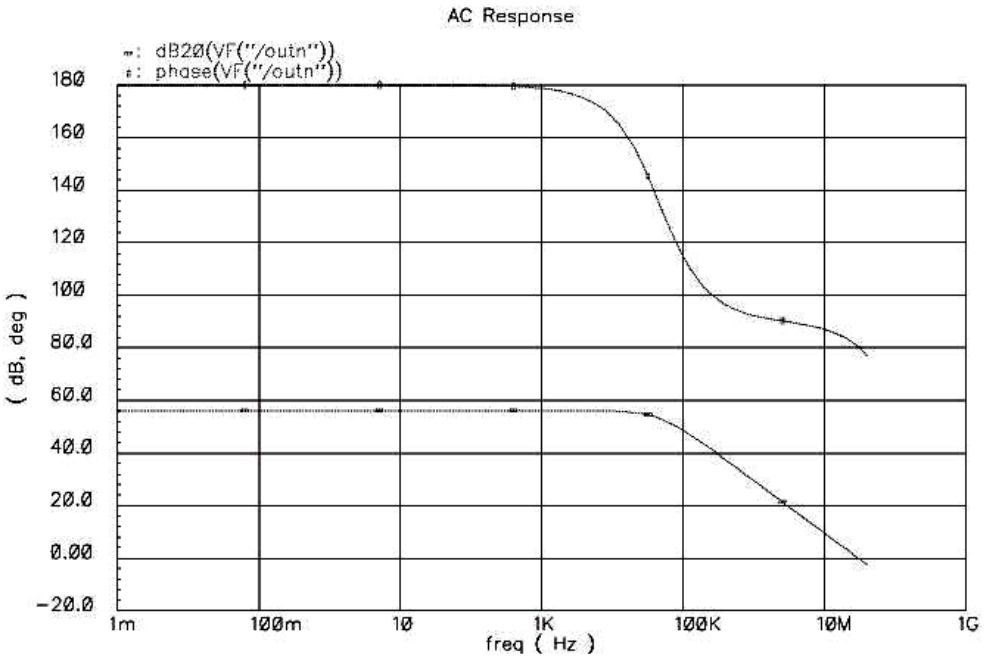


Figure 6-5 Frequency response of opamp.

6.3.2 Size of input sample capacitors

In delta sigma ADCs implemented with switched-capacitor circuits, the size of the input sample capacitors could be a major limiting factor to the resolution achievable. In Figure 6-3, the input sampling capacitor is circled. During both the sampling and the integrating phases, it samples the thermal noise of the two sampling switches connected to it. No matter how large the switch resistances are, the sampled noise power is always kT/C, where C is the capacitor size. To keep the sampled thermal noise under a certain level so that it will not limit the overall resolution, the size of the input sampling capacitor needs to be big

enough. According to the calculation, at least 4 pF input sample capacitor needs to be used on each half of the differential circuit if the thermal noise power is expected to be 85 dB lower than that of the full scale sine wave.

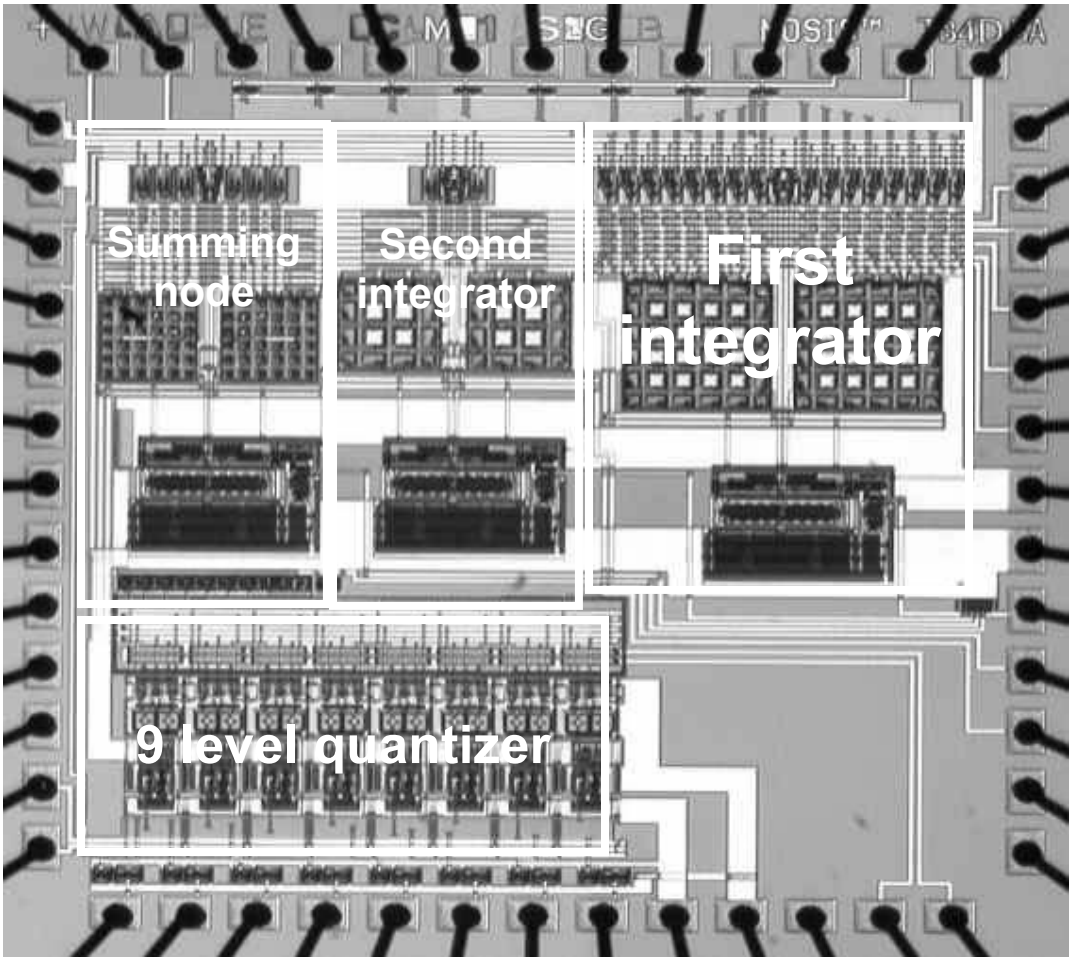


Figure 6-6 Die photo of test chip.

6.4 Measurement results

The die photo of the chip is shown in Figure 6-6. The fully symmetric layout for the opamps, capacitors and switches is to truly realize the differential configuration. The design of the test board is shown in Figure 6-7~Figure 6-9.

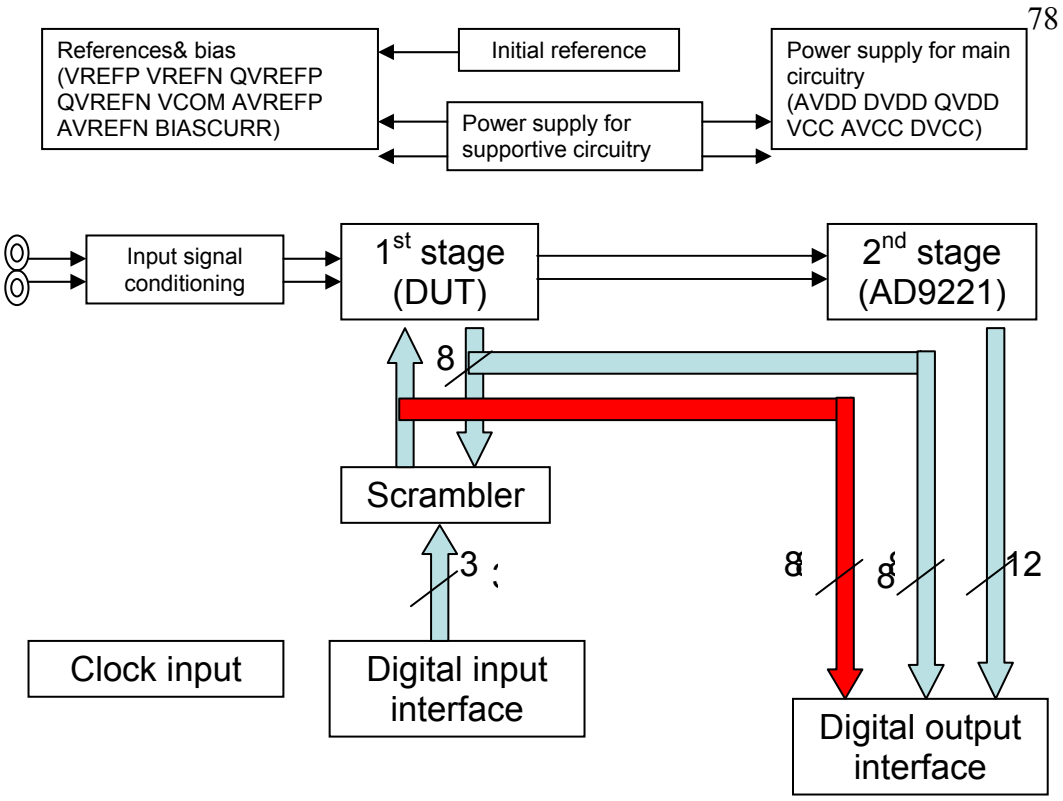


Figure 6-7 Test board design.

The measurement results are shown in Figure 6-10 ~ Figure 6-13. Using a clock rate of 100 kHz, when input signal is a sine wave at 1 kHz and with a amplitude of -6 dB under full scale, without the noise leakage compensation and the proposed DAC correction but with the scrambler functioning, the SNDR of the output of the experimental ADC was 58.6 dB, as shown in Figure 6-10. After the noise leakage compensation was applied, the SNDR went up only to 60.3 dB although an obvious change in the out-of-band noise floor can be observed in Figure 6-11, indicating that in the signal band, the DAC error was dominant. It can be estimated by the result in Figure 6-11 that the unit-element errors are approximately 0.5% RMS. When 1st order DEM was applied to the DAC by controlling the butterfly structure in the scrambler with 1st-order shaped sequences,

the SNDR changed a little to 61.6 dB, corresponding to a output spectrum shown in Figure 6-12 After both the noise leakage compensation and the DAC correction were applied, the SNDR was improved by 12 dB to 72.6 dB. The noise floor was remarkably lowered both in and outside the signal band, as shown in Figure 6-13. It can be observed that the SNDR achieved in Figure 6-13 is worse than that of the ideal case shown in Figure 4-15. The reason behind this difference could be the external noise, the thermal noise of the opamps or the nonlinearity of the opamps.

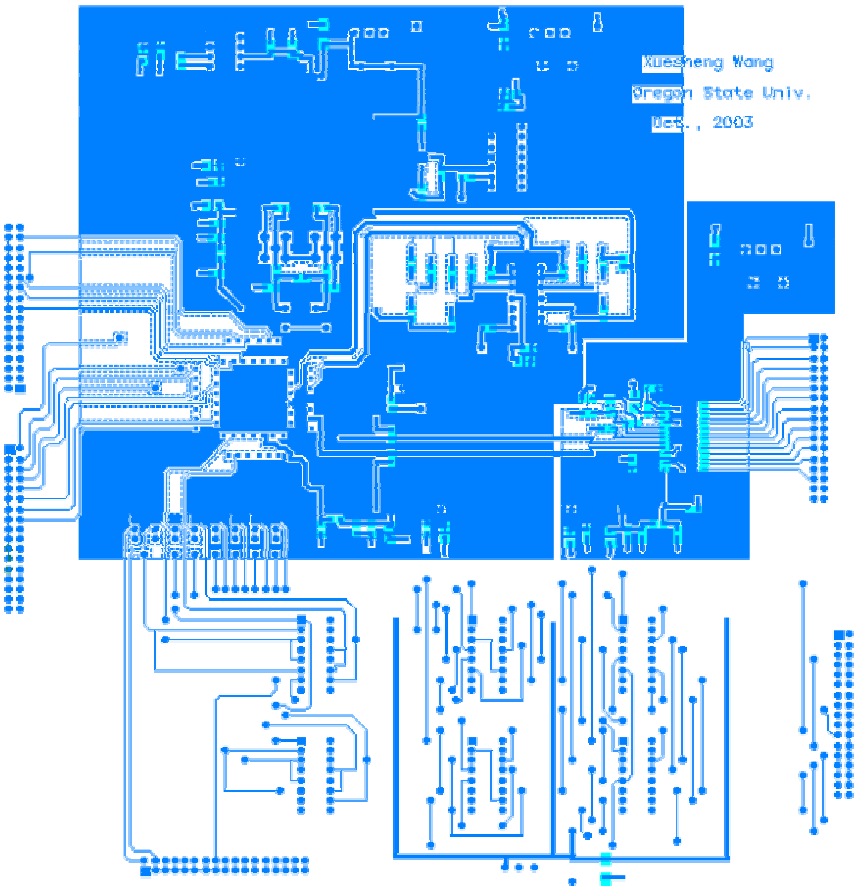


Figure 6-8 Layout of test board: top layer

Additional measurements were carried out with different amplitudes of the input signal. Figure 6-14 shows a summary of the results. For input amplitudes below -2.5 dBFS, the SNDR results for the correlation-based correction technique were better by about 12 dB than those for the first-order mismatch error shaping.

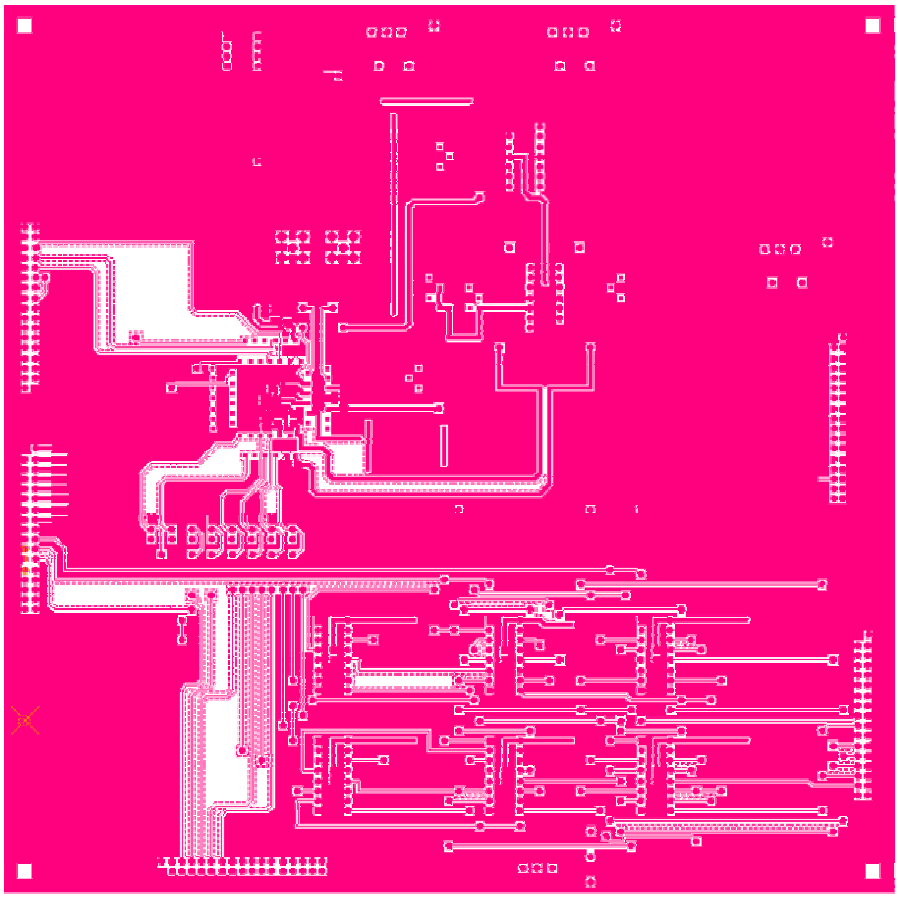


Figure 6-9 Layout of test board: bottom layer

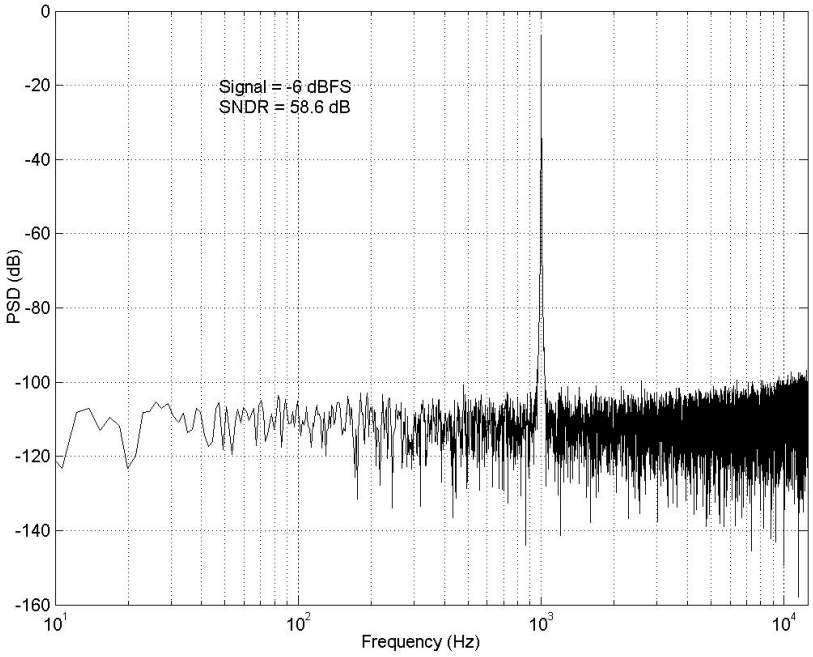


Figure 6-10 Measurement results: output without compensation for noise leakage or DAC correction

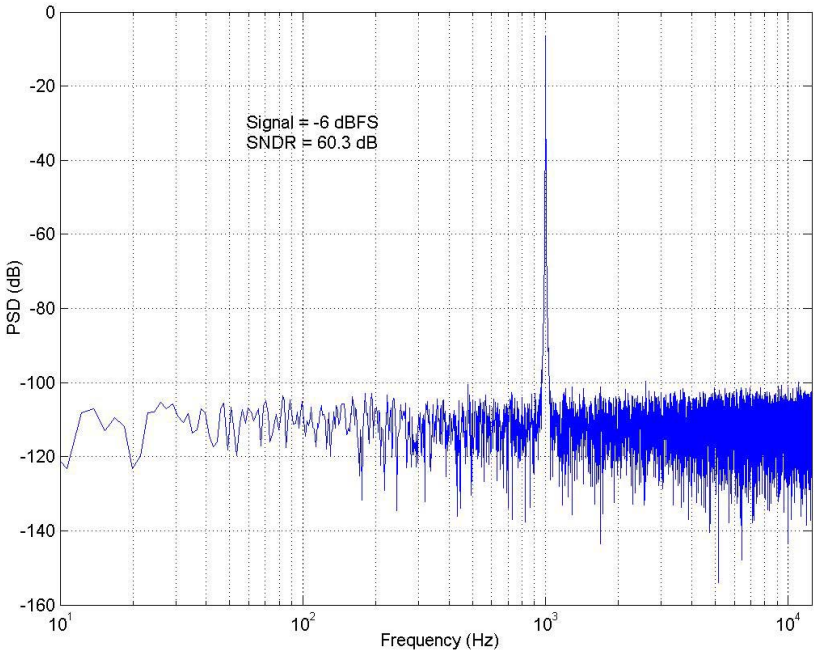


Figure 6-11 Measurement result: output with compensation for noise leakage without DAC correction.

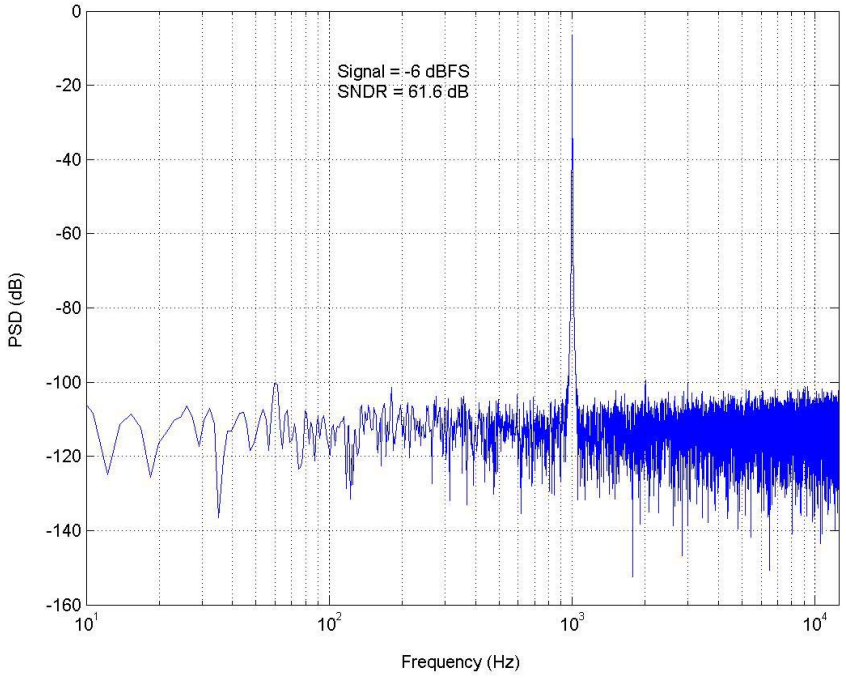


Figure 6-12 Measurement result: output with compensation and 1st order DEM

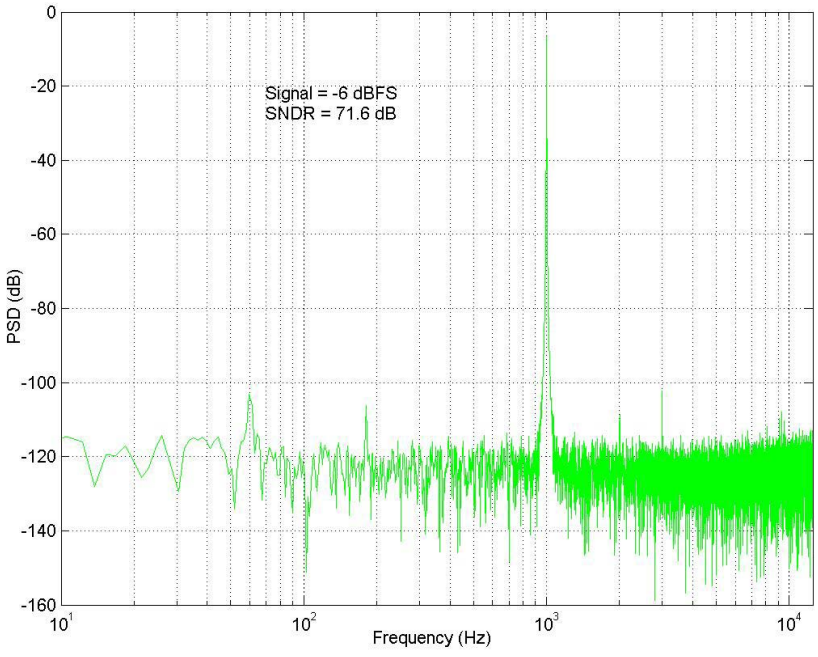


Figure 6-13 Measurment result: output with both compensation for noise leakage and DAC correction

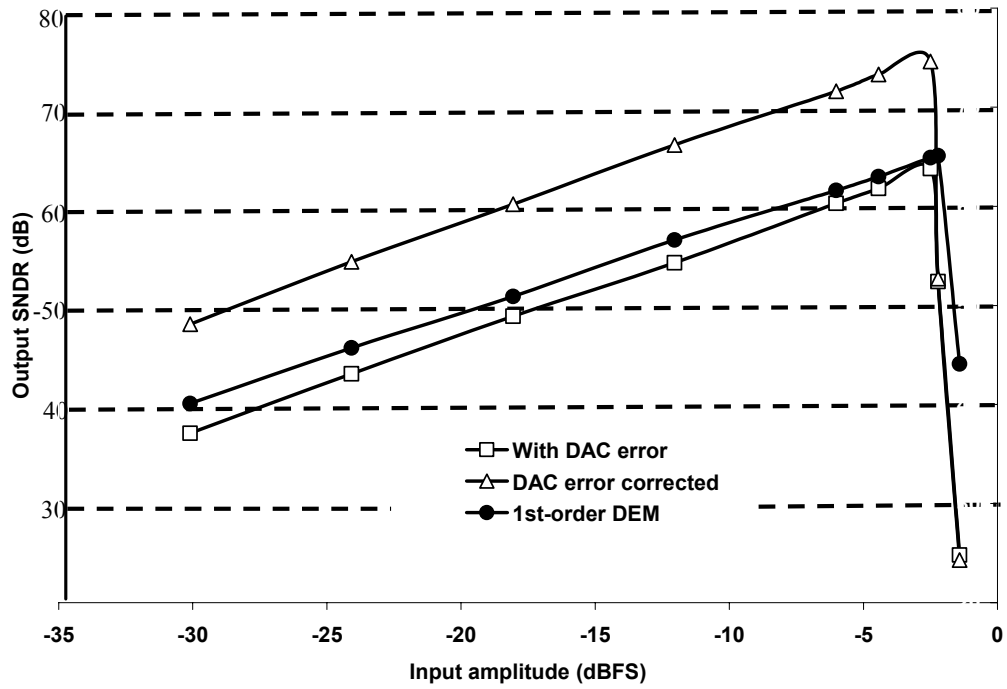


Figure 6-14 SNDR vs. input signal amplitude

6.5 Conclusion

An experimental ADC was built to verify the proposed DAC correction technique. The first stage of the ADC was designed and fabricated in one chip; other parts were either implemented with commercial chips or implemented off-line with computer programs. Measurements showed that the proposed technique worked well in the experimental ADC, proving the feasibility and effectiveness of the DAC correction technique in practical circuits of integrated form.

Chapter 7 Summary and future work

7.1 Summary

In this dissertation, a novel fully digital technique was proposed to detect and correct the DAC error in multi-bit delta sigma ADCs. Many associated topics have been examined in detail. These include:

1. The principle of delta sigma ADCs, the reason of choosing multi-bit quantization over single-bit quantization.

2. Modeling of the output error of the internal DAC based on unit-elements and the impact of the error on the ADC performance.

3. Analysis of the current techniques dealing with the DAC error, with their drawbacks pointed out.

4. Simulation of the proposed technique with the adaptive compensation for the noise leakage in MASH ADCs. The two techniques were shown to be able to work together, paving a road to design high performance ADCs with coarse analog circuits.

Finally, an experimental ADC was designed and tested. The measurement results proved the feasibility and effectiveness of the proposed technique in practical circuits of integrated form.

7.2 Future work

So far all the digital processing except for the scrambler was implemented by computer programs with almost infinite accuracy both in the simulation or the test of the experimental system. The effect of limited word length on the accuracy of DAC error detection and correction is of great interest.

The topic of designing low power, low voltage and low cost VLSI specific for the DAC correction technique is very important. For instance, the correlator is the core of the proposed technique. Structures that can efficiently implement it should be studied.

It is possible that the DAC correction technique be applied in data converters other than delta sigma ADC. Actually, MASH ADCs are similar to pipelined ADC in several ways, so one of the natural extensions of the proposed technique will be in that direction.

Bibliography

[1] D. A. Kerth, D. B. Kasha, T. G. Mellissionos, D. S. Piasecki, and E. J. Swanson, "A 120 dB linear switched-capacitor delta-sigma modulator." in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers,* February 1994, pp. 196-197.

[2] Y.Matsuya *et al.*, "A 16 b oversampling A-to-D conversion technology using triple-integration noise shaping," *IEEE J. Solid-State Circuits,* vol. SC-22, pp. 921-929, Dec. 1987.

[3] I. Fujimori *et al.*, "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8x oversampling," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1820—1828, Dec. 2000.

[4] K. Vleugels, S. Rabii and B. Wooley, "A 2.5 V Sigma-Delta Modulator for Broadband Communications Applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1887—1899, Dec. 2001.

[5] Y. Geerts, M. S. J. Steyaert, and W. Sansen, "A high-performance multibit delta-sigma CMOS ADC", *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1829-1840, Dec. 2000.

[6] Eric Fogleman, Jared Welz, Ian Galton; "An audio ADC delta--Sigma modulator with 100-dB peak SINAD and 102-dB DR using a second-order mismatch-shaping DAC", *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 339-348, March 2001.

[7] R. T. Baird and T. S. Fiez, "A low oversampling ratio 14-b 500-kHz ΔΣ ADC with a self-calibrated multibit DAC**",** *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 312 -320, March 1996.

[8] F. Chen and B. H. Leung, "A high resolution multibit sigma-delta modulator with individual level averaging," *IEEE J. Solid-State Circuits*, vol. 30, no. 4, pp. 453 -460, Aug. 1997.

[9] A. Yasuda, H. Tanimoto and T. Iida; "A third-order Δ-Σ modulator using second-order noise-shaping dynamic element matching," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1879-1886, Dec. 1998.

[10] U. K. Moon, J. Silva, J. Steensgaard, G. C. Temes, "A switched-capacitor DAC with analog mismatch correction." *Proceedings of The 2000 IEEE International Symposium on Circuits and Systems,* vol. 4, pp. 421-424, May 2000

[11] M. Sarhang-Nejad, *Realization of a High-Resolution Multibit Sigma-Delta Analog/Digital Converter*, Ph.D. thesis, University of California, Los Angeles, 1991.

[12] P. Kiss, U. Moon, J. Steensgaard, J. T. Stonick, and G. C. Temes, **"**Multibit delta-sigma ADC with mixed-mode DAC error correction," *Proceedings of the IEEE International Symposium on Circuits and Systems*, 8 May 2001, pp. I.280–I.283.

[13] C. Petrie and M. Miller, "A background calibration technique for multibit delta-sigma modulators", *Proceedings of the 2000 IEEE International Symposium on Circuits and Systems,* vol. 2, pp. 29-32, May 2000.

[14] Paul Gray, *Possible Analog IC Scenarios for the 90's*, presentation slides.

[15] S. R. Norsworthy, R. Schreier, G. C. Temes, *Delta-Sigma Data Converters*, IEEE Press, Piscataway, NJ, 1997.

[16] J. C. Candy and G. C. Temes, *Oversampling Delta-Sigma Data Converters*, IEEE Press, New York, 1992.

[17] A. V. Oppenheim *et al*, *Signals and Systems*, Prentice Hall; 2nd edition, August 6, 1996.

[18] J. Steensgaard, *Adaptive delta-sigma modulator*, Technical report, Oregon State University, Department of Electrical and Computer Engineering, August 2000.

[19] X. Wang, U. Moon, M. Liu, and G. Temes, "Digital correlation technique for the estimation and correction of DAC errors in multibit MASH delta-sigma ADCs", *IEEE Int. Symp. Circuits Syst.*, vol. IV, pp. 691-694, May 2002.

[20] J. Silva, U. Moon, J. Steensgaard and G.C. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electronics Letters*, vol. 37, no. 12, pp. 737—738, June 2001.

[21] Richard Schreier, "The delta-sigma toolbox 5.1 for Matlab 5.0," Matlab code and documentation, April 1998, available on the official website of Mathworks.

[22] P. Kiss, *Adaptive Digital Compensation of Analog Circuit Imperfections for Cascaded Delta-Sigma Analog-to-Digital Converters*, PhD thesis.

[23] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effect of op-amp imperfection: autozeroing, correlated double sampling, and chopper stabilization," *Proc. of the IEEE*, Nov. 1996, pp. 1584-1614.

[24] P. Kiss, J. Silva, A. Wiesbauer, T. Sun, U. Moon, J. T. Stonick, and G. C. Temes, "Adaptive correction of analog errors in MASH ADCs – Part II. Correction using test-signal injection," *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 47, pp. 629–638, July 2000.

[25] Robert Adams, Khiem Q. Nguyen, Karl Sweetland; "A 113-dB SNR oversampling DAC with segmented noise-shaped scrambling", *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1871-1878, December 1998.