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A 1V 10b 60MS/s Hybrid Opamp-Reset/Switched-RC Pipelined ADC

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Abstract— **The fully differential Opamp Reset Switching Technique (ORST) for low voltage applications is presented. The technique is demonstrated in a 1V, 10-bit, 60MS/s pipelined ADC where a hybrid ORST/Switched-RC topology is adopted for improved accuracy at low voltage supplies and achieves 50dB SNDR in 0.18μm CMOS while dissipating 34mW. The architecture also uses a passive input track-and-reset to save power and has an input bandwidth greater than 90MHz.**

I. Introduction

Scaling of CMOS processes demands lower supply voltages, requiring new techniques to circumvent the floating switch, reduced headroom, and insufficient opamp performance issues in data converters. The Opamp Reset Switching Technique (ORST) has been shown to avoid floating switch non-linearity in multi-amplifier, switched capacitor ADCs using the previous stage amplifier to reset sampling capacitors instead of using CMOS switches. The technique has been demonstrated with pseudo-differential architectures for Δ-Σ [1], pipelined [2], and two-stage algorithmic [3] ADCs but each lack the advantages of a fully differential structure.

This paper proposes adopting a fully differential ORST topology to further suppress distortion and improve supply rejection of the converter at low supply voltages. This is accomplished by addressing the inherent switching common-mode of the ORST and applying fully differential techniques.

Section II reviews the traditional Opamp Reset Switching Technique and presents the proposed fully differential topology. Section III more specifically covers the circuit design aspects of a pipelined ADC utilizing the fully differential hybrid ORST/Switched-RC. Section IV presents measured results from the fabricated chip, and section V finishes with concluding remarks.

II. Opamp Reset Switching Technique

A. Pseudo Differential ORST

A basic, single ended ORST structure is shown in Fig. 1. During ϕ_1 the signal from stage $k-1$ is sampled onto C_s. During ϕ_2, the $k-1$ amplifier resets in a unity gain configuration to a defined reference using a feedback switch, pushing the signal charge from C_s onto C_f. Thus the series floating switch that isolates the stages and the shunt switch to reset C_s, which are present in traditional switched-capacitor configurations, are no longer needed. This allows the circuit to operate at very low voltages and high speeds.

To ensure that the amplifier resets quickly, the feedback reset switch that places the amplifier in unity feedback requires a large overdrive voltage for sufficient conductance, therefore the reset output value of the amplifier must be near ground during the reset. Viewed differentially, the reset mode of the amplifier outputs require a common-mode shift, switching between mid-rail during amplification to near-ground during the reset mode. The traditional ORST uses a pseudo-differential topology to directly apply this single-ended, unity feedback reset.

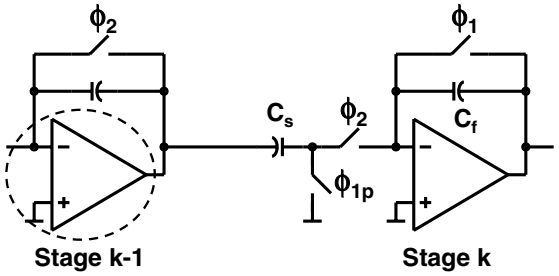

Fig. 1. Basic ORST configuration

B. Fully Differential ORST

Fully differential circuits can be reset with switches similar to their pseudo differential counterparts by placing the amplifier in a unity configuration with additional common-mode feedback (CMFB) circuitry to control the output common-mode. The latter uses the reference terminals of the amplifiers to define the output common-mode, while the former requires a mechanism within the CMFB loop to switch the common-mode between phases. The key challenge of attaining a fully differential ORST topology is designing a fast, switchable CMFB circuit. This paper proposes using true fully differential amplifiers with such a CMFB circuit.

This may at first appear to be a power/complexity penalty because the pseudo differential approach does not need the CMFB circuitry. Yet after noting that the pseudo-differential ORST requires two amplifiers that are differential to establish a virtual ground reference, the power consumption of the fully differential ORST is actually comparable to the pseudo differential structure.

Instead of a unity gain reset, the proposed fully differential ORST technique uses resistive feedback during the reset similar to [3]. As shown in Fig. 2 the feedback factor of the amplifier can be similar during both amplification and reset, allowing both phases to have comparable settling times.

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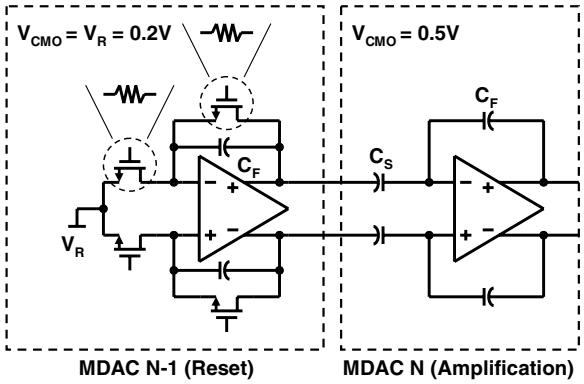

Fig. 2. Resistive feedback during reset

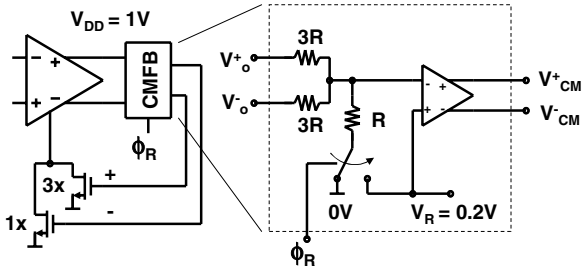

Fig. 3. Switching common-mode feedback

To avoid floating switches in switched capacitor CMFB implementations, a continuous-time approach is used. The switching mechanism that enables the fully differential ORST is shown in Fig. 3. The CMFB uses resistive common-mode sensing with a level shifting shunt resistance to drop the signal level before being applied to the input pair of the common-mode amplifier. Using a set of switches that toggle the level shifting resistor between ground and a low reference (V_R), and designing a proper ratio between the sensing and level-shifting resistors, the output common-mode of the amplifier switches between 0.2V and 0.5V for the reset mode and amplification phase, respectively, when using a 1V supply. This switching mechanism does not affect the characteristics of the CMFB loop, allowing similar settling for the rising and falling common-mode transients.

The CMFB loop is stabilized with adequate speed by using minimum length devices, properly sizing the common-mode amplifier, and using a gain reduction technique for stabilization described in section III. Sufficient common-mode settling time is achieved by designing the CMFB loop bandwidth to be approximately equal to the differential loop bandwidth. This occurs when the gain reduction through the CMFB circuit is equal to the feedback factor of the MDAC.

III. Circuit Design

The fully differential ORST is implemented in the design of a 10-bit pipelined ADC with 1.5-bit stages. Stages are scaled down the pipelined to conserve power, but each utilizes the ORST technique for low-voltage operation. To additionally

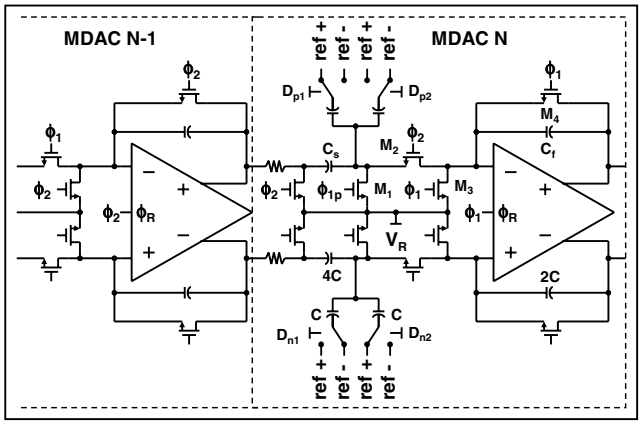

Fig. 4. Fully differential ORST MDAC for a pipelined ADC

save power, a simple, passive, track-and-reset is used at the front end instead of a dedicated sample-and-hold.

A. MDAC

The full MDAC of a stage in the ADC is shown in Fig. 4. M_1 stores the previous stage residue during the sampling instant while M_3 and M_4 provide the resistive feedback during the reset phase to mimic the capacitive feedback of the amplification phase. Additional M_2 switches provide isolation between the sampling and reset portions of the MDAC during the sampling/reset phase.

The direct connection between stages inherent to the ORST forces the residue settling time to be dependent on both the reset and amplifying structures, resulting in slower operation. Noise from the reset opamp is also undesirably amplified through to the residue. Acknowledging that the output voltage of the reset stage is well defined, a switched-RC [4] structure that resets to the same reference is used in series between the stages to improve the reset settling time and attenuate noise from the previous stage. The switched-RC block is reset only while the previous stage opamp is in the reset mode and does not interfere with the normal residue transfer between the stages.

At low voltages, the sampling capacitors cannot double as DAC capacitors so additional reference injecting capacitors are used, resulting in a feedback factor of about $1/5$ and capacitor spread of $4{:}1$. The ϕ_R terminals of the opamps indicate the CMFB switching mechanism controlled by one of the non-overlapping clocks.

B. Track and Reset

An input circuit is required to perform the reset for the first stage. To save power as well as to avoid noise and non-linearity from an active sampling device, a simple track-and-reset (T/R) is used, allowing an input signal bandwidth of more than 90MHz. A single ended depiction of the T/R is shown in Fig. 5. The cascade of R-MOSFET blocks allows passive sampling of the input signal by the first stage during its sampling phase and resets the sampling capacitor while attenuating the input signal during the amplification phase. The

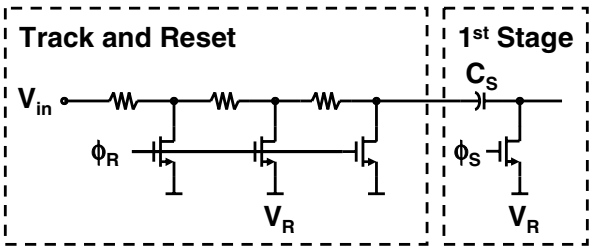

Fig. 5. Input track and reset

reset voltage reference used in the T/R is the same reference used by the CMFB and interstage switched-RC blocks. Small signal feedthrough due to finite attenuation of the input signal creates no distortion because it is corrected by redundancy, but it does lead to a small shaping of the overall ADC transfer function.

Using only passive devices, the T/R can operate with a rail-to-rail input signal range. For an equivalent SNR, increasing the input range by two while decreasing the first stage gain allows a decrease of the input sampling capacitance by four. For a 1V supply, this design allows a rail-to-rail 2Vpp differential signal while benefiting from the reduced sampling capacitance and increased feedback factor of the first stage.

Many tradeoffs exist in the design of the T/R. On one hand, the total series resistance must be large enough to sufficiently attenuate the input signal during the reset and to avoid excessive loading of the ADC driver during reset mode. On the other hand, resistance must be small enough to provide adequate input bandwidth and to allow recovery from the reset mode quickly. The shunt switches must also be a reasonable size to not add distortion to the rail-to-rail signal due to non-linear drain capacitances.

High frequency signal integrity without a sample-and-hold is assured using a 1.5-bit stage with maximum redundancy range and a fast dynamic latch in the sub-stage ADC to minimize sampling skew and bandwidth mismatch errors between the MDAC and sub-ADC paths. This design demonstrates little change in distortion (SFDR) measured up to a 90MHz full-scale input.[1]

C. Operational Amplifier

A two-stage, folded cascode opamp shown in Fig. 6 is used to operate at low voltages with gain boosting to offset the loss of transistor output impedances due to using all minimum length devices and tight biasing. A PMOS input pair is chosen to allow NMOS switches in the MDAC and for low flicker noise.

Cascode compensation is chosen to avoid the forward zero path and to improve supply rejection while providing a wide bandwidth. The output common-mode voltages are controlled by the NMOS current source of the first stage and the V_{gs} of the second stage input device sets the output common-mode of the first stage.

[1]Clean measurements were only possible up to 90MHz due to lack of input signal filters.

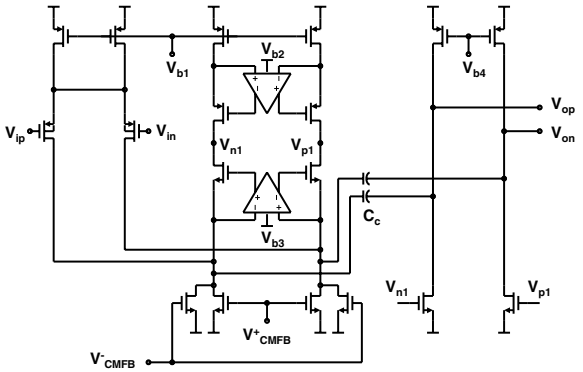

Fig. 6. Two-stage, gain boosted opamp

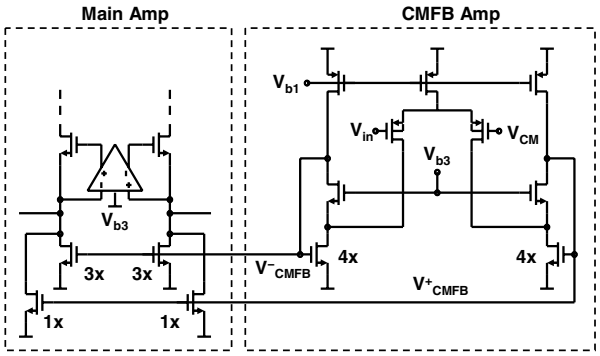

Fig. 7. CMFB loop gain reduction using positive feedback

D. Common-Mode Feedback

The common-mode amplifier is a scaled, low-gain replica of the opamp first stage to ensure reasonable current mirroring into the opamp despite using minimum length transistors. To reduce the gain around the CMFB loop and improve stability, the NMOS control in the opamp is split. Instead of creating another replica to DC bias a part of the split NMOS, differential control of the common-mode is accomplished by using the already available positive feedback terminal from the common-mode amplifier as shown in Fig. 7.

With the proper cancellation between negative and positive feedback paths, the gain can be reduced without any added power or complexity. This design uses one quarter of the NMOS control for positive feedback, resulting in a gain reduction of two.

IV. Measured Results

The prototype fully differential hybrid ORST/Switched-RC pipelined ADC was fabricated in a 0.18μm CMOS technology. Fig. 11 is a die photo of the implemented architecture. With a 1V supply, the ADC demonstrates speeds up to 60MS/s for 34mW total power and a 51.4dB SNR for a -1.5 dB input signal at 500kHz as shown in Fig. 9. Performance for varying input frequencies at a 60MS/s sampling rate is shown in Fig. 10 which demonstrates the effective use of the T/R with wide input bandwidth. Fig. 8 shows the DNL as +0.4/-0.7 LSB and INL as +1.5/-2.7 LSB. The limited distortion

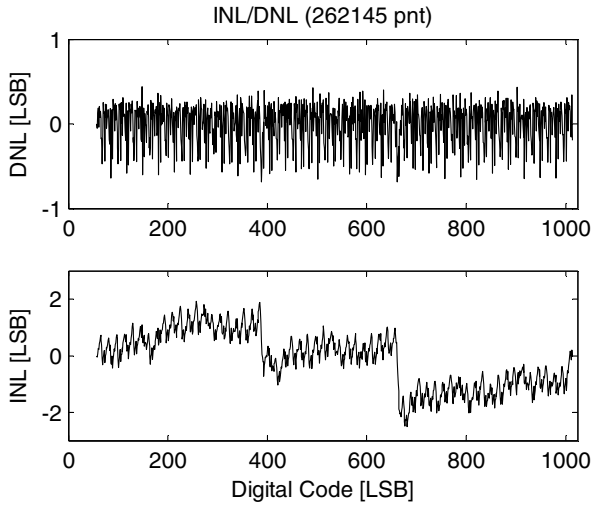

Fig. 8. DNL and INL

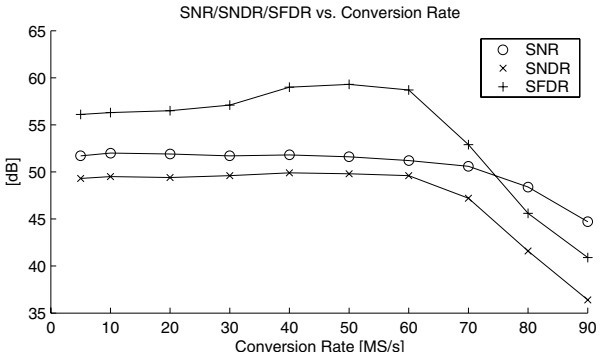

Fig. 9. Performance vs. conversion rate

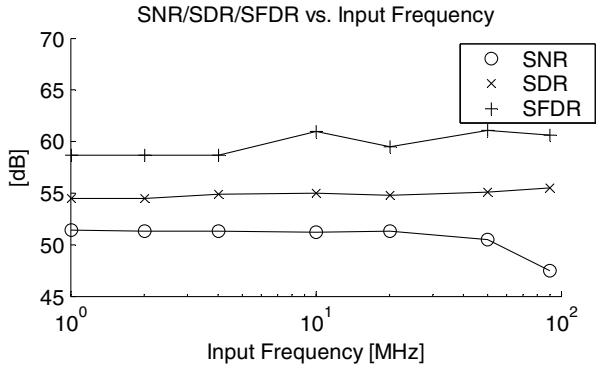

Fig. 10. Performance vs. input frequency

performance apparent in the INL and SFDR is suspected to be due to insufficient opamp gains in the fabricated design.

V. Conclusion

The design of a 1V, 10-bit pipelined ADC using a fully differential hybrid ORST/Switched-RC topology has been presented. Fully differential ORST allows low voltage operation by avoiding critical floating switches while benefiting from fully differential structures as opposed to a pseudo-differential implementation. The active die area of the chip occupies 1.44mm^2, dissipates 34mW at a 60Ms/s sampling rate, and achieves a 50dB SNDR.

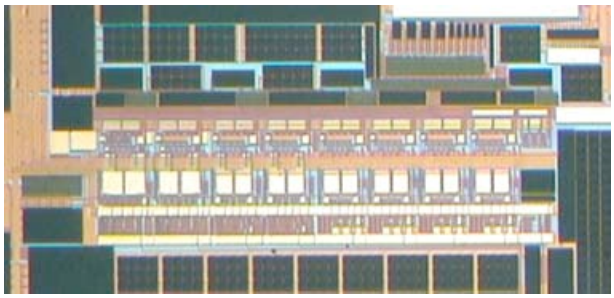

Fig. 11. Die photograph

TABLE I
Performance Summary

Technology	0.18 μm CMOS
Supply Voltage	1.0 V
Fs	60 MS/s
DNL	+0.4/-0.7 LSB
INL	+1.5/-2.7 LSB
SNR Vin = -1.5 dBfs @ 0.5/50 MHz	51.4/50.4 dB
SFDR Vin = -1.5 dBfs @ 0.5/50 MHz	58.8/61.1 dB
SNDR Vin = -1.5 dBfs @ 0.5/50 MHz	49.7/49.3 dB
Power consumption	34 mW
Die area	1.8 $\times$ 0.8 mm^2

Acknowledgments

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