A Sub 1-V Constant G_m–C Switched-Capacitor Current Source

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***Abstract*—A switched-capacitor bias that provides a constant G_m–C characteristic over process and temperature variation is presented. The bias can be adapted for use with subthreshold circuits, or circuits in strong inversion. It uses eight transistors, five switches, and three capacitors, and performs with supply voltages less than 0.9 V. Theoretical output current is derived, and stability analysis is performed. Simulated results showing an op-amp with very consistent pulse response are presented.**

***Index Terms*—Constant G_m–C, constant transconductance, G_m–C filters, switched-capacitor current source.**

I. Introduction

THE "constant transconductance" bias (also known as a beta-multiplier) shown in Fig. 1 is popular because a MOSFET biased from this source will have a transconductance (approximately) proportional to $1/R$ regardless of MOS process corners, power supply voltage, and temperature (PVT) [1], [2]. This bias was originally intended for a resistively loaded MOS differential pair [4]. When used in this application, the gain will be $G_M \cdot R_{\mathrm{LOAD}} = R_{\mathrm{LOAD}}/R$, which is well controlled over PVT if the resistors are of the same type.

The bias is also used ubiquitously for operational amplifiers, but it is not the best choice because the resulting operational amplifier's bandwidth (i.e., G_m–C) will be proportional to $1/RC$, where R is the resistor used in the bias and the C is the amplifier's compensation capacitance. Accordingly, the operational amplifier bandwidth will vary as much as $\pm 50\%$ over resistor and capacitor corners. In addition, the bias current is proportional to $1/R^2$ so parameters such as slew rate and power consumption can vary much more than $\pm 50\%$. Even if an external resistor is used, operational amplifier performance will be inversely proportional to process dependent internal capacitance values.

Various master/slave tuning techniques can be used [3], [5], [6], [9], but a more compact choice is to realize the resistance in the bias using a switched-capacitor resistor. This is shown conceptually in Fig. 2 [1]. A pMOS operational amplifier biased with this source will have a bandwidth determined by capacitor ratios and a clock frequency. These parameters are well controlled, and the resulting amplifier bandwidth will be essentially independent of process corners. Among other things, this makes the amplifier considerably easier to design. Unfortunately, the topology shown in Fig. 2 has too much ripple to be practical. There are other subtle problems such as body effect and unmatched drain–source voltages that limit the practicality of this circuit. A practical realization of a constant G_m–C bias is the subject of this brief. The circuit is described in Section II. Stability is addressed in Section III, and Sections IV–VI show simulated results of a complete circuit.

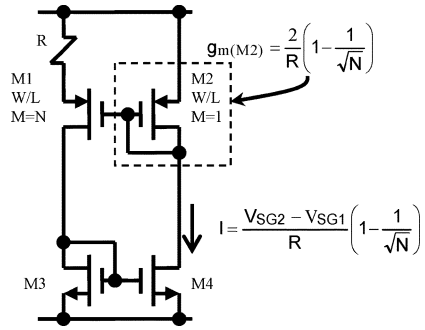

Fig. 1. Classical "Constant Transconductance" bias.

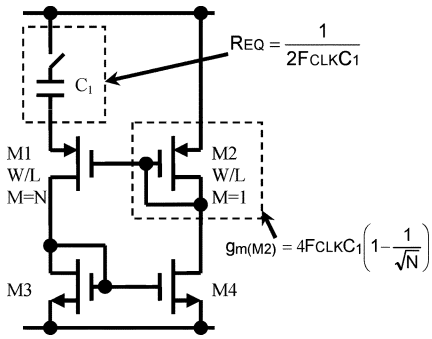

Fig. 2. Constant G_m–C bias.

II. Practical Switched-Capacitor Current Source

The circuit shown in Fig. 3 is a practical way to generate a current equivalent to that produced with a switched-capacitor resistor. It is similar to circuits reported in [7]–[9]. The operation is as follows. There are two nonoverlapping phases: $\phi 1$ and $\phi 2$. During $\phi 2$, the capacitor C_1 is discharged completely. At the same time, C_2's voltage is forced to V_{REF} by the virtual ground. During $\phi 1$, the output of the operational amplifier provides a constant voltage to the gate of $\mathrm{M4}$, which, in turn, provides a constant current to C_1 and C_2 via the mirror $\mathrm{M1}$ and

Manuscript received July 20, 2006; revised September 22, 2006. This work was supported by the Semiconductor Research Corporation under Contract 2005-HJ-1308. This paper was recommended by Associate Editor G. Manganaro.

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Digital Object Identifier 10.1109/TCSII.2006.889446

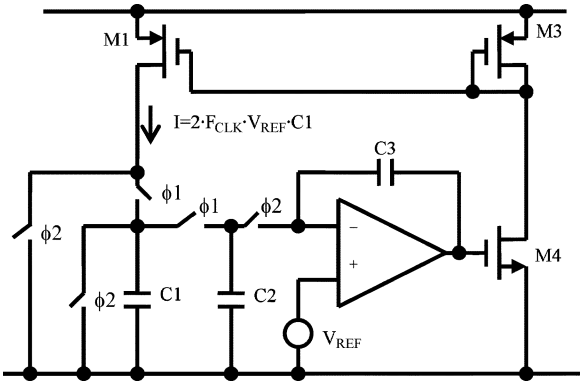

Fig. 3. Practical switched-capacitor current source.

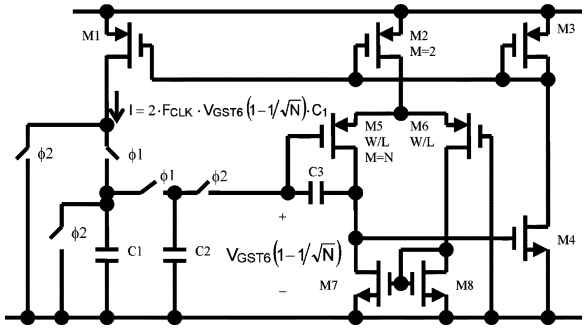

Fig. 4. Compact circuit to generate constant G_m–C bias using a current density mismatch in M5 and M6 to create a reference voltage. V_{GST6} is $V_{\mathrm{GS6}} - V_{T6}$.

M3. Accordingly, the voltage across C_1 and C_2 ramps linearly, and at the end of $\phi 1$, its value is

$$V(C_2) = \frac{C_2 V_{\mathrm{REF}} + I \cdot \Delta T_1}{C_1 + C_2} \tag{1}$$

where $\Delta T1$ is the duration of $\phi 1$. C_2 is then discharged into the integrating capacitor C_3 during $\phi 2$ at the same time C_1 is discharged to ground. If the voltage across $C_2(V(C_2))$ is larger than V_{REF}, the output of the operational amplifier will decrease when C_2 is discharged into the virtual ground. This will cause a decrease in current for the next cycle. Similarly, if $V(C_2)$ is less than V_{REF}, the current will be increased for the next cycle. Thus, if the loop is stable, the steady-state value of $V(C_2)$ is equal to V_{REF}, and the steady-state current will be

$$I = V_{\mathrm{REF}} C_1 / \Delta T_1 = 2 V_{\mathrm{REF}} C_1 F_{\mathrm{CLK}} \tag{2}$$

where we have assumed a 50% duty cycle for simplicity (i.e., $2\Delta T_1 = 1/F_{\mathrm{CLK}}$).

The functionality of Fig. 3 is captured compactly in Fig. 4. Transistors M2 and M5–M8 act as an integrating operational amplifier that drives the gate of M4. The rest of the elements are numbered the same as Fig. 3. The circuit generates its own reference because M5 and M6 are biased so that they will have the same current, but M5 is N times as wide asM6; therefore, the voltage difference across their gates will be (assuming strong inversion operation)

$$V_{\mathrm{REF}} = V_{\mathrm{GS5}} - V_{\mathrm{GS6}} = \sqrt{\frac{2IL}{\mu C_{\mathrm{OX}} W}} \left(1 - \frac{1}{\sqrt{N}}\right). \tag{3}$$

This is the same voltage produced by the circuits in Figs. 1 and 2. A MOS differential pair transistor of dimensions $W_{\mathrm{DIFF}}/\mathrm{L}_{\mathrm{DIFF}}$ biased with a current equal to the current in M6 will have a transconductance

$$G_M = 4 F_{\mathrm{CLK}} C_1 \sqrt{\frac{L}{W} \frac{W_{\mathrm{DIFF}}}{L_{\mathrm{DIFF}}}} \left(1 - \frac{1}{\sqrt{N}}\right) \tag{4}$$

where W and L are the dimensions of M6.

Finally, the bandwidth of an amplifier built with this differential pair and compensated with a capacitance C_C will be

$$\frac{G_M}{C_C} = 4 F_{\mathrm{CLK}} \frac{C_1}{C_C} \sqrt{\frac{L}{W} \frac{W_{\mathrm{DIFF}}}{L_{\mathrm{DIFF}}}} \left(1 - \frac{1}{\sqrt{N}}\right) \tag{5}$$

which is independent of process and temperature.

A similar derivation assuming weak inversion for M5 and M6 as well as the operational amplifier differential pair results in

$$\frac{G_M}{C_C} = 2 F_{\mathrm{CLK}} \frac{C_1}{C_C} \ln(N) \tag{6}$$

which is also independent of process and temperature.

For best performance, the input differential pair of the operational amplifier should not only be the same type as M5 and M6, but it should operate at a current density equal to the geometric mean of the current densities of M5 and M6. If this is done, then a constant G_m–C characteristic will occur regardless of the bias region (sub-threshold, strong inversion, etc) of the differential pair. As a practical matter, good results are obtained even if the bias points are not identical.

Of course there are countless ways of using feedback and transistors biased at different current densities to produce this same type of result. One advantage of the topology in Fig. 4 is that the differential pair can be biased to mimic the differential pair of the operational amplifier which it is to bias. In addition, small switches can be used because most of the supply voltage can be used to drive them since one side of the switch is always at (or close to) the negative supply rail. This circuit can be used to generate small currents, so it is an alternative to [10].

III. Stability

The difference equation for the drain current of M4 (Fig. 3) is

$$I(n+1) = I(n) + G_{\mathrm{M(M4)}} \left(V_G(n+1) - V_G(n)\right) \tag{7}$$

where $V_G(n+1) - V_G(n)$ is the difference in the gate voltage of M4 from period nT to $(n+1)T$. Its value is

$$V_G(n+1) - V_G(n) = -\frac{C_2}{C_3} \left(\frac{I(n)\Delta T_1 - C_1 V_{\mathrm{REF}}}{C_1 + C_2}\right). \tag{8}$$

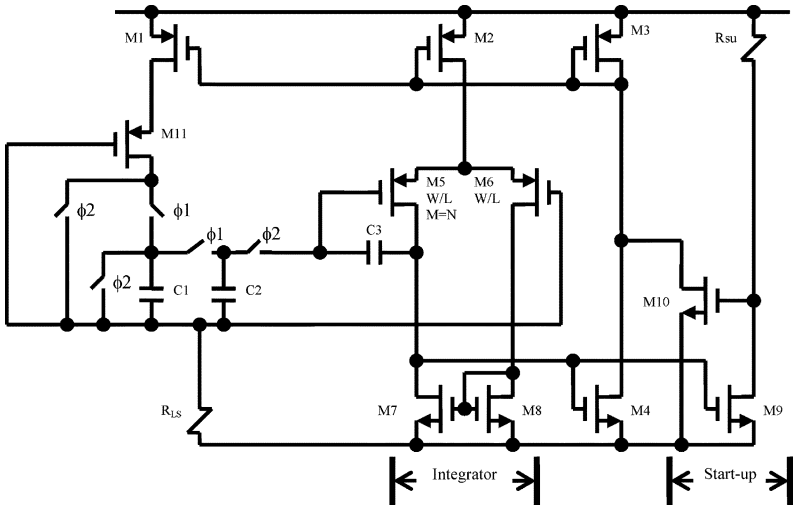

Fig. 5. Constant G_m–C switched-capacitor bias used for simulations.

Assuming a 50% duty cycle for $F_{\rm CLK}$, a z-domain analysis of (7) and (8) shows the current to be

$$I(z) = \frac{\frac{G_{M(\rm M4)}C_2C_1}{C_3(C_2+C_1)}V_{\rm REF}}{1+z^{-1}\left(\frac{1}{2C_1F_{\rm CLK}}\frac{G_{M(\rm M4)}C_2C_1}{C_3(C_2+C_1)}-1\right)}. \quad (9)$$

This will be stable (i.e., the poles will be inside unit circle) if

$$\frac{G_{M(\rm M4)}}{4F_{\rm CLK}}\frac{C_2}{C_3(C_2+C_1)} < 1. \quad (10)$$

For a given current the only variables that change stability are $G_{M(\rm M4)}$, C_2 and C_3. The size of the integrating capacitor (C_3) can be reduced by making C_2 or $G_{M(\rm M4)}$ small. $G_{M(\rm M4)}$ can be reduced with resistive degeneration, or by using a current source in parallel with M4 that supplies close to the correct current so that M4 only has to supply a small error correction current.

The integrating amplifier (M5–M8) is stabilized with a capacitor from the drain of M7 to ground. The gate–source capacitance of M4 is usually sufficient.

IV. Complete Circuit

The complete circuit shown in Fig. 5 was simulated in a 0.18-μm process. The bias operates the same as the one in Fig. 4 except that transistor M11 is added to improve power supply rejection by replicating the drain–source voltage of M2 to M1. In addition, an optional level shifting resistor $R_{\rm LS}$ is included that may be necessary to ensure M5 and M6 are biased in the saturation region if the $V_{\rm GS}$ of M8 is larger than the V_T of M6. (Similarly, the $V_{\rm GS}$ of M4 must be less than the V_T of M5 if $R_{\rm LS}$ is not used.) The complexity is similar to [11].

Start-up is ensured with devices $R_{\rm SU}$, M9, and M10. Unlike most start-up circuits, it is not necessary that M10 shuts completely off—nonzero current in M10 will only create a small systematic error from M7 and M8 having different drain–source voltages. The output current is obtained by mirroring the current in M1.

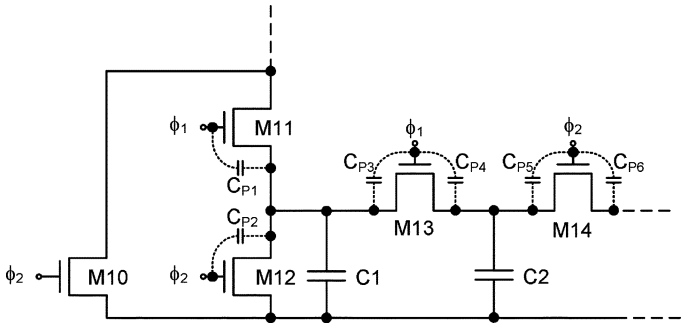

Fig. 6. Detail of the nMOS switches and relevant parasitic capacitances of the circuit in Fig. 5.

V. Power Supply Rejection

The circuit provides good power supply rejection because of the dc high gain of the integrating operational amplifier and the large output resistance of M4. In addition, the switch arrangement cancels much of the supply dependent charge injection. As can be seen by Fig. 6, the charge injected from $C_{\rm P2}$ onto C_1 can be cancelled by $C_{\rm P1}$ and $C_{\rm P3}$ if the width of M12 is equal to the sum of the widths of M11 and M13. Similarly, the charge put onto C_2 by $C_{\rm P4}$ is cancelled by $C_{\rm P5}$ if they are the same size. $C_{\rm P6}$ injects charge onto C_3 (Fig. 5), which produces a small ripple that can be reduced by adding a dummy switch if desired. Simulations show that a 10% change in supply results in less than a 0.3% change of the current in M1.

VI. Simulation Results

Simulations were run to compare the "constant G_m–C" bias (Fig. 5) against the "constant transconductance" bias assuming both used internal components. The corners tested were: Temp:-55/125C, resistors $+/-30\%$, and capacitors $+/-20\%$. To ensure a fair comparison, the constant transconductance bias was created by replacing the switched capacitor in Fig. 5 with a temperature-stable resistor that produced the same nominal current and a temperature stable transconductance.

The op-amp circuit in Fig. 7 was used to evaluate the performance over corners of each bias circuit. The op-amp used

TABLE I
DEVICE SIZES FOR CIRCUIT IN FIG. 5

Device	Size
M1	50 um /5um
M2	400 um /5 um
M3	100 um /5 um
M4	40 um /5 um
M5	5.5 um /0.18 um, M=8
M6	5.5 um /0.18 um
M7	80 um /5 um
M8	80 um /5 um
M11	2.8 um /0.18 um
C1	4.3pF
C2	0.1pF
C3	15pF
R_{LS}	0
F_{CLK}	10MHz

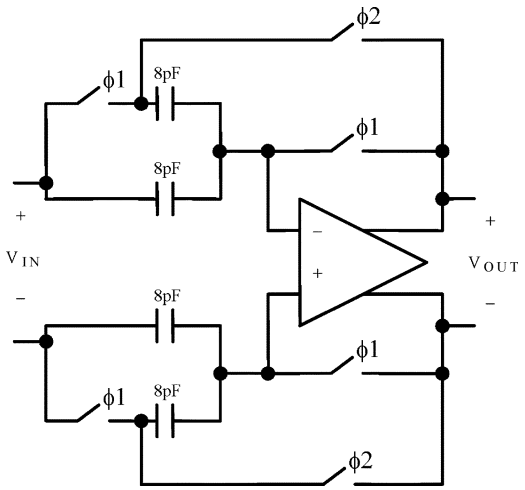

Fig. 7. Test circuit for the constant gm/C bias. The bias in Fig. 5 was used to power the op-amp in this test circuit.

a pMOS differential pair biased at a current density equal to the geometric mean of the current densities of M5 and M6. As explained earlier, this pMOS differential pair will have a transconductance proportional to $1/R$ when biased by the constant transconductance circuit. Because of this, one would expect inconsistent transient performance of the constant transconductance circuit over both resistance and capacitance corners.

On the other hand, the transconductance of the differential pair biased by the constant G_m–C bias will be proportional to $C_1 F_{\mathrm{CLK}}$, so one would expect almost complete rejection of the process variations.

The results are shown in Figs. 8 and 9. Clearly, the constant G_m–C bias gives more consistent performance over process corners since it automatically adjusts to compensate for those corners. The small variations in performance are probably caused by parasitic capacitances that do not scale with the bias capacitance. For example, the different pair input capacitance.

The transient response of the output current during start-up and the steady-state response is shown in Fig. 10. The start-up time is about 50 μs, and is determined mostly by the ratio of C_2 to C_3. The detail shows a ripple of about 5 nA (0.02%) and

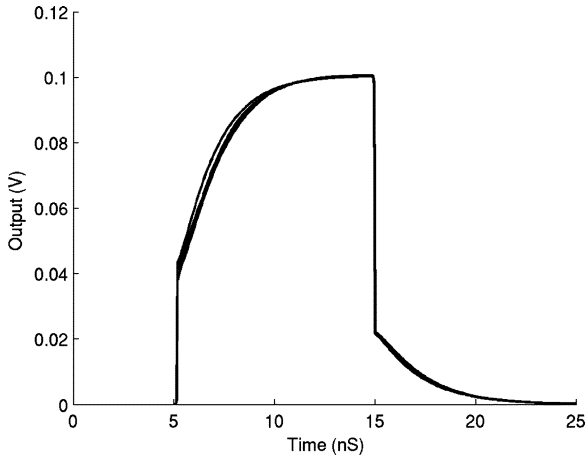

Fig. 8. Simulated response of test circuit over process and temperature corners when biased with "constant G_m–C" circuit.

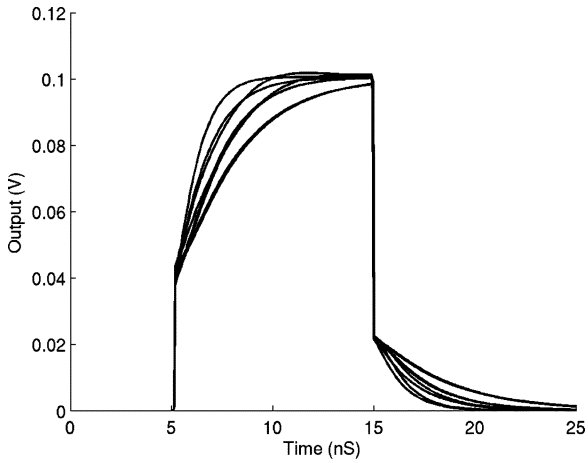

Fig. 9. Response of test circuit over process and temperature corners biased with "constant transconductance" circuit.

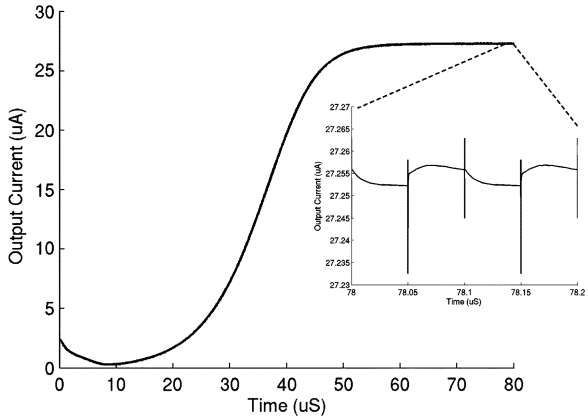

Fig. 10. Typical start-up waveform and steady-state detail of output current ($V_{\mathrm{DD}} = 0.9$ V).

short duration spikes caused by the charge injected into the integrating capacitor C_3. The ripple could be filtered if necessary. The initial nonzero current is the start-up current.

Simulations indicate the circuit performs with supplies as low at 0.9 V over the previously mentioned process and temperature corners.

VII. Conclusion

Unlike previously published circuits, the circuit in Fig. 5 uses a small number of components to generate a constant G_m–C current for an op-amp. The differential pair in Fig. 5 can be made to scale with the differential pair of the biased op-amp, allowing for good transconductance tracking over process and temperature corners. Small switches that minimize charge injection can be used because they are positioned so that nearly the full supply drives them. Simulations show transient performance over resistor, capacitor, and temperature corners is substantially better than the popular constant transconductance bias.

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