A High-Speed, High-Resolution Analog Front End for Digital Subscriber Line Applications

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Abstract

A 5V CMOS chip providing the D/A, A/D, filter, and a programmable gain amplifier (PGA) for HDSL and ADSL is described. The chip includes 12-bit, 10 Msample/sec converters, filters, and a PGA having 48 dB gain with 1.7 MHz bandwidth. This chip is used in an El-rate (2.048 Mbps) ADSL transceiver achieving a bit error rate of less than 10^-7 over 5.4 km of 0.4 mm twisted copper wire.

1. System Background

This D/A, A/D, filter and PGA chip is designed for applications involving digital subscriber lines, such as HDSL and ADSL. With a DSL system, the channel consists of a twisted pair of copper wires, as is common today in the telephone infrastructure. While traditional analog voice communications is maintained, the wire pair is also used to transport high speed data. One such application, asymmetric digital subscriber line (ADSL), is shown in Fig. 1.

The system functions by using a modulation scheme known as carrierless AM/PM (CAP) [1]. This modulation scheme maps the incoming sequence of digital bits into a combination of in-phase and quadrature digital levels. These levels are fed into a digital FIR filter, having an impulse response that determines the spectrum of the resulting output. These symbols are converted to an analog waveform, which is transmitted across the telephone line where it experiences attenuation and dispersion. At the receiver, an adaptive equalizer compensates for the line loss, and a decision circuit determines the received symbol based on a maximum likelihood decision.

2. Transceiver Architecture

The transceiver has been partitioned into a multichip solution as shown in Fig. 2, with the integration of the digital signal processing functions described in [2]. The analog portion of the transceiver consists of two chips, the one described here, and a line driver/receiver amplifier.

This chip consists of a 12-bit, 10 Msample/sec D/A and an active RC filter in the transmit path. Similarly the receiver consists of a PGA, an active RC filter and a 12-bit, 10 Msample/sec A/D. The A/D has been described in [3].

Figure 1. ADSL Application

Figure 2. ADSL Transceiver Architecture
Each of these blocks will be described in more detail in the following sections.

3. Self-Calibrating High Speed D/A

For conversion rates at 10 Msamples/sec, most D/A designs depend on transistor matching techniques to achieve the desired resolution. This approach has proven successful to about 8-9 bits of resolution. In high speed applications requiring more than 8-9 bit performance, transistor matching will not achieve the desired resolution, and other techniques must be used. The methods in which this precision can be enhanced are either trimming at wafer level, or dynamic calibration [4]. In this design the latter technique is used. Here the performance of the self-calibrated DAC is further enhanced over previously reported work by introducing a novel biasing technique that is instrumental in achieving high speed calibration.

3.1 D/A Architecture

A basic block diagram of a 12 bit self-calibrating DAC is shown in Fig. 3. It consists of most significant bit (MSB) and least significant bit (LSB) arrays, a thermometer encoder, biasing circuit, timing circuit, and control blocks. The MSB array consists of 63 current sources, each supplying a current, I₀. The output current of this array is determined by taking the 6 MSB’s, thermometer encoding the inputs into 63 signals. These signals then control the direction of current flow of each cell in the array. Meanwhile, the 6 LSB’s control the LSB array, which consists of six binary weighted current sources.

3.2 MSB Calibration

The bias circuit, the circuit used to calibrate the MSB array cells, and a single MSB cell are shown in Fig. 4. Here only one MSB cell is shown, although there are a total of 63 cells that are switched either to a positive or a negative output, summed at resistors connected to the positive supply. There is also a 64th MSB cell, which is used as a spare cell, replacing the cell under calibration.

An MSB cell is comprised of a current source supplying 0.95I₀ of a total output current I₀, calibration transistor, M₁, data selector switches S₁ and S₂, and calibrating switches S₃ and S₄.

In the calibration mode, switches S₁ and S₂ are open, and switches S₃ and S₄ are closed. This forces a current I₀ through S₃ into M₁ and the current source of the MSB cell. Since the current source provides a current 0.95I₀, the gate of M₁ will be forced to a voltage so that M₁ provides the remaining 0.05I₀. With the same calibration circuit used to calibrate every MSB cell, the mismatches in M₁ and the current source will be corrected. Following calibration, switches S₃ and S₄ are opened, either S₁ or S₂ is closed, and I₀ will flow from the positive or negative output.

An important part of proper conversion is the maintenance of the voltage at node 3 at the same value for calibration and operation. This reduces error in the cell current due to variation in the V_DS of M₁ and the current source, 0.95I₀, and it allows a short calibration time. Since the bias and calibration circuitry is designed to have W/L_M₁ = 10W/L_M₁, node I_cal is fixed at V_ref during calibration.

![Figure 3. D/A Block Diagram](image1)

![Figure 4. D/A MSB Calibration](image2)
The voltage at node 3 during calibration is then

\[ V(3) = V_{ref} - R_{on}I_0 \]

where \( R_{on} \) is the on-resistance of switch \( S_3 \).

In normal operation, the voltage at node 3 is determined by either the voltage at node 4 or node 5 and the resistance of switch \( S_1 \) or \( S_2 \). With the bias circuitry designed to have \( W/L_{M4} = W/L_{M5} = W/L_{M6} \), then node 4 or 5 will be held at \( V_{ref} \). The voltage at node 3 during operation is then

\[ V(3) = V_{ref} - R_{on}I_0 \]

the same as the node voltage during calibration.

3.3 LSB Calibration

A simplified schematic of the LSB array is shown in Fig. 5. The LSB currents are derived from further dividing one MSB current source into binary weighted inner current sources. Here the 0.95I_0 current source and \( M_1 \) are identical to those in an MSB cell.

In MSB calibration, there is a spare cell that replaces the cell being calibrated, and using the same approach for the LSB portion of the D/A would imply a duplicate LSB array. Instead the LSB array calibration is completed without replacing the complete array, but rather the current source and calibration transistor \( M_1 \) are duplicated. During one calibration clock period, the left-hand current source is calibrated, while the right-hand source provides current to the array. During the next calibration clock period, the cells are exchanged and the process repeated.

As in the MSB array, the biasing is designed to maintain a constant voltage across the current sources during calibration and normal operation to improve speed and accuracy. This is achieved by scaling the transistors connected to \( V_{bias} \). Again, this maintenance of a constant voltage increases the speed of calibration.

4. Transmit (Reconstruct) Filter

Following the D/A converter in the transmit path is a lowpass filter designed to remove the images of the transmitted spectrum that occur at multiples of the sampling frequency. By operating the D/A at four times the sampling rate, the filter is simplified, reducing noise and improving linearity. The resulting transmit filter is fourth order, implemented as cascade of two second order Rauch filters followed by a buffer to drive the external load. This filter is trimmed at wafer testing to reduce variations due to resistor and capacitor processing, and the 3 dB frequency is programmable to support the T1/E1 HDSL and ADSL applications.

5. Receive (Anti-aliasing) Filter

Like the reconstruct filter, the anti-alias filter is a lowpass. Here the filter removes high frequency noise that would otherwise be aliased into the signal band by the sampling of the A/D. Again, the order of this filter depends on the frequency of the signal passband and the sampling frequency. Here, a digital decimator and oversampling of the A/D by a factor of four was used to simplify the anti-alias filter. This also improves the signal to noise performance of the converter. The 3 dB frequency of the resulting fourth order filter is programmable to support the T1/E1 HDSL and ADSL applications. The implementation is similar to the reconstruct filter.

6. Programmable Gain Amplifier (PGA)

For HDSL, the received signal occupies the same frequency band as the transmitted signal, while for ADSL it occupies a different band. These two differing systems create two different requirements for receiver gain. For E1-rate (2 Mbps) ADSL, the signal may pass through a channel consisting of as much as 4.25 km of 0.4 mm copper wire for a 2 Mbps (E1-rate) system. This corresponds to a 60 dB mid band loss, with more than 85 dB loss at the high end of the band. To compensate for such a channel and band loss, the PGA design combines high gain and wide bandwidth, while maintaining a high input impedance and an input noise.
voltage of less than $10 \, nV/\sqrt{Hz}$. The gain of the PGA is partitioned to the three stages, one having 30 dB gain with 6 dB steps, one with 15 dB gain with 3 dB steps, and one with 3 dB with 0.3 dB steps.

7. Measured Results

This chip has been incorporated in a 2.048 Mbps/24 kbps ADSL designed for E1 systems. While the system objective for E1-rate ADSL transmission is 60 dB of loop loss at 300 kHz, this CAP modulation approach allows even longer reach. Fig. 6 shows the receiver constellation for a 64-CAP signal on a 5.4 km loop of 0.4 mm cable having 78 dB loss. This results in a bit error rate of less than $10^{-7}$.

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<tr>
<td>Gain range</td>
</tr>
<tr>
<td>THD</td>
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<tr>
<td>Bandwidth</td>
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<td>Filters</td>
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References


![Figure 6. Received CAP-64 Constellation](image1.png)

![Figure 7. Chip Photomicrograph](image2.png)

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