A Noise-Shaped Switched-Capacitor DC-DC Voltage Regulator

A. Rao, W.McIntyre [1], U. Moon, and G. Temes
Oregon State University, Corvallis, Oregon
National Semiconductor Corporation, Grass Valley, California [1]
rao@ece.orst.edu

Abstract

This paper presents a delta-sigma control loop for a buck-boost dc-dc converter with fractional gains. The charge pump used to convert the input voltage acts as a D/A converter in the loop, and its output ripple is frequency shaped by the loop, which also provides the pulse- frequency modulation needed for the conversion. A test chip realised in a 0.72-µm CMOS process and clocked at 1MHz provided suppression of tones up to 50dB in the 0-500kHz range. The target output voltage may be from 1.8V to 4V for loads up to 150mA. The input voltage range is 3V to 5V.

1. Introduction

For many years the inductive conversion topology has been the standard solution to providing a constant and stable voltage from a battery. With the continued shrinking of the hand-held devices as cell phones, PDA's, pagers and laptops, the use of traditional inductive based regulators is becoming less attractive. The compact switched-capacitor regulator is preferable to the bulky inductive-based regulator. While the inductive DC/DC converter uses a magnetic coil, the switched-capacitor system uses an array of switches and capacitors.

Some of the primary reasons to choose capacitive DC/DC conversion over inductive are reduced electro-magnetic induction (EMI) and high-frequency noise. Switched capacitors do not produce substantial EMI noise. Switched-capacitor regulators also tend to be more efficient for lower input voltages. Thus switched-capacitor power conversion offers reduced physical volume, less radiated EMI, efficiency and cost advantages over inductive based structures.

A conventional method to regulate voltage in a switched-capacitor converter is to use pulse-frequency modulation (PFM) or burst-mode operation. These control techniques suffer from tones in the frequency spectrum. The tones are difficult to filter, as their frequencies are hard to determine. As a result, the circuits that use the regulated voltage are susceptible to noise in the frequency region of operation. Furthermore, these tones can mix with unwanted signals outside the band of interest and modulate into the desired signal band.

An alternate control technique using a delta-sigma loop is presented which spreads the tones in the conventional switched-capacitor regulator. For implementation, we have applied the new control loop architecture to an existing buck-boost fractional-gain regulator designed at National Semiconductor Corp. [1] and shown in Fig.1.

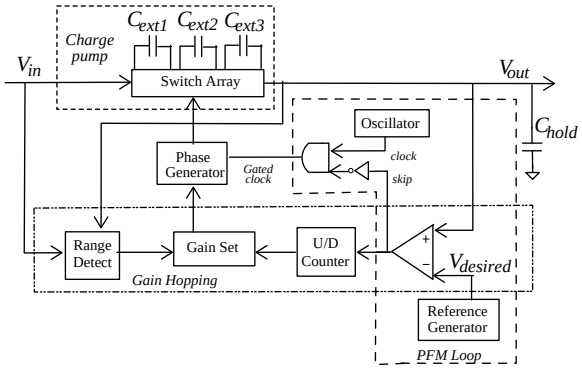

Figure 1: Burst mode switched-capacitor DC/DC regulator (LM3352)

2. Fractional gain charge pump architecture

Fractional gains can be realised by connecting external capacitors to an on-chip switch array, as shown in Fig. 2 [2]. The switch array can provide 7 different gains (G): 1/2, 2/3, 3/4, 1, 4/3, 3/2, and 2. Each gain is implemented in two phases of a 1MHz clock. For example, Fig. 3 shows the configuration used to implement G=2.

To guarantee that current does not flow into the battery (which may result in damage to it) we have to ensure that $G>V_{REG}/V_{IN}$, where V_{REG} = desired output voltage and V_{IN} = unregulated battery voltage. Also, to maximize efficiency, G must be as close to V_{REG}/V_{IN} as possible. The gain that satisfies these conditions is defined to be the minimum gain, G_{MIN}.

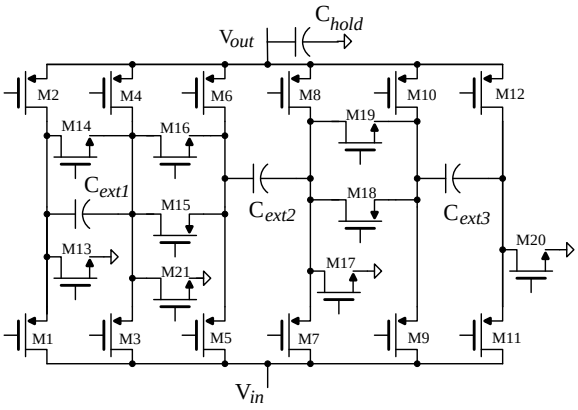

Figure 2: Switch array with external capacitors

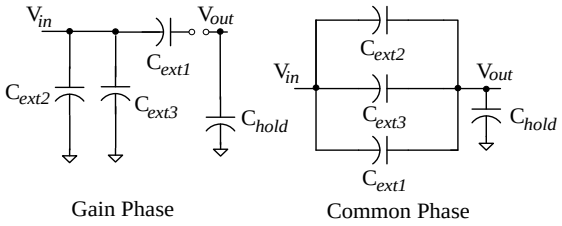

Figure 3: Capacitor configuration for G = 2

When the pump provides the gain G_{MIN}, the largest current that it can deliver to the load is approximately

$$I_{MAX} \cong (G_{MIN} * V_{IN} - V_{REG}) / R_{OUT},$$

where R_{out} is the equivalent output impedance of the switch array. Each gain configuration has a unique R_{out}, which is a function of switching frequency, capacitor size and the switch impedance. Selecting a gain larger than G_{MIN} increases I_{MAX}. By increasing the gain only when needed, power is delivered more efficiently. The *gain-hopping* loop controls the gain based on a measure of the load current and sets the value of G_{MIN} as a function of V_{IN}. Figure 4 illustrates the minimum gain versus V_{IN} for V_{REG} = 3.3V.

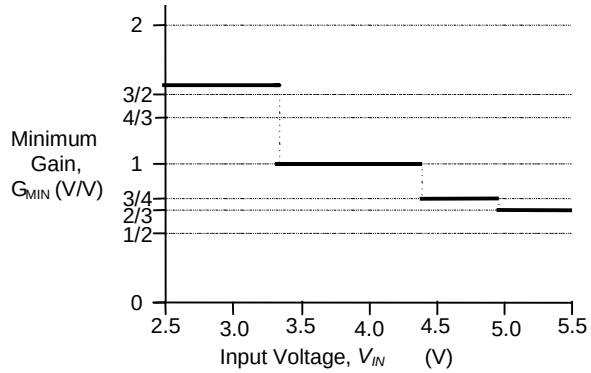

Figure 4: G_{MIN} vs. V_{IN} (for V_{REG}=3.3V)

The *gain-hopping* loop contains an up-down counter, gain set block and comparator. The up-down counter integrates the pulse density of the comparator output and directs the gain-set block to increase or decrease the gain.

The PFM loop in Figure 1 consists of a voltage reference, an analog comparator and an oscillator. The comparator output is sampled at 1MHz. When V_{REG} is below the reference, the switch array delivers current to the load. Alternately, when V_{REG} is above the reference, the switch array rests. By controlling the switching, the output impedance is PFM modulated to provide the regulation. Also, for a given gain configuration, the pulse density of the comparator is proportional to I_{LOAD}. If I_{LOAD} is constant, the duty cycle of the output is fixed resulting in a highly tonal frequency spectrum.

3. Delta-sigma (ΔΣ) control loop

The modified regulator with a first-order delta-sigma control loop (shaded) is shown in Fig. 5. The ΔΣ loop provides the necessary gain selection and the signal to switch the charge pump on and off. A simplified model of the ΔΣ loop is shown in Fig. 6. The ΔΣ loop contains an integrator and a 4-bit A/D converter. The LM3352 is used as the D/A in the loop.

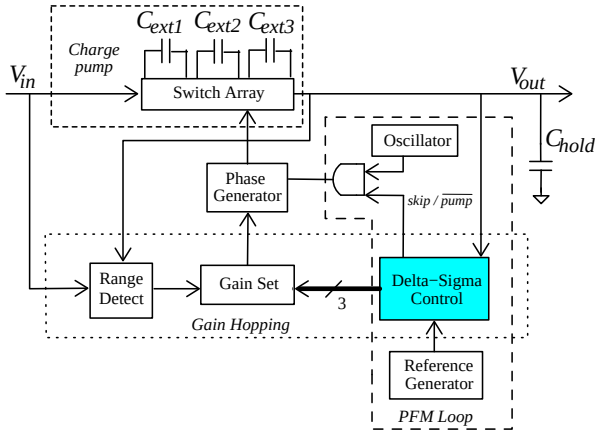

Figure 5: Regulator with ΔΣ loop

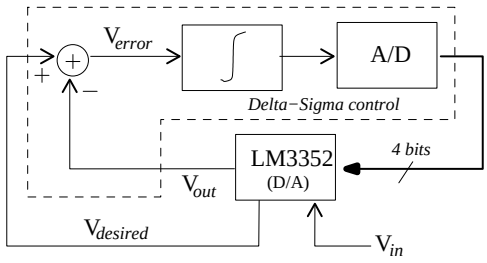

Figure 6: Block diagram of the ΔΣ loop

The 3 MSB's from the A/D select one of the seven gain levels, and the LSB controls the pump or skip cycle of the charge pump. It decides whether the charge pump should be idle or deliver charge.

The error between the desired voltage and the output voltage is integrated, and is fed to the 4-bit A/D. As the output voltage approaches the desired voltage, the error signal decreases, reducing the input to the A/D. This causes a smaller gain to be chosen, until we are forced to use the minimum gain. Since the ΔΣ control is a first -order loop, we need to add some dither before the A/D to avoid tone generation.

The charge pump can be modeled as a lossy integrator [3]. It creates a pole after the quantizer, as shown in Fig. 7, and can cause the loop to be unstable. In order to stabilize the loop, we added a feed-forward path around the integrator with a gain greater than 1. Simulations showed that the optimum value of the feed-forward path is 4.

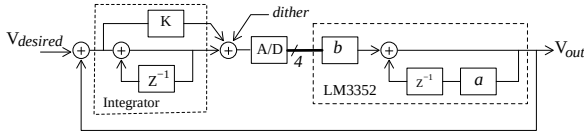

Figure 7: ΔΣ system architecture

The ΔΣ loop makes the gain selection more random and thus spreads the tones. The loop also enables the use of the minimum gain more often and thus makes the system more efficient. It should be mentioned that the delay through the loop is critical, and it will affect the load and line response of the regulator.

4. Circuit design

Since the ΔΣ loop controls only the gain selection and is not part of the signal path, it was kept very simple and small. All circuitry was single ended since the LSB was large (150mV). The integrator and the gain block are standard switched-capacitor stages. The unit capacitance used was 250fF. A simple two-stage Miller-compensated operational amplifier, with an open-loop gain of 65dB, unity-gain frequency of 17MHz and phase margin of 55 degrees, was used. The A/D implemented is a classical 4-bit flash structure [4], as shown in Fig. 8.

A clocked CMOS comparator was used, and is shown in Fig. 9. The inverters have current sources to limit the current flow and hence the power dissipation. A resistor ladder sets the reference voltage levels. The total resistance of the ladder is 220kΩ. The dither circuit is a standard pseudo-random number generator using flip-flops and XOR gates.

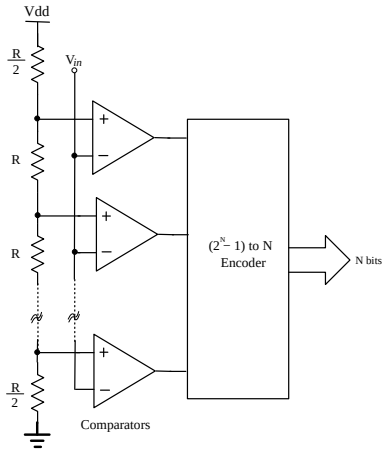

Figure 8: 4-bit flash A/D

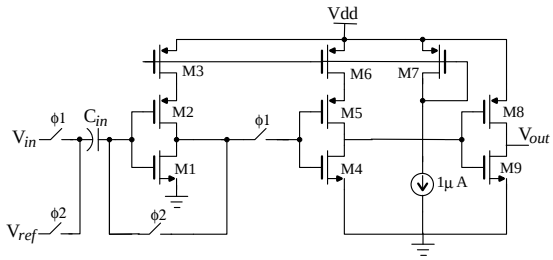

Figure 9: Clocked CMOS comparator

The existing LM3352 chip was combined with the ΔΣ loop in the implementation. The voltage reference block is shown in Fig.10. It consists of a bandgap, a reference buffer, a D/A converter and an E^2PROM block. This generates the $V_{DESIRED}$ ranging from 3V to 5V. The E^2PROM allows post-package trimming of the bandgap voltage and V_{REG} adjustment through the D/A converter.

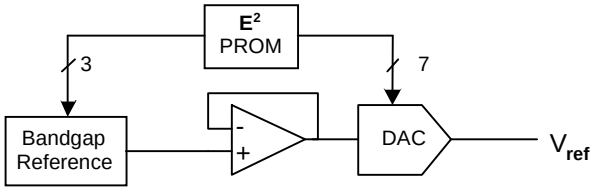

Figure 10: Reference block

5. Experimental results

The fabricated chip was tested through the input range of 3V to 5V for several loads and output voltages. A typical measured output ripple and spectrum for a load of 150mA, output voltage of 4.7V and input voltage of 3.4 V is shown in Figs. 11 and 12.

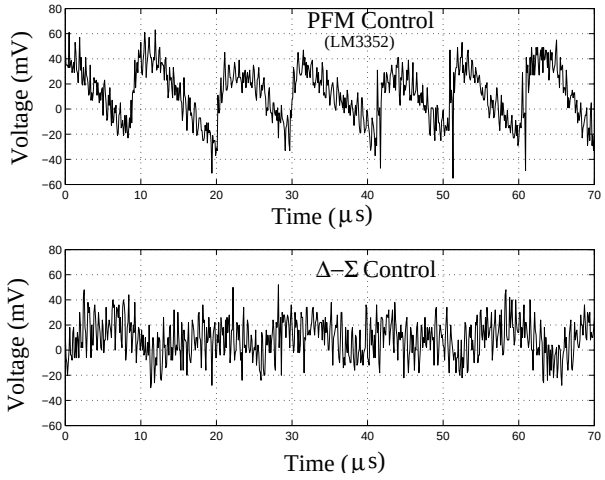

Figure 11: Measured output ripple of regulator with PFM and delta-sigma control

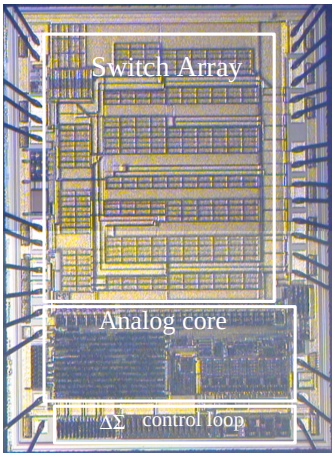

Figure 13: The die photograph of regulator with ΔΣ control

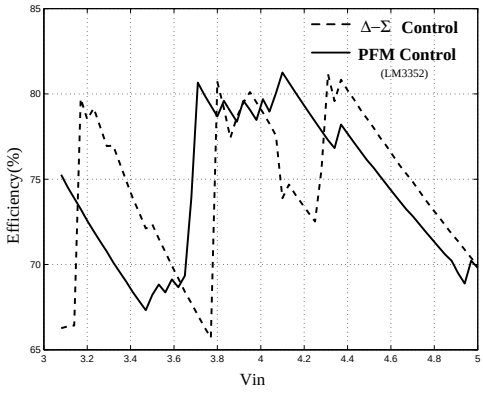

Figure 14: Measured efficiency plot of regulator with and without ΔΣ control loop

The ripple of the PFM controlled regulator is periodic, while the delta-sigma control has a random ripple and hence a smoother spectrum. Figure 13 shows the die photograph. The efficiency of the two architectures is plotted in Fig. 14. They are comparably efficient.

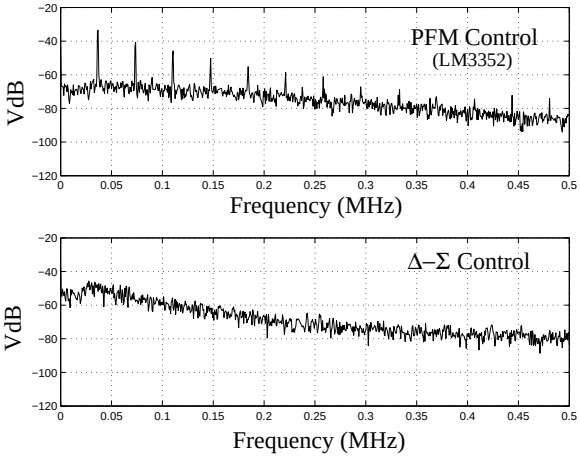

Figure 12: Measured frequency spectrum of regulator with PFM and delta-sigma control

The spectral characteristics of the regulator with delta-sigma control are clearly superior. The regulation, however, is not as good as that of the pulse-frequency modulation. PFM gives a regulation of around 2% over line and load changes while the delta-sigma control has a regulation of around 4% over the same range. This can possibly be attributed to the increased ripple due to the increased delay through the loop.

6. Conclusions

A pulse-frequency-modulation voltage regulator with a ΔΣ control system was designed and fabricated. The test results indicate that the suppression of tones is possible using this technique. The additional delay through the loop increases the ripple slightly and causes slightly poorer regulation.

7. Acknowledgement

This research was funded by National Semiconductor Corporation. The authors thank T. Glad, P. Wong , J. Parry and M. Farley for their valuable help.

8. References

[1] National Semiconductor Data Sheet, LM3352

[2] US Patent *6,055,168*, Apr. 25, 2000, Kotowski et al.

[3] A. Rao, W. McIntyre, J. Parry, U. Moon and G. Temes, "Buck-boost switched-capacitor DC-DC voltage regulator using delta-sigma control loop," *IEEE International Symposium of Circuits and Systems*, May 2002

[4] A. G. F. Dingwall, "Monolithic Expandable 6-bit 20-MHz CMOS/SOS A/D Converter," *IEEE J. of Solid-State Circuits*, Vol. 14, pp. 926-931, December 1979.