A 1.8 V CMOS DAC CELL WITH ULTRA HIGH GAIN OP-AMP IN 0.0143 mm^2

Brandon R. Greenley[⋆†], *Un-Ku Moon*[⋆], *and Raymond Veith*[†]

[⋆] Electrical and Computer Engineering, Oregon State University
[†] Tektronix, Inc., Beaverton, OR

ABSTRACT

This paper presents a novel 1.8 V digital-to-analog converter (DAC) which is designed to operate at DC for a wide variety of circuit calibration techniques. To achieve 10-bit performance at 1.8 V, an ultra high gain op-amp is introduced for servoing. In order to minimize area consumption while maximizing performance, a segmented plus binary plus R-2R architecture is used. The DAC was designed in a standard digital 0.18 μm CMOS process. The DAC occupies 0.0143 mm^2 (110 μm $\times$ 130 μm), and consumes 2.8 mW of power. The 5 stage cascaded op-amp with feed-forward compensation achieves 130 dB of gain with 81° phase margin while consuming only 60 μW.

1. INTRODUCTION

In the design of mixed-signal ASICs, it is often very convenient to have small calibration circuits that can be used repeatedly throughout the chip. These calibration circuits should be as small as possible so that the surrounding circuitry remains virtually unchanged in the layout. This paper deals with one such calibration circuit in the form of a 10-bit DAC. This style of DAC is used widely in the design of mixed-signal ASICs to provide reference voltages and bias currents. The advantage of having a small DAC cell is that the reference voltages and currents can be varied easily by a micro-controller during calibration.

Designing circuits with low voltage supplies is becoming necessary as we move into the age of portable electronic devices. This DAC will be fabricated in a 0.18 μm CMOS process with a single 1.8 volt supply. The low voltage introduces some limitations, the most obvious being the lack of head room present for providing output currents from the DAC. To overcome this limitation, this paper presents a mirroring technique for providing linear output voltages and currents.

Providing linear current and voltage outputs with the use of strictly CMOS devices presents the need for a high gain servoing op-amp. With layout area being of prime concern and only a single 1.8 volt supply, a 5 stage cascaded op-amp is used. This paper presents the detailed analysis of a five stage conditionally stable op-amp which produces 130 dB of gain and 81° phase margin. A positive feed-forward stage was implemented to achieve stability at unity gain crossover. The op-amp consumes 60 μW and occupies only 30 μm $\times$ 26 μm.

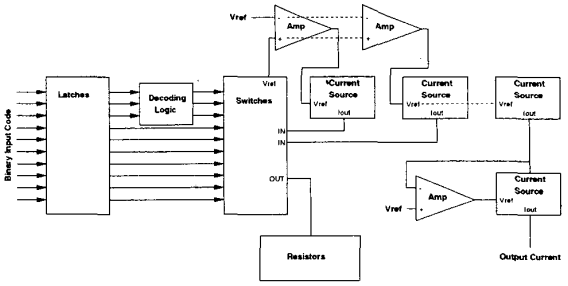

Figure 1: System Block Diagram.

Figure 1 shows a block diagram of the system. The latches are simple back to back inverters with a pass gate. The decoding logic is needed for the 3 upper bits that are segmented. The switches, resistors, cascodes and op-amps can be seen in detail in figures 2 & 4.

2. SEGMENTED PLUS BINARY PLUS R-2R DAC DESIGN

It is well known that segmenting current sources in a DAC design provides better linearity for given element mismatches than binary weighting or an R-2R approach. It is also well known that segmenting an entire 10-bit DAC would consume a large amount of area [1–3].

This DAC utilizes the performance advantages of segmentation on the upper 3 bits, while capatalizing on the area savings of the R-2R ladder for the lower 6 bits (Fig. 2). In between the segmented portion (M7-M13) and R-2R portion (M0-M5), there exists a binary weighted branch, M6. A typical segmented plus R-2R architecture would include

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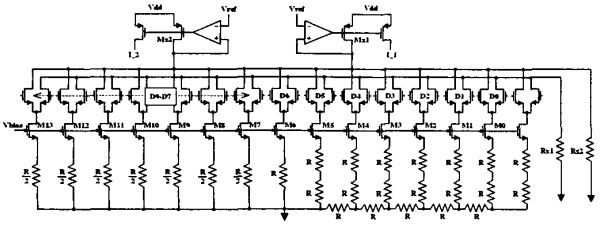

Figure 2: DAC Schematic Showing the Segmented, Binary, and R-2R Combination.

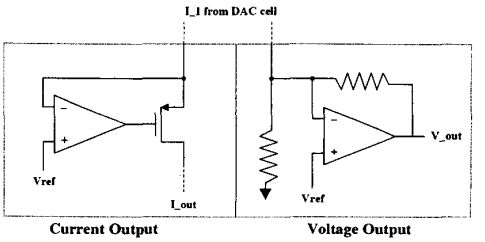

Figure 3: Linear Output Blocks: Voltage and Current.

the branch of M6 in the R-2R ladder, hence placing 2 resistors in the M6 branch and adding a resistor between the M5 and M6 branches. Such a typical approach would only require one resistor per branch for the segmented portion.

Figure 2 shows that the segmented branches (M7-M13) have 2 resistors in parallel for each branch (R/2). With two resistors per branch, the matching of the resistors in the segmented portion can be improved because the effect of a linear process gradient can be eliminated by proper layout. Hence the reason that the middle branch (M6) is binary weighted rather than included in the R-2R portion.

If the entire 10 bits of the DAC were structured in a R-2R scheme, the upper 4 bits (D6-D9) would contain 12 resistors, 8 switches and zero logic gates. In the implemented architecture, the upper 4 bits contain 15 resistors, 16 switches and 8 logic gates. A trade-off analysis was performed for the two different architectures in order to choose a design that maximizes performance without compromising much layout area.

Table 1 shows a summary of the number of resistors, switches, and 2-input logic gates needed to implement the upper 3, 4 or 5 bits. The binary bit that exists between the segmented and R-2R portions of the implemented architecture is included in the 3, 4 or 5 bits examined in the table. Table 1 shows that the device increase from the R-2R ladder to the implemented architecture is acceptable for 3 and 4 bits, but the increase in number of resistors, switches, and gates is not acceptable for 5 bits.

The outputs from the DAC are shown in figure 2 as I_1 and I_2. Figure 3 shows the circuit blocks used to obtain either output voltage or output current. Although output current could be taken directly from I_1 and I_2, the ouput node needs to be held at $Vref$ in order to mirror the DAC current linearly. The DAC is designed so that $Vref$ can vary from 0.6V up to 1.4V without sacrificing performance. The servoing op-amps which allow for the variation of $Vref$ will be discussed in section 3.

Op-amp offset does not effect the linearity of the DAC. The 2 servoing op-amps in the DAC core can have any amount of mismatch in their offsets because the DAC outputs are differential. Thus, the DAC operates like two independent, single ended DACs. Resistors Rx1 and Rx2 are used to maintain a constant bias current through Mx1 and Mx2 regardless of input code (Fig. 2). These resistors alleviate the need for a large gate voltage swing of Mx1 and Mx2. Limiting the amount of swing needed at the gates of Mx1 and Mx2 assures that the op-amps always operate in their linear region.

A full MATLAB model of the DAC was created to analyze the effects of device mismatches on the INL and DNL of the DAC. Using an element matrix that exactly replicates the layout of the DAC, we were able to see that the effects of linear process gradients are negligible. The model also shows that 10 bit performance will be achieved with the projected matching for the process, and that the effects of random mismatch in threshold voltages can be decreased with proper choice of resistor values.

3. ULTRA HIGH GAIN OP-AMP DESIGN & MODELING

Servoing applications often require an op-amp with exceptionally high DC gain. While high DC gain is often accomplished with the use of cascoding and gain boosted output stages, 1.8 volt operation limits the use of these techniques. The common approach to achieving high gain with a low supply voltage is to cascade several gain stages. The bottleneck associated with cascading multiple gain stages is com-

Upper Bits	Element	R-2R	Implemented	Δ
3	resistors	9	7	-2
	switches	6	8	2
	gates	0	3	3
4	resistors	12	15	3
	switches	8	16	8
	gates	0	8	8
5	resistors	15	31	16
	switches	10	32	22
	gates	0	23	23

Table 1: Trade-off Analysis: Number of Bits to Segment.

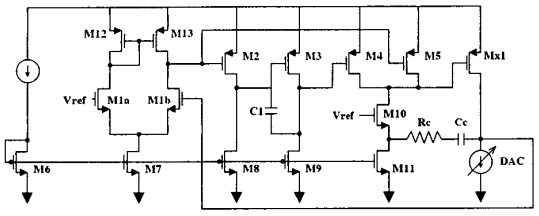

Figure 4: Feed-forward Amplifier Schematic.

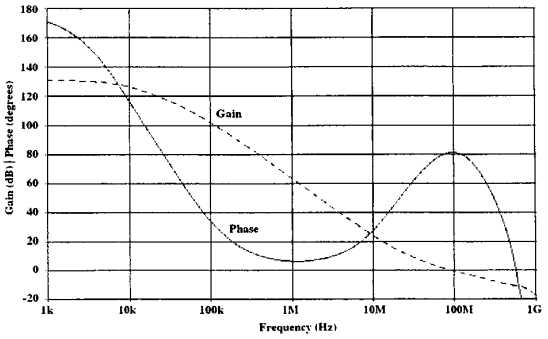

Figure 5: Simulated Amplifier Response.

pensating the op-amp to provide sufficient phase margin at unity gain. This op-amp, shown in figure 4 uses a positive feed-forward gain stage to achieve stability [4–6]. This feed-forward path acts as a path for high frequency signals, therefore bypassing the three stages comprised of M2, M3, and M4 which provide the high gain, low frequency path. A compensation capacitor (C1) is used between M2 and M3 to effectively slow the low frequency path even more, making the feed-forward path more dominant at high frequency. The final stage of the op-amp is actually the current source device of the DAC (Mx1). Since the drain of Mx1 is the node being servoed, Mx1 itself acts as an additional gain stage to the op-amp. These aggressive compensation techniques are used with a set of highly simplified gain stages because we are only interested in near DC operation of the DAC. Figure 5 shows the loop gain and loop phase properties of the op-amp with the output stage composed of Mx1 and the DAC as the current source.

A detailed analysis was performed on this op-amp to correctly model the pole/zero locations and to identify how process variations will effect the response. Figure 6 shows the small signal model used to derive the transfer function of the op-amp.

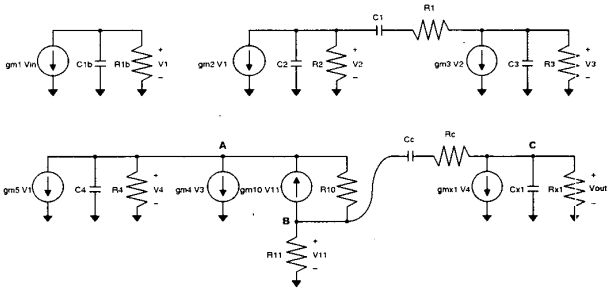

Figure 6: Small Signal Model Used to Create Mathematical Model.

The transfer function from Vin to $V1$ is

$$\frac{gm_1 R_1}{(1 + sR_{1b}C_{1b})}$$

The calculated transfer function from $V1$ to $V3$ is

$$\frac{gm_2 gm_3 R_2 R_3 (1 - \frac{sC_1}{gm_3} + sR_1 C_1)}{cs^3 + bs^2 + as + 1}$$

where

$$c = R_1 R_2 R_3 C_1 C_2 C_3$$
$$b = R_2 R_3 (C_1 C_2 + C_1 C_3 + C_2 C_3) + R_1 C_1 (R_2 C_2 + R_3 C_3)$$
$$a = R_2 (C_1 + C_2) + R_3 (C_1 + C_3) + gm_3 R_2 R_3 C_1 + R_1 C_1$$

Node equations can be written at **A**, **B**, and **C** as

$$\mathbf{A}: gm_5 V_1 + \frac{V_4}{Z_4} + gm_4 V_3 - gm_{10} V_{11} + \frac{V_4 - V_{11}}{R_{10}} = 0$$

$$\mathbf{B}: \frac{V_{11}}{R_{11}} + \frac{V_{11} - V_4}{R_{10}} + gm_{10} V_{11} + \frac{V_{11} - V_{out}}{Z_C} = 0$$

$$\mathbf{C}: \frac{V_{out}}{Z_{X1}} + gm_{X1} V_4 + \frac{V_{out} - V_{11}}{Z_C}$$

The final transfer function for the whole system, $H = \frac{Vout}{Vin}$, ends up with a 5^{th} order numerator and an 8^{th} order denominator. The coefficients of the transfer function are too numerous to list, but figure 7 shows the theoretical pole/zero locations and frequency response. The addition of the parallel feed-forward stage creates pole/zero doublets that can be seen in figure 7 [5]. The RHP zero that would normally be present because of the miller capacitor C1 is moved to the left half plane due to a larger LHP zero created by the feed-forward stage. The presence of the pole/zero doublets degrades the settling time [5], but the op-amp still settles to within 0.01 % in 25 ns, making it more than adequate for the DC application.

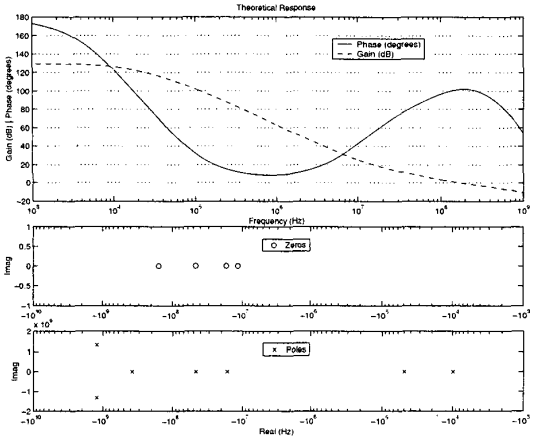

Figure 7: Theoretical Amplifier Results.

4. IMPLEMENTATION

To verify the operation of this DAC cell, the chip will be manufactured in a 0.18 μm standard digital CMOS process. The area consumed by this DAC cell is only 0.0143 mm^2 (110 μm $\times$ 130 μm). Figure 8 shows the layout of the DAC cell with the current source array in the center and the resistor array directly below. The resistor array could be expanded to reduce power consumption and improve matching, but it is kept at the same pitch as the current source array to minimize area. If there was a strong desire to use less that 2.8 mW, the resistor array could easily be expanded and the current through the resistors dramatically decreased.

Actual INL and DNL values will not be known until the chip is measured. The matching of each branch current will be strongly dependent on the matching between the elements in the current source array and the resistor array.

5. CONCLUSIONS

In this paper, the circuit design and modeling to implement a 1.8 V, 10-bit DAC cell were presented. This DAC cell was designed for maximum performance with minimum area, while incorporating a novel high gain op-amp to overcome the limitations of a single 1.8 V power supply.

The five stage servoing op-amp provides 130 dB gain and 81° phase margin. Accurate modeling of the op-amp transfer function was presented along with a brief overview of the feed-forward parallel path compensation technique. Simulations show that this DAC cell has near zero INL and DNL when no mismatches are added. The DAC cell presented is ideal for applications where a small, low frequency, calibration DAC is needed for adjusting bias conditions in mixed-signal ASICs.

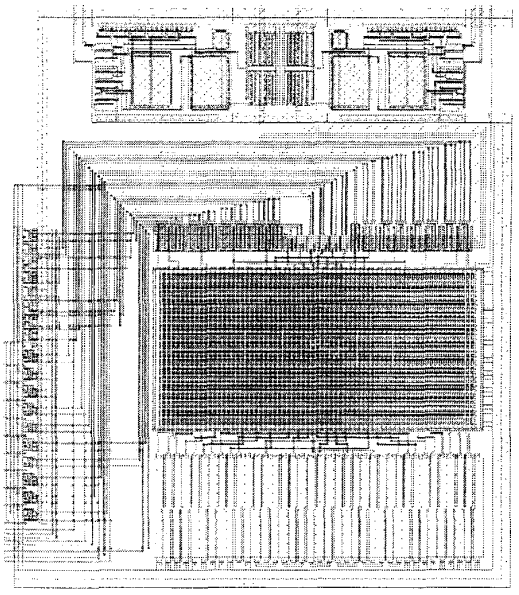

Figure 8: DAC Cell Layout in 0.18 μm CMOS.

6. REFERENCES

[1] C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, December 1998.

[2] A. Bugeja, B.-S. Song, P. Rakers, and S. Gillig, "A 14-b, 100-MS/s CMOS DAC designed for spectral performance," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 12, pp. 1719–1731, December 1999.

[3] J. Bastos, A. Marques, M. Steyaert, and W. Sansen, "A 12-Bit intrinsic accuracy high-speed CMOS DAC," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 13, pp. 1959–1969, December 1998.

[4] A. Thomsen, E. Angel, S. Wu, A. Amar, L. Wang, "A DC measurement IC with 130nV$_{pp}$ noise in 10Hz," in *Proc. of the IEEE International Solid-State Circuits Conference*, February 2000, pp. 334–335.

[5] R. Eschauzier, and J. Huijsing, *Frequency Compensation Techniques For Low-Power Operational Amplifiers*, Dordrecht, The Netherlands: Kluwer Academic Publishers, 1995.

[6] A. Thomsen, "A 5 stage chopper stabilized instrumentation amplifier using feed-forward compensation," in *Proc. of the IEEE VLSI Circuits Symposium*, June 1998, pp. 220–223.