AN EXTENDED RADIX-BASED DIGITAL CALIBRATION TECHNIQUE FOR MULTI-STAGE ADC

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ABSTRACT

A radix-based digital self-calibration technique for multi-stage analog-to-digital converter(ADC) is presented. This technique can correct errors due to capacitor mismatch and finite opamp gain. The equivalent radix of each stage is extracted by measuring the discontinuity on the ADC transfer curve and iteratively adjusting the equivalent radix to minimize this discontinuity. A much more accurate analog to digital conversion can be achieved by calculating the digital output based on these equivalent radices. While the principle is very similar to the method in [1], this technique can be applied to those ADCs having multiplying-digital-to-analog-converter(MDAC) with more widely used "capacitor-flip-over" structure. This can be seen as an extension to [1].

1. INTRODUCTION

Digital self-calibration is a very promising technique to improve the accuracy of switched-capacitor pipeline ADCs, which is largely limited by capacitor mismatch and finite opamp gain [1]-[5]. The key concept of this technique is to measure these errors by the converter itself, and then use these measured values to correct the converter in digital domain. The most attractive feature of digital self-calibration technique is the minimum extra analog circuit involved. So it could be simpler, robust, flexible, easier to implement and potentially power efficient compared to those analog techniques or laser trimming.

Among various digital self-calibration schemes for pipeline ADC or cyclic ADC, some have the limitation that the calibration accuracy of each stage depends on the accuracy of its following stages, so the calibration has to be done step by step from the end stages to front stages up the pipeline[2] [3]. But the methods proposed in [1][4][5] do not suffer from this limitation: the calibration of each stage is independent on prior calibration of other stages, so they are more suitable for cyclic ADCs. To achieve this independence, in [4], the ideal output of each stage during calibration is zero, which makes it less effective to compensate the finite opamp gain. However, in [5], an innovative iterative equivalent radix extraction algorithm was proposed for the calibration of single stage cyclic ADC(1-bit-per-stage). This algorithm was extended to multi-stage ADC in [1], but the MDAC in each stage had to be modified from the "capacitor-flip-over" structure.

In this paper, the radix-based digital self-calibration technique proposed in [1] is extended to the ADC with more widely used "capacitor-flip-over" MDAC. The accuracy of proposed scheme is comparable with [1], and no extra circuit beyond [1] is needed. In the following sections, the details of this calibration scheme will be presented.

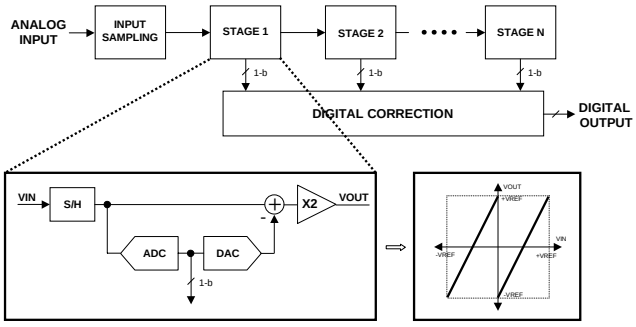

Fig. 1. Block diagram of a typical pipeline ADC.

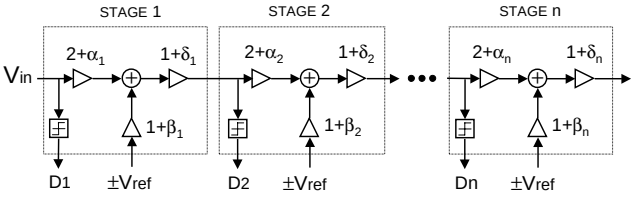

Fig. 2. Function diagram of a 1-bit-per-stage pipeline ADC.

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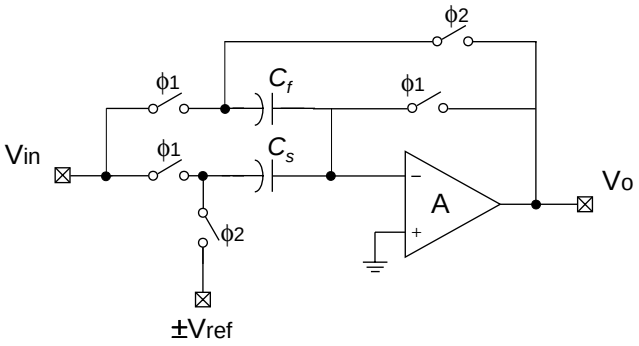

Fig. 3. MDAC with "capacitor-flip-over" structure.

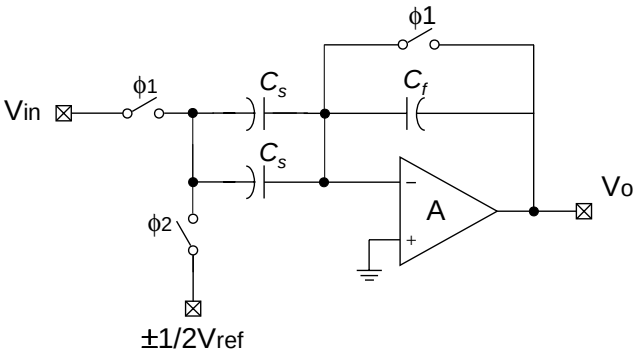

Fig. 4. MDAC with "non-capacitor-flip-over" structure.

2. PROPOSED RADIX-BASED DIGITAL SELF-CALIBRATION

Fig. 1 shows the block diagram of a typical pipeline ADC. Here, a 1-bit-per-stage architecture is used because it's simple, fast and easy to calibrate. Assuming that the ADC is ideal and the radix is 2(the radix is usually chosen to be less than 2 in practical design to account for opamp and comparator offsets which could possibly make the stage output go out of signal range), the analog input and output relation is given by:

$$\begin{aligned} V_o &= 2V_i - D \cdot V_{ref} \\ &= 2(V_i - D \cdot V_{ref}/2), \end{aligned} \tag{1}$$

where D is ± 1 depending on the input voltage level. In transistor level circuit implementation, the non-ideal effects such as capacitor mismatch and finite opamp gain will cause errors to the conversion. Fig. 2 shows the function diagram of a pipeline ADC with the presence of non-ideal terms. α_i, β_i and δ_i denote the errors caused by capacitor mismatch and finite opamp gain. Since the signal independent charge injection and opamp offset only cause offset to the pipeline ADC without affecting the linearity as far as the analog output of each stage is kept within the signal range, here we only focus on the other error terms and did not show them in Fig. 2.These shown error terms are based on the MDAC with commonly used "capacitor-flip-over" structure shown in Fig. 3. The analog input and output relation is:

$$V_o = (1+\delta)\big((2+\alpha)V_i - D(1+\beta)V_{ref}\big). \tag{2}$$

For a non-ideal pipeline ADC with all the error terms mentioned above, the conversion will be inaccurate and a calibration is needed.

For single stage cyclic ADC, we can rewrite Eq.(2) as:

$$V_o = (1+\delta)(2+\alpha)\big(V_i - D\frac{1+\beta}{2+\alpha}V_{ref}\big). \tag{3}$$

It is obvious that the Eq.(3) is equivalent to Eq.(1) if we take $(1+\delta)(2+\alpha)$ as the new radix and $\frac{2(1+\beta)}{2+\alpha}V_{ref}$ as the redefined reference voltage. So the correct digital output of the ADC can be obtained by using a simple radix calculation based on the modified radix value[5]:

$$\begin{aligned} D_{out} &= D_n + D_{n-1}\cdot(ra) + D_{n-2}\cdot(ra)^2 + \cdots \\ &\quad + D_2\cdot(ra)^{n-2} + D_1\cdot(ra)^{n-1}, \end{aligned} \tag{4}$$

where ra is the new radix number taking into account the effects of all error terms. However, this algorithm can not be applied to a multi-stage ADC, because the redefined reference voltage will be different from stage to stage. To solve this problem, a "non-capacitor-flip-over" MDAC shown in Fig.4 was proposed in[1]. In this modified MDAC scheme, the analog input V_i and the reference V_{ref} will see identical error terms, so the analog input and output relation can be written as[1]:

$$V_o = ra\cdot(V_i - D\cdot V_{ref}/2). \tag{5}$$

Notice the radix number ra varies from stage to stage but the reference voltages are same for all the stages. The digital output of the ADC can be calculated by[1]:

$$\begin{aligned} D_{out} &= D_n + D_{n-1}\cdot ra_{n-1} + D_{n-2}\cdot(ra_{n-1})(ra_{n-2}) \\ &\quad + D_{n-3}\cdot(ra_{n-1})(ra_{n-2})(ra_{n-3}) + \cdots \\ &\quad + D_1\cdot(ra_{n-1})(ra_{n-2})\cdots(ra_2)(ra_1). \end{aligned} \tag{6}$$

However, the conventional "capacitor-flip-over" MDAC is more widely used in practical design due to its large feedback factor. So it is very desirable to find a more general solution which can be applied to both MDAC structures. Fortunately, such a general solution does exist and can be easily achieved after some simple manipulations.

To understand how this general solution works, we can do some equivalent transformations to the pipeline ADC's

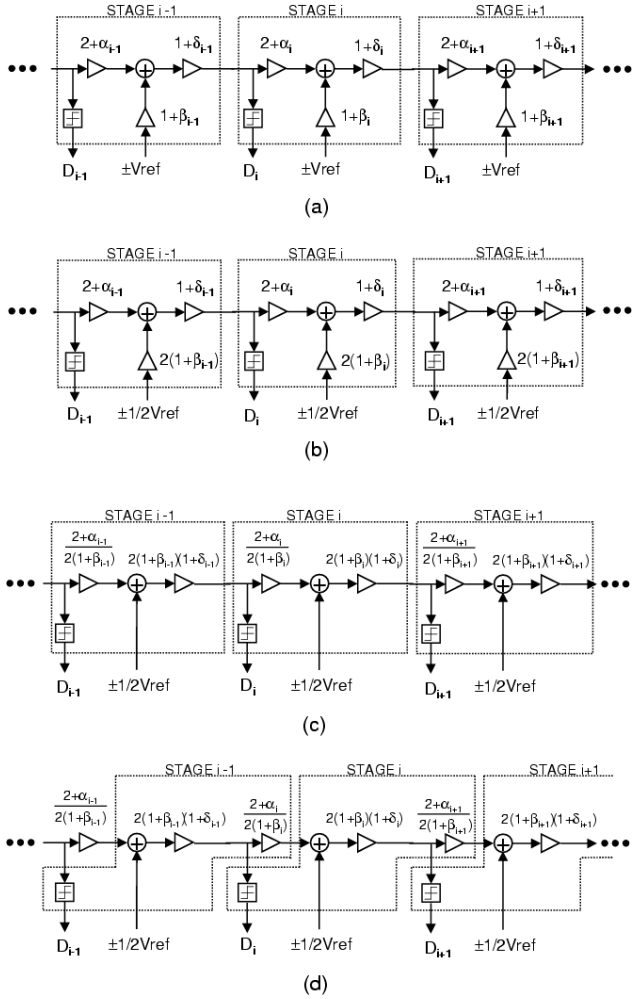

Fig. 5. Equivalent transformation of a pipeline ADC.

function diagram shown in Fig.2. The procedure of transformation is shown in Fig.5. Fig.5(a) is the function diagram of a pipeline ADC with all the error terms. If we change V_{ref} to $1/2V_{ref}$ and adjust the gain factor of reference voltage correspondingly, we get the equivalent function diagram Fig.5(b). Then we merge the gain factor of the reference voltage into the input gain factor and the output gain factor to arrive at Fig.5(c). Now we redefine the stage input and output, so each stage's input gain factor is merged into its previous stage's output gain factor and the next stage's input gain factor is merged into this stage's output gain factor. The resulted equivalent ADC is shown in Fig.5(d). It can be easily noticed that Fig.5(d) is the function diagram of a pipeline ADC whose stage input and output relation can be written in the form of Eq.(5). And the equivalent radix of each stage is given by:

$$ra_i = (1+\beta_i)(1+\delta_i)\left(\frac{2+\alpha_{i+1}}{1+\beta_{i+1}}\right). \qquad (7)$$

That means we can use Eq.(6) to calibrate a multi-stage ADC with "capacitor-flip-over" MDAC. So this radix-based digital calibration scheme is a general calibration technique and can be applied to any 1-bit-per-stage pipeline or cyclic ADC without the limitation on the structure of MDAC. Here, the key point is to redefine the stage input and output, so the desired form of input and output equation can be achieved. One issue in from this redefinition is that the comparator within each stage still see the original input voltage before the redefinition. This equivalently adds offset to the comparator. Fortunately, this is usually not a problem because this added offset is small and can be compensated by the digital redundancy of the pipeline ADC without performance degradation.

Since an inaccurate pipeline ADC can be linearized by radix-based digital calibration as discussed above, next the question is how to obtain these equivalent radices. Although Eq.(7) tells us the relation between equivalent radix and all existing error terms, we can't use it to calculate the equivalent radix because those error terms can not be known in advance. However, an iterative equivalent radix extraction algorithm very similar to [1] can be employed to do this job and will be described next.

As demonstrated in [1], the discontinuity will occur to the pipeline ADC transfer curve where there is a bit transition. These discontinuities are referred as *major-carry jumps* [1] which should be less than 1-LSB if we use correct radices to calculate the digital output. If the radices we used are not the actual radices, the *major-carry jumps* would be larger than 1-LSB. Based on this observation, we can extract the equivalent radix as follows: First, we give an initial estimated value for the radix. Then we approach the actual radix iteratively:

$$ra_i[n+1] = ra_i[n] - \Delta \cdot (mcj[n] - 1LSB), \qquad (8)$$

where n is the iteration index and Δ is the step size. After certain number of steps, the estimated radix will converge to the actual equivalent radix.

During each iteration, to measure the *major-carry jump*, the analog input is set to zero and the bit value is forced to 1, the resulted digital output is D1 (after radix based calculation). Next, the bit value is forced to 0, the resulted digital output is D0 (after radix based calculation). The *major-carry jump* is:

$$mcj[n] = D1 - D0. \qquad (9)$$

When there are 2 or more radices need to be determined, we can alternatively update their values based on the latest values of other radices until all the *major-carry jumps* are equal to 1-LSB, which indicates that a linear transfer curve has been achieved. More detailed description can be found in [1].

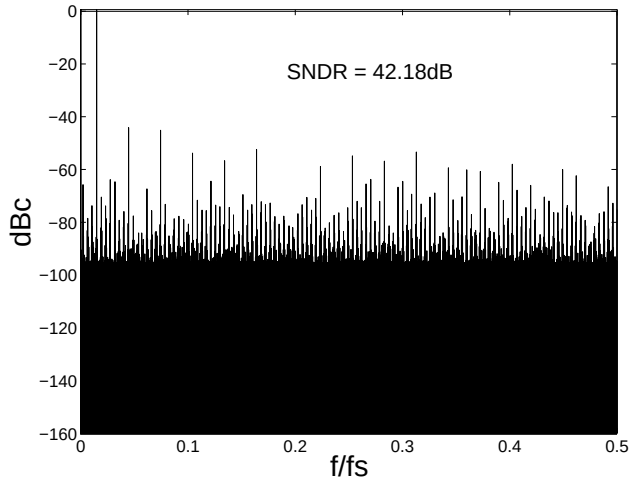

Fig. 6. Output spectrum of the prototype ADC before calibration

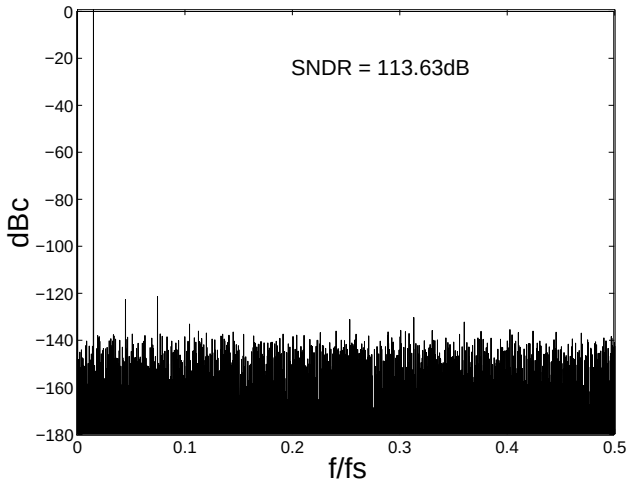

Fig. 7. Output spectrum of the prototype ADC after calibration

3. SIMULATION RESULTS

Some behavior simulations have been done to verify the proposed calibration scheme. The ADC in simulation is a 20-bit two-stage cyclic ADC(1-bit-per-stage). The nominal radix value has been set to 1.95. 40dB opamp loop gain and 1% capacitor mismatch were assumed in simulation. The two equivalent radices calculated by using Eq.(7) are 1.899975 and 1.961464. The values extracted by applying proposed algorithm are 1.899969 and 1.961468. The iterative radix extraction algorithm converges very quickly. Here the number of iteration is only 128(see Eq.(8)). And the radix update step size Δ is 2^{-20}. Fig.6 shows the output spectrum of the prototype ADC without calibration(assumed radix of 1.95). The SNDR is only about 42dB. Fig.7 shows the simulation results of the same ADC with proposed calibration scheme. The SNDR is about 113dB. The proposed calibration scheme is very effective to improve the linearity of multistage ADC.Even the ADC with very large capacitor mismatch and very low opamp gain can be calibrated to have more than 18bit linearity.

4. CONCLUSIONS

The errors caused by capacitor mismatch and finite opamp gain in multistage pipeline ADCs can be corrected by adjusting the radices used in the digital output calculation. This radix-based digital self-calibration technique is very simple, accurate and robust. It can improve the linearity of pipeline ADC dramatically as shown in simulation results. While two-stage cyclic ADC was used in simulation to demonstrate the effectiveness of proposed scheme, this calibration technique can be applied to any multi-stage pipeline or cyclic ADC without the limitation on MDAC structure. Although 1-bit-per-stage ADC architecture is preferred in this calibration scheme for it's simplicity, 1.5-bit-per-stage or multi-bit-per-stage architecture can also be used with added circuit complexity.

5. REFERENCES

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