32.2 A 0.5 to 2.5GHz PLL with Fully Differential Supply-Regulated Tuning

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PLLs are important building blocks that are used to generate and distribute clocks in all high-performance digital systems. Integrating PLLs on large digital chips in deep submicron processes poses three main challenges. First, power supply noise caused by increased digital switching currents degrades the jitter performance of the VCO. Second, the wide loop bandwidth required to suppress ring oscillator noise exacerbates the phase noise caused by charge-pump noise. In particular, the flicker noise in short-channel-length devices dominates the overall in-band noise. Finally, the need to integrate many clock-distribution PLLs on a single chip mandates that they each occupy a small area. This paper describes a PLL that alleviates power supply noise through the use of a fully differential supply-regulated tuning method and suppresses charge-pump flicker noise by using a passive resistor in place of a conventional active current source. A ring VCO is used rather than an inductor-based VCO to satisfy die area constraints. The PLL operates over a wide frequency range (0.5 to 2.5GHz) with 3.29ps rms jitter at 2.4GHz and consumes 25mW from a 1.8V supply.

A block diagram of the PLL is shown in Fig. 32.2.1. The need for wide operating range and small area mandate the use of a ring-type VCO in the PLL. It is well known, however, that ring VCOs employing inverter-based delay cells are very sensitive to power supply noise. For the best supply noise immunity, a fully differential signal path is desired. PLLs employing differential charge-pumps and loop filters (LFs) are common, but existing ring-VCO tuning methods are inherently single ended. The LF output, therefore, must pass through a differential-to-single-ended converter circuit before it can be used as the VCO control voltage [1]. This single-ended control voltage, however, is very susceptible to supply noise. For this reason, a differentially controlled VCO is desired.

An existing technique to isolate the PLL from supply noise uses the supply voltage of the VCO as the control voltage [2]. A buffer between the output of the loop filter and the VCO acts as a supply regulator (Fig. 32.2.2). This technique is not, however, immune to ground noise. In this work, fully differential tuning is achieved by using the difference between the positive and negative supplies of the VCO as the tuning voltage as shown at the bottom of Fig. 32.2.2. Ideally, delay is proportional to the difference of the positive and negative supplies and is not affected by the common-mode voltage, although the body effect limits common-mode rejection.

In deep submicron processes, the flicker noise corner is high enough that flicker noise is the dominant contributor to PLL phase noise, despite being filtered below the loop bandwidth. Therefore, it is desirable to size devices within the delay cell as large as possible. As device sizes increase, device parasitics also increase and the oscillation frequency decreases. To minimize parasitics, a simple CMOS inverter is used as a delay cell and the minimum number of delay stages (3) is used. The single-ended nature of an inverter is tolerated since the supply is regulated. If the output of the fully differential buffer is used directly as the virtual supply, the opamp must drive a prohibitively large current into the VCO, which is operating at a high frequency. A solution is to add a transistor between the actual supply and the virtual supply, so that current is drawn from the actual supply rather than the output of the opamp. The final VCO configuration incorporating this idea is shown in Fig. 32.2.3.

While the VCO noise is high-pass filtered by the PLL, the charge-pump noise is low-pass filtered. Using a wide bandwidth to suppress VCO noise, therefore, means the charge-pump low-frequency noise must be minimized. As mentioned earlier, flicker noise is large in deep submicron processes. It would be advantageous if we could use a passive device to generate the charge-pump current rather than an active device. In a traditional charge-pump (Fig. 32.2.4), the up and down pulses from the PFD drive switches connected in series with transistor current sources, which convert the voltage pulses to current pulses of the same width. The down current pulse is subtracted from the up current pulse at the output node and the resulting signal drives the loop filter. The noise from both the up and down current sources directly appears on the loop filter. The proposed charge-pump is shown in Fig. 32.2.4. The voltage pulses are converted to current pulses by the resistors between the up and down inputs and the opamp inputs. Instead of subtracting the current signals before driving the loop filter, the filter is split in half and the difference information is contained in the resulting differential signal.

As desired, the charge-pump current is now defined by a flicker-noise-free resistor rather than a transistor. The opamp noise adds a voltage error on the control voltage as indicated in Fig. 32.2.4. The control-voltage-to-output transfer function of the PLL is bandpass, however, so the opamp flicker noise contribution is significantly reduced. A plot of the simulated charge-pump current noise spectrum is included in Fig. 32.2.4. For the sake of comparison, the current noise spectrum of a traditional charge-pump with equal pumping currents is also shown. It is apparent that the flicker noise corner is reduced in the proposed design. These noise spectra were obtained from periodic noise simulations which take into account the fact that the traditional charge-pump current noise is passed only during the fraction of the reference period when the PFD reset pulse is high.

The PLL was fabricated in a 0.18µm CMOS technology. The measured jitter histogram showing 3.29ps rms jitter at an oscillation frequency of 2.4GHz is shown in Fig. 32.2.5. In order to quantify the dynamic power-supply noise sensitivity, a 50mV tone was added to the supply and the jitter degradation was measured. The measured jitter degradation caused by a 1MHz tone is 12.3ps rms. The performance of the PLL is summarized in the table shown in Fig. 32.2.6 and a die micrograph is shown in Fig. 32.2.7.

Acknowledgment:
The authors thank National Semiconductor for providing IC fabrication and particularly Orhan Norman for his sponsorship. This work is supported by SRC under contract 2003-HJ-1076.

References:
[1] G. Wei, et al., "A 500MHz MP/DLL Clock Generator for a 5Gb/s Backplane Transceiver in 0.25µm CMOS," *ISSCC Dig. Tech. Papers,* pp. 464-465, Feb., 2003.
[2] S. Sidiropoulos, et al., "Adaptive Bandwidth DLLs and PLLs using Regulated Supply CMOS Buffers," *Proc. IEEE Symp. VLSI Circuits*, pp. 124–127, June, 2000.

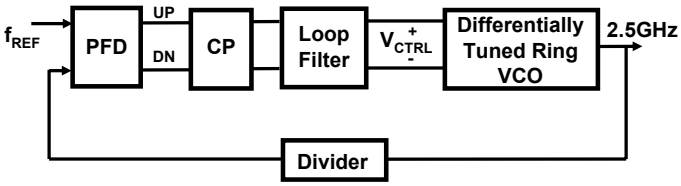

Figure 32.2.1: PLL block diagram.

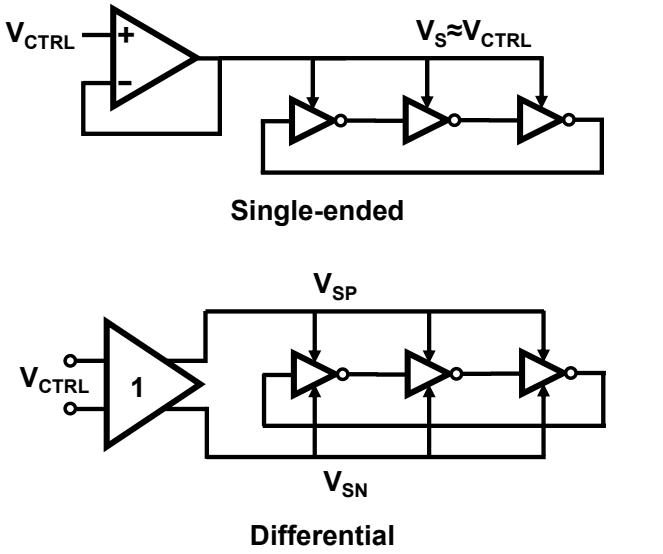

Figure 32.2.2: Single-ended and differential supply-regulated tuning.

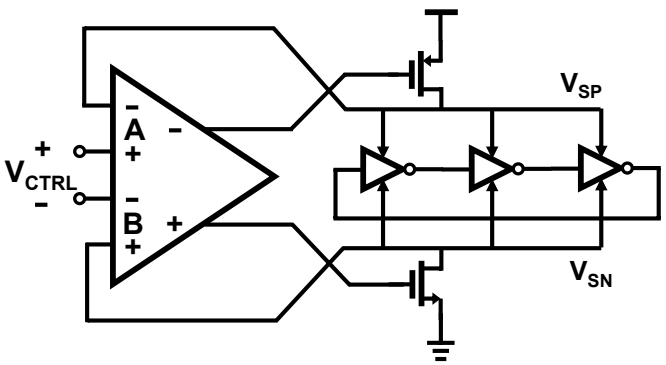

Figure 32.2.3: Differentially tuned VCO.

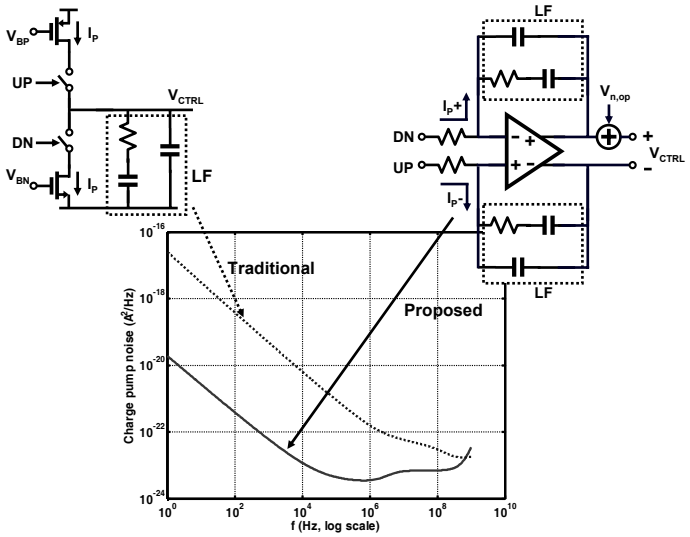

Figure 32.2.4: Traditional versus proposed charge pump and their current noise spectra.

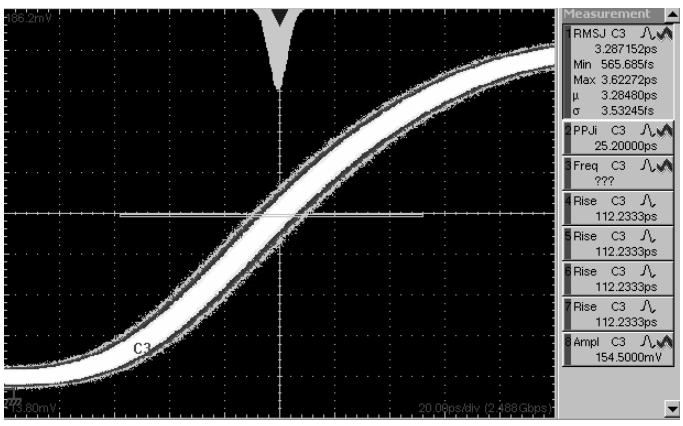

Figure 32.2.5: Measured PLL jitter histogram.

Technology	0.18μm CMOS
Frequency Range	0.5 to 2.5GHz
Power Dissipation	25mW
Die Area	0.15mm^2
RMS Jitter	3.29ps
Dynamic Supply Noise Jitter Degradation (50mV, 1MHz tone)	12.3ps

Figure 32.2.6: Performance summary.

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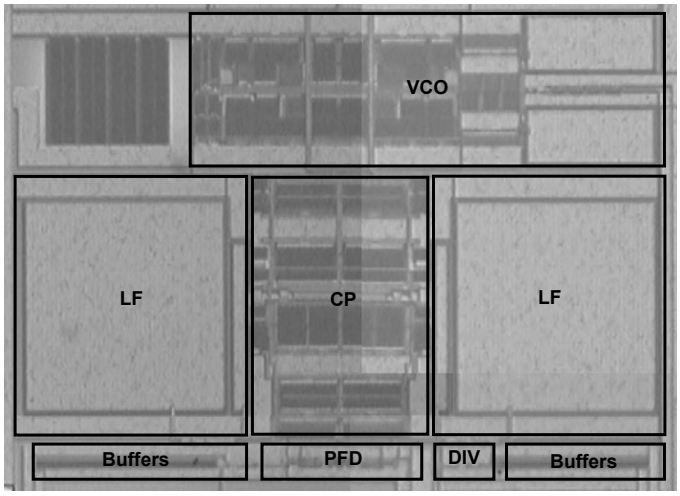

Figure 32.2.7: Die micrograph.

