A 0.9-V 12-mW 5-MSPS Algorithmic ADC With 77-dB SFDR

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***Abstract*—An ultra-low-voltage CMOS two-stage algorithm ADC featuring high SFDR and efficient background calibration is presented. The adopted low-voltage circuit technique achieves high-accuracy high-speed clocking without the use of clock boosting or bootstrapping. A resistor-based input sampling branch demonstrates high linearity and inherent low-voltage operation. The proposed background calibration accounts for capacitor mismatches and finite opamp gain error in the MDAC stages via a novel digital correlation scheme involving a two-channel ADC architecture. The prototype ADC, fabricated in a 0.18 μm CMOS process, achieves 77-dB SFDR at 0.9 V and 5 MSPS (30 MHz clocking) after calibration. The measured SNR, SNDR, DNL, and INL at 80 kHz input are 50 dB, 50 dB, 0.6 LSB, and 1.4 LSB, respectively. The total power consumption is 12 mW, and the active die area is 1.4 mm^2.**

***Index Terms*—Algorithmic ADC, background digital calibration, low power, low voltage, pipelined ADC, two channel ADC architecture.**

I. Introduction

THE continued downscaling of power supply voltage in the state-of-the-art deep-submicron CMOS technology brings many new challenges to the high performance switched-capacitor (SC) circuit design. First, the gate overdrive voltage of CMOS sampling/floating switches is becoming too small to achieve fast settling, and it could reach the point where the floating switch would fail to turn on as the supply voltage becomes less than the sum of the NMOS and PMOS threshold voltages. Second, high gain opamps, one of the most important building blocks in SC circuits, are very difficult to design at ultra-low-voltage supplies because most commonly used gain boosting techniques are no longer feasible. Third, it is more difficult to achieve a good signal-to-noise ratio (SNR) due to reduced signal range and increased noise coupling in high density mixed-signal integrated circuits (ICs). Thus, in order to achieve high performance at reduced supply voltage, it is necessary to explore other design techniques that can overcome or mitigate these issues.

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This paper presents a prototype algorithmic ADC design which directly addresses the low-voltage design issues mentioned above. It incorporates an opamp resetting technique [1]–[4] to achieve high speed operation at very low supply voltage. Because all nodes of this resetting technique operate within the supply voltage rails, there are no added long-term reliability issues as in the clock boosting and bootstrapping techniques [5]–[7]. The resetting technique, which works by placing the opamp into a unity-gain feedback configuration during reset, is also much faster than the switched opamp technique [8] which turns the opamp on/off in every clock cycle. The prototype ADC presented in this paper also incorporates a new background digital calibration method which can efficiently correct for errors caused by finite opamp gain, capacitor mismatches, and incomplete linear settling [9]. As a result, the opamp can be optimized for high speed and maximum signal swing instead of large open loop gain. So it is possible to maintain a good SNR and high-speed conversion at a reduced power supply voltage without placing a large burden on power consumption.

The prototype two-stage algorithmic ADC (design details to follow) demonstrates a 77-dB SFDR performance at 5 MSPS (30 MHz clocking) operation, while consuming only 12 mW at 0.9-V supply. We anticipate that this design can easily be migrated to a straight pipeline ADC design producing a similar performance at 30 MSPS (same 30 MHz clocking with bias current scaling) with about 30-mW power consumption at 0.9 V.

The rest of this paper is organized as follows. Section II describes the proposed calibration scheme, Section III details circuit design, experimental results are summarized in Section IV, and conclusions are given in Section V.

II. Background Digital Calibration Using Correlation

Various calibration techniques have been proven effective in improving the accuracy of high performance pipelined ADCs. During the past two decades, many different calibration schemes have been developed to overcome the accuracy limitations set by analog inaccuracies [10]–[23]. However, due to their considerably increased power consumption and circuit complexity, these calibration techniques are usually only adopted in ADCs with 14-bit or higher resolution. For lower resolution ADC design, brute force design optimization without calibration or trimming is commonly applied to push the performance. However, this design practice is becoming increasingly more difficult at very low supply voltage, mainly due to the low opamp gain problem mentioned earlier. Therefore, it would be highly desirable to introduce some calibration schemes to relax the opamp gain requirement even for 12-bit or lower resolution ADCs but with

ultra-low-voltage operation. Based on this observation, we propose a fast and accurate correlation-based background digital calibration scheme in the context of a 1.5-bit-per-stage pipelined or cyclic ADC architecture. In the proposed calibration scheme, the errors due to capacitor mismatches and finite opamp gain are corrected by recalculating the digital output based on the equivalent radix value of each stage. The equivalent radices are extracted on-line using a correlation-based algorithm. To minimize the interference from the input signal in the correlation-based radix extraction, a two-channel ADC architecture is used. The total capacitance used is the two-channel ADC is same as the equivalent single-channel ADC, resulting in similar total power consumption. There is only a small amount of power consumption overhead in the two-channel ADC architecture due to the extra comparators used and other miscellaneous components. The details of this calibration scheme are described in the following.

The multiplying digital-to-analog converter (MDAC) is the key building block in pipelined (or algorithmic) ADCs. In the transistor-level circuit implementation of an MDAC, the nonideal effects coming from capacitor mismatches and finite opamp gain will degrade the conversion accuracy. Fig. 1 shows a functional diagram of a 1.5-bit-per-stage pipeline ADC in the presence of these nonideal terms, α_i, β_i, and δ_i, where the results of capacitor mismatches are represented by α_i and β_i, and the finite opamp gain by δ_i. The "capacitor-flip-over" MDAC structure shown in Fig. 2 is assumed in this functional diagram. Since signal-independent charge injection and opamp offset only add to the overall pipeline ADC offset, they are not shown in Fig. 1. The resulting analog output of an MDAC is

$$V_o = (1+\delta)\big((2+\alpha)\cdot V_i - D\cdot(1+\beta)\cdot V_{\rm ref}\big) \qquad (1)$$

where D is ± 1 or 0 depending on the input voltage level (i.e., the sub-ADC output). In practical pipeline ADC implementation, the conversion will be inaccurate due to these nonideal terms and some kind of calibration would be needed to achieve improved performance.

One simple and robust calibration method is the equivalent radix calibration [4], [9], [20], which we have adopted for this implementation. In the radix-based calibration, the correct digital output of a nonideal ADC can be calculated by applying the measured/extracted radix numbers (one per 1.5-bit MDAC stage) to the uncorrected digital code [4]:

$$\begin{aligned} D_{\rm out} = {} & D_n + D_{n-1}\cdot ra_{n-1} + D_{n-2}\cdot(ra_{n-1})(ra_{n-2}) \\ & + D_{n-3}\cdot(ra_{n-1})(ra_{n-2})(ra_{n-3}) \\ & + \cdots + D_1\cdot(ra_{n-1})(ra_{n-2})\cdots(ra_2)(ra_1). \end{aligned} \qquad (2)$$

Because of the 1.5-bit MDACs used, the "three-level LSB" (± 1 or 0) is denoted by D_n and the "three-level MSB" by D_1. The first MDAC radix is ra_1 and the last MDAC radix is ra_{n-1} (total of $n-1$ MDAC stages) in this nonideal n-bit ADC output code. The equivalent radix of each stage is given by [9]

$$ra_i = (1+\beta_i)(1+\delta_i)\left(\frac{2+\alpha_{i+1}}{1+\beta_{i+1}}\right). \qquad (3)$$

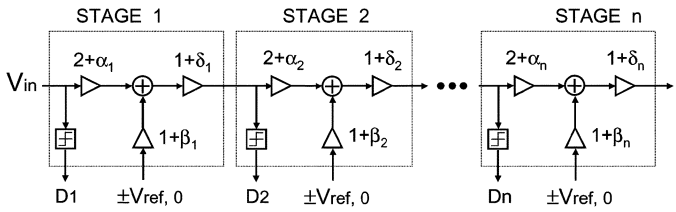

Fig. 1. Functional diagram of a pipeline ADC (1.5 bit per stage).

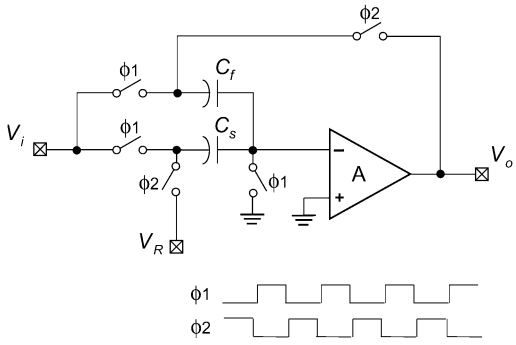

Fig. 2. Capacitor-flip-over MDAC.

The index i represents the MDAC stage number under observation, and the index $i+1$ represents the following MDAC stage number.

Equation (3) can give us insight to the relationship between the equivalent radix and the error terms in a nonideal pipelined ADC. However, it cannot be used for calibration because these error terms cannot be known in advance. In [4], an accurate foreground radix extraction/measurement scheme was employed to obtain the equivalent radices in a nonideal pipeline ADC. However, the ADC operation had to be interrupted to perform this radix extraction/measurement. Although the calibration can be done during the system power-up or standby, it would be desirable to run the calibration at all times to track device and environmental variations. An ideal solution should be in the form of a background calibration scheme which can detect the equivalent radices without interrupting the normal A/D conversion.

In pipelined ADCs which incorporate digital redundancy, there is an efficient way to do the background radix detection. We propose this method as illustrated in Fig. 3. A scaled (by approximately 1/8) binary pseudorandom noise sequence is injected at the input of the sub-ADC. The resulting ADC digital output D_o is

$$\begin{aligned} D_o = {} & \left(V_i + Q_N + \left(\frac{1}{8}\right)P_N\right)\cdot ra_{\rm es} \\ & - \left(Q_N + \left(\frac{1}{8}\right)P_N\right)\cdot ra + O_N \end{aligned} \qquad (4)$$

where P_N is the pseudorandom noise sequence, ra is the actual radix, $ra_{\rm es}$ is the estimate of the radix in digital domain, Q_N is the quantization noise of this stage, and O_N includes all other noise sources such as thermal noise and quantization noise of the back-end ADC.

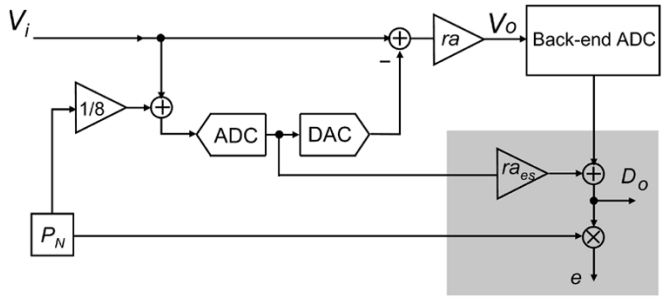

Fig. 3. Background equivalent radix extraction.

If we correlate the ADC digital output D_o with the same pseudorandom sequence (see Fig. 3), and assuming a perfect correlation process, we get the radix error

$$e = \left(\frac{1}{8}\right)(ra_{\rm es} - ra). \tag{5}$$

A near-perfect correlation process can be assumed if the pseudorandom sequence is long enough, and the actual radix can be calculated by $ra = ra_{\rm es} - 8e$.

At a glance, this radix detection scheme may seem similar to the interstage gain error calibration schemes proposed in [21] and [22]. The key modification here is to inject the pseudorandom sequence at the input of the sub-ADC instead of the sub-DAC. This change gives us a number of advantages. First, the injected pseudorandom noise can now be considered time-varying (but limited/bounded) comparator offsets. Thus, it can be absorbed and corrected by the digital redundancy of the pipeline ADC without any performance degradation. It does not require that the input signal magnitude be reduced when injecting the pseudorandom noise. Second, we do not need to face the complications of needing an accurate match of scaling (the 1/8 value) in the analog and digital domain. Third, in the circuit implementation, the injection of pseudorandom noise can be implemented by randomly varying the comparator threshold level (comparator dithering). There is no fundamental change to the MDAC, which is the most critical and sensitive block in the pipeline ADC design. As a result, we can expect faster operation and less noise coupling from this radix detection scheme.

Although the proposed correlation-based algorithm of Fig. 3 can be employed "as is" to extract the equivalent radix, the calibration process would be much slower than the foreground algorithm in [4]. The main reason is the strong interference from the input signal to the ADC. Specifically, when we correlate the ADC's digital output with the pseudorandom sequence to detect the radix error, the input signal is transformed into noise at the same time (because the input signal is uncorrelated to the pseudorandom sequence). This input signal transformed noise will interfere with the radix error detection, making it very slow to reach high accuracy. This situation is illustrated in Fig. 4. As shown in the figure, e is the small radix error that needs to extracted. It is first modulated by a pseudorandom sequence P_n, then added to the ADC's input signal $V_{\rm in}$. After A/D conversion, it is demodulated in the digital domain. Comparing the spectrum before and after demodulation, we can observe an obvious

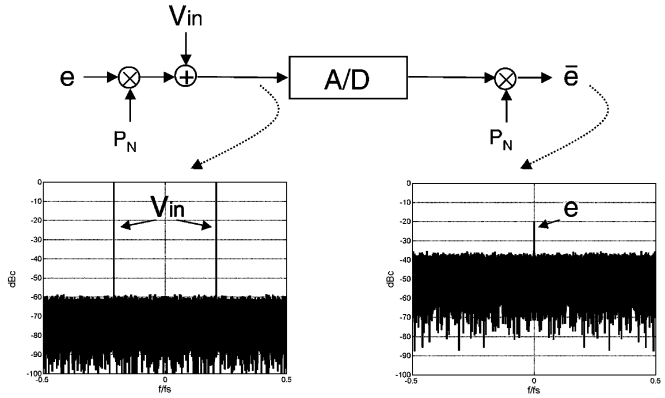

Fig. 4. Interference from the input signal.

rise of the noise floor that is due to the input signal being transformed into noise. Although other noise sources such as thermal noise, $1/{\rm f}$ noise, and back-end ADC's quantization noise also affect the detection, the signal transformed noise is the dominant interference because the signal is usually strong (e.g., full scale input), and other noise sources are much smaller in comparison. This interference issue is common to all correlation-based calibration techniques, and it will limit the calibration accuracy. This problem is usually mitigated by increasing the length of the pseudorandom sequence, but it is not very effective because the noise level only goes down by 3 dB for each doubling of the sequence length. The principle behind this correlation method is equivalent to spread spectrum systems where strong interferences are spread to broadband noise in order to lower the interference spectrum density inside the signal band. The processing gain (the ratio of noise bandwidth to signal bandwidth) obtained is quantified by the spreading ratio which is proportional to the length of the pseudorandom sequence.

In order to improve the correlation efficiency of the proposed calibration scheme, which in current form faces a strong interference from the input signal, we propose a two-channel ADC architecture shown in Fig. 5. We place two identical ADCs in parallel to build a two-channel ADC. The two ADC channels are not time-interleaved. Instead, they take the same input signal but with opposite polarity. While the final ADC output is properly generated from the two parallel ADCs, the digital correlation/calibration path uses the opposite polarity to eliminate the signal to maximize correlation efficiency. While the channel mismatches can severely degrade the SNDR in *time-interleaved* two-channel ADCs, here they only mildly reduce the efficiency of the background radix extraction algorithm because of the incomplete cancelling of the ADC's input signal in the correlation process. No tones will be produced because the operations of these two ADC channels are parallel and synchronized, not time-interleaved.

At first glance, it may seem that the two-channel ADC architecture will double the die area as well as power dissipation. But in reality, it just increases the die area taken up by the comparators and the digital calibration circuitry. In high accuracy switched-capacitor circuits, the die size is dominated by the total capacitor area, as the capacitor size is determined by the kT/C noise requirement. Given the same SNR requirement and the same input signal magnitude, we can reduce each ADC

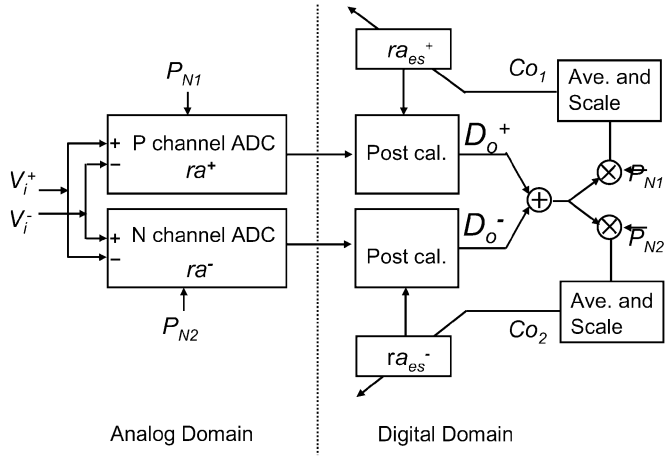

Fig. 5. Overall ADC with proposed background digital calibration.

channel's capacitor size by half. Thus, the total capacitor size of this proposed two-channel ADC is equal to the total capacitor size of a conventional single-channel ADC. Although the resulting noise power would be four times higher in the proposed two-channel ADC, the equivalent input signal power is also four times higher since the equivalent input signal magnitude is doubled (we take both ADC channels' digital output). Thus the SNR does not change. The main die size overhead is due to the fact that the number of comparators and digital calibration hardware is doubled (the numbers of opamps is also doubled but each opamp is smaller) in the two-channel ADC architecture. Despite this small overhead, this innovative two-channel architecture offers many desired features. First, it makes the correlation very effective, even if the interference cancellation is limited to only a 40-dB level due to channel mismatches. The digital correlation could easily be ten thousand times (power ratio of 40 dB) faster than conventional single channel architecture. Second, it is very simple and easy to implement. Neither complex digital signal processing (DSP) algorithm nor extra accurate analog circuitry is needed. In fact, because the two ADC channels are identical, there is little extra design and layout effort in circuit implementation. Third, this two channel calibration scheme is relatively insensitive to process and environment variation mainly because the two ADC channels have the same structure and very similar activity (processing the same input), so they track one another well.

Also illustrated in Fig. 5 is the overall iterative calibration algorithm used. Note that two uncorrelated pseudorandom sequences P_{N1} and P_{N2} are used to calibrate both channels simultaneously. To achieve a very robust operation, we iteratively extract the equivalent radix instead of using (5). First, we give an initial value to the estimated radix. Then we start an iteration to approach the actual radix value. The radix update equations are

$$\begin{aligned} ra_{\rm es}^{+}[n+1] &= ra_{\rm es}^{+}[n] - \Delta \cdot \left((Do^{+} + Do^{-}) \otimes P_{N1}\right) \\ ra_{\rm es}^{-}[n+1] &= ra_{\rm es}^{-}[n] - \Delta \cdot \left((Do^{+} + Do^{-}) \otimes P_{N2}\right) \end{aligned} \quad (6)$$

where $ra_{\rm es}^{+}$ and $ra_{\rm es}^{-}$ are the estimated radices of P and N channel ADC stages, respectively, P_{N1} and P_{N2} are the two pseudorandom noise sequences used in radix extraction, n is the iteration index, and Δ is the step size. One key advantage of this iterative method is that the calibration of each stage is insensitive to the errors of its back-end ADC.

As explained earlier, in order to accurately detect the radix error, the noise spectrum density after the spreading should be smaller than the radix error that we are trying to extract. Therefore, the minimum required length estimate is expressed as

$$L_{\min} \propto \left(\frac{V_{\rm int}}{e}\right)^2 \quad (7)$$

where $V_{\rm int}$ is the interference input signal, and e is the scaled radix error defined in (5). Equation (7) also clearly indicates the speed advantage of the proposed interference cancelling technique. For example, if the interference due to the ADC input signal is suppressed by 40 dB (1%) after cancellation, the length of PN could be 10 000 $\times$ (power ratio of 40 dB) smaller to achieve the same accuracy, which leads to a dramatic reduction of convergence time. The optimum radix estimate update size [Δ in (6)] is determined primarily based on the tradeoff between converging time and stability. Using a large step size can make the radix number to converge to its final value quickly but would suffer from reduced accuracy, and the iteration process can possibly become unstable and fail to converge. On the other hand, a step size that is too small would take a very long time to converge. It is possible to incorporate an adaptive algorithms to dynamically adjust the step size (e.g., gear shifting), but at an added implementation cost. In this study, we found that the step size of $\Delta = 2^{-7}$ (with digital output used in correlation normalized to ± 1 full scale) achieves stable operation with sufficiently fast and accurate convergence. The radix number was found to converge to its final value within 128 steps, each of which utilize a pseudorandom sequence length of 2^{12}. This implies that the overall cold convergence time (e.g., at power-up) is about 0.1 second for this ADC when operating at the sampling rate of 5 MSPS.

When there are multiple stages that need to be calibrated, we can choose to use more pseudorandom noise sequences to extract the radices simultaneously. Or we can share the same pseudorandom noise sequence among different stages and do the multistage ADC calibration by stepping through one stage at a time, so that the number of pseudorandom noise sequences can be reduced.

Some behavioral simulations have been performed to verify the proposed calibration scheme. The prototype ADC in simulation was a 17-bit two-stage cyclic/algorithmic ADC as shown in Fig. 6. Note that the pseudorandom sequences are shared between two stages in this example to reduce the number of pseudorandom sequence generators. Gaussian distributed random capacitor mismatches of $\sigma = 0.1\%$ and 60-dB opamp gain were assumed for this ADC. The two ADC channels were also given a fixed 1% $V_{\rm ref}$ input offset and 1% gain mismatches. In the equivalent radix extraction, the number of total samples was 2^{20}, and the radix update step size was $\Delta = 2^{-7}$, as given in (6). Note that this $\Delta = 2^{-7}$ is based on digital output Do^{+} and Do^{-} normalized to ± 1 full scale. One typical output spectrum of the prototype ADC is shown in Fig. 7. Fig. 7(a) shows the output spectrum of the prototype ADC before calibration. The SNDR

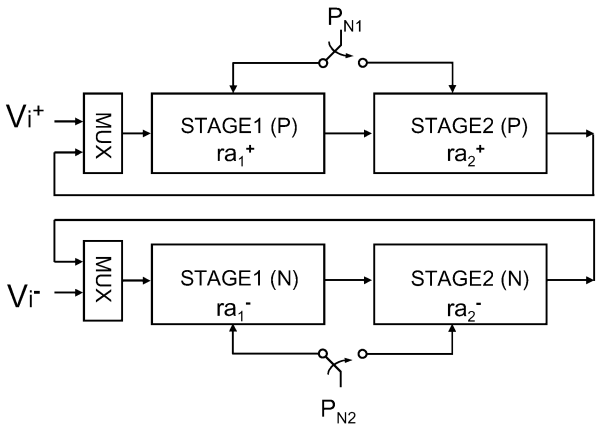

Fig. 6. Two-stage algorithm ADC with calibration.

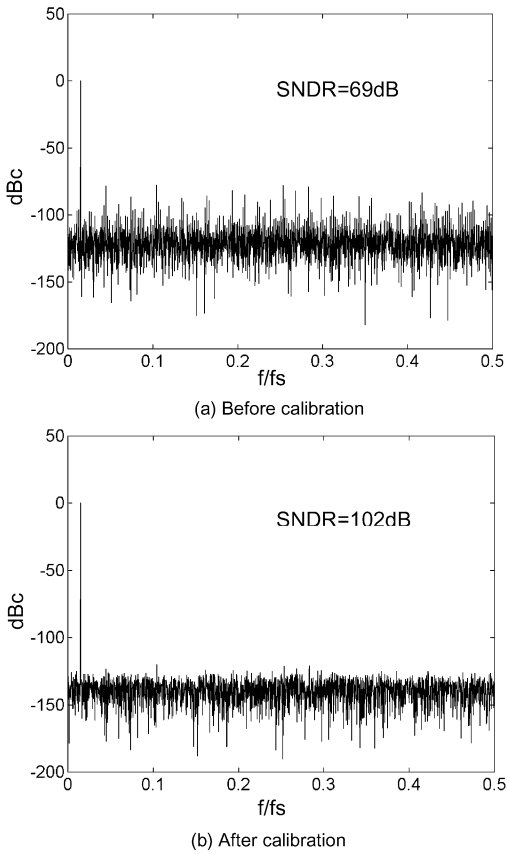

Fig. 7. Behavior simulation results.

before calibration is 69 dB. Fig. 7(b) shows the simulation results of the same ADC after the proposed background calibration is applied. The SNDR is improved to 102 dB.

III. Circuit Design

A prototype two-channel algorithm ADC as shown in Fig. 6 was designed in a 0.18 μm CMOS technology. Each channel includes two stages (1.5-bit/stage). It takes six clock cycles to process one sample and produce 12-bit binary output. In the following, the design details of some critical building blocks are described.

A. Low-Voltage MDAC

Fig. 8 shows the low-voltage MDAC based on the opamp resetting scheme. Note that the conventional floating CMOS switches in the signal path are eliminated. The sampling capacitor is discharged by the resetting the opamp of the previous/driving stage into unity-gain configuration. The reference voltages is injected through a separate capacitor $C_{\rm ref}$ which is scaled down to 1/8 of the sampling capacitor C_s. There are several advantages of this downscaling. First, the effective reference voltages can also be scaled to $V_{\rm REFP} = 0.9$ V and $V_{\rm REFN} = 0$ in 0.9-V supply operation (absolute signal voltage is from 225 mV to 675 mV). This enables the use of NMOS or PMOS switches ($|V_{\rm th}| \approx 0.45$ V). It also greatly simplifies the ADC voltage reference network design since we can connect the voltage reference node to the power supply potential directly without using reference buffer or resistor ladder. As a result, the power consumption and die area can be saved. Second, the kT/C noise from $C_{\rm ref}$ is reduced because of the smaller capacitor size. Third, opamp feedback factor is increased, which not only improves opamp settling, but also reduces noise from the opamp. The drawback of this downscaling of $C_{\rm ref}$, however, is the large capacitor spread ratio (1:8), which makes it more difficult to achieve good matching in practical implementation. Fortunately, this is not an issue here because the background calibration will effectively correct the errors due to capacitor mismatches. This is a good example of how digital calibration can help achieve a good tradeoff during ultra-low-voltage circuit design process.

Because it is very difficult to implement the fully differential topology employing a traditional common-mode feedback circuit at the 0.9-V operation, a pseudodifferential MDAC architecture is used, as shown in Fig. 8. The classic common-mode error amplification/accumulation problem in pseudodifferential pipelined ADC is alleviated by adding extra cross-coupling positive feedback capacitors [3]. This makes the common-mode gain of MDAC equal to one while keeping the differential gain of two. Therefore, any common-mode error will not be amplified from stage to stage down the pipeline. While the proposed pseudodifferential MDAC alleviates difficulties for ultra-low-voltage operation, it does face an increased difficulty in common-mode noise rejection. Thus, it is important to minimize any common-mode variation to achieve good performance. Another important source of common-mode error in SC circuits is charge injection. In this implementation, dummy switches are carefully placed at critical nodes of MDAC (e.g., opamp virtual ground) to minimize charge injection.

Another important issue in this design is the control of opamp feedback factor which can vary dramatically from the amplifying phase to the resetting phase. This makes it very difficult to optimally implement opamp compensation. At the amplifying phase, feedback network is formed by the sampling and feedback capacitors. The resulting feedback factor is around 1/4 considering the parasitic capacitance at the opamp input. However, during the resetting phase, the opamp is in unity-gain configuration, where the feedback factor is equal to 1. For example, if we compensate the opamp in such a way that phase margin is about 60° at feedback factor of 1/4 during the amplification

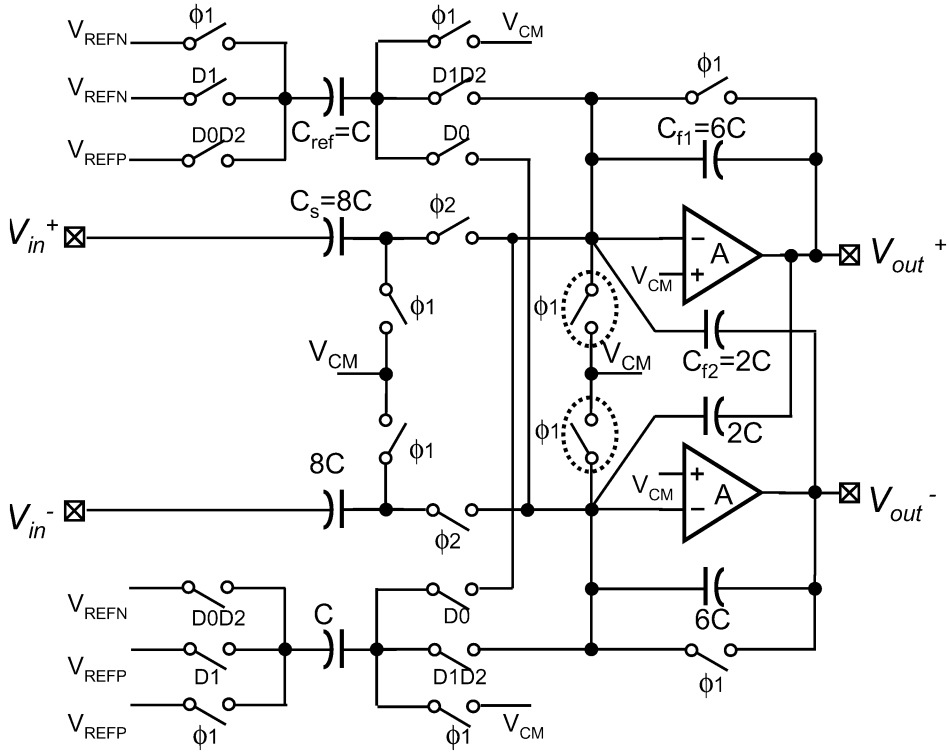

Fig. 8. Low-voltage MDAC.

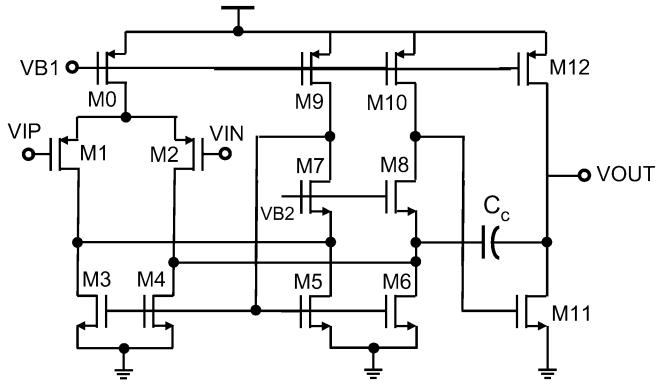

Fig. 9. Low-voltage single-ended opamp.

TABLE I
SIMULATION RESULTS OF OPAMP

Technology	0.18μm CMOS
Supply Voltage	0.9V
DC gain	65dB
Settling time	13ns
Signal Swing	0.5Vpp
Input Cap	0.2pF
Bias Current	1.5mA

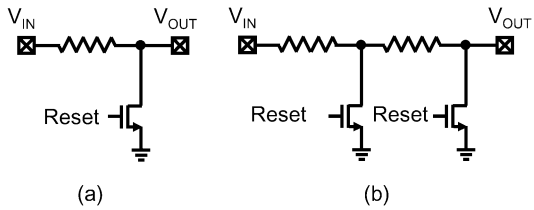

Fig. 10. Passive track-and-reset circuit MDAC.

phase, phase margin will be much smaller than 60° when feedback factor is 1 during the resetting phase. As a result, a large overshoot and ringing would be observed. This will directly impact the settling of the next stage because the sampling capacitor of the next stage is discharged by this resetting opamp. One simple solution adopted here is to place a switch between opamp input and $V_{\rm CM}$ as shown in Fig. 8. With the addition of these switches at resetting phase, a feedback network is formed by the resetting switch and the added switch from the opamp input to $V_{\rm CM}$. This gives us the control to easily optimize the settling behavior for both clock phases. As a compromise, the opamp gain drops due to resistive (MOS switches) loading during this resetting phase. Fortunately, this only creates offset to the data conversion and does not causing nonlinearity.

Fig. 9 shows the single-ended opamp design used in the MDAC. Two-stage architecture is chosen for large output swing and high dc gain under low supply voltage. The first stage is a folded-cascode gain stage suitable for low supply voltage. The PMOS input differential pair enables low input common-mode level (112.5 mV which is 1/8 of supply in our design), allowing NMOS switches to be used at the virtual ground to minimize clock feed-through and parasitic capacitance. The second stage is just a simple inverter formed by M11 and M12, which maximizes the output signal swing. The Cascode compensation scheme [24] is used in this design to achieve faster settling with lower power consumption. The simulated opamp parameters are summarized in Table I.

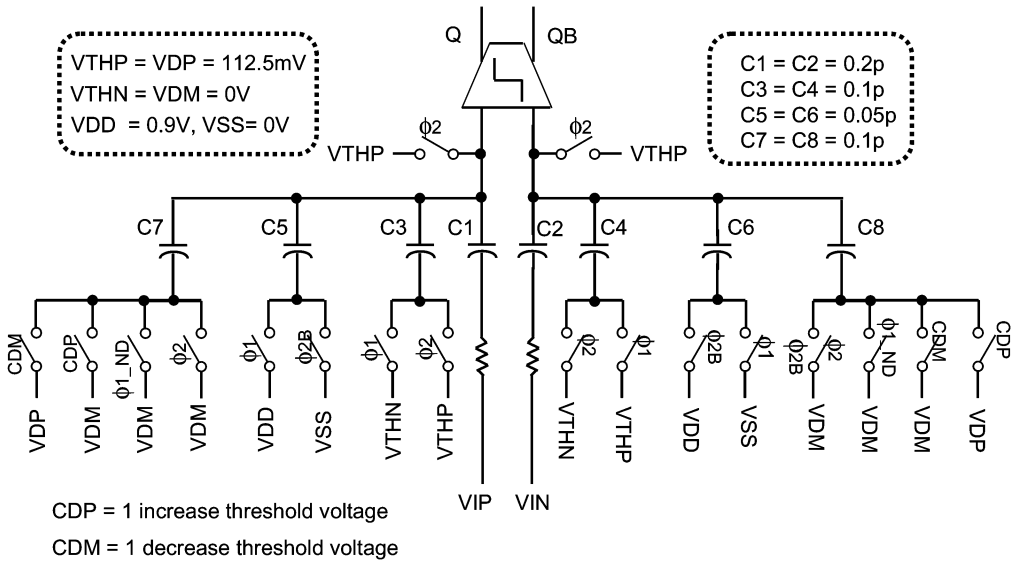

Fig. 11. Low-voltage SC comparator with dithering.

B. Low-Voltage Input Sampling Circuit

Any ADC design requires an equivalent front-end sample-and-hold function. This is a nontrivial issue in ultra-low-voltage design. A track-and-reset circuit equivalent to a floating switch is needed in this resetting opamp architecture (as in switched-opamp architecture) to realize the front-end sampling function. In [4], an active track-and-reset circuit with excellent linearity was proposed to meet this requirement. For low-frequency or moderately high-frequency applications, however, a simple passive track-and-reset circuit shown in Fig. 10(a) can be used instead. It has the advantages of low noise, ultra-low power consumption and very small die area. Observing that there is an input signal leakage during the resetting phase, since the input node is always connected to the sampling capacitor via a resistor (this leakage directly causes signal distortion due to the nonlinear on-resistance of the resetting switch), a cascaded track-and-reset passive circuit shown in Fig. 10(b) is employed in this implementation. The second R-MOSFET network further suppresses the undesired nonlinear input signal leakage. This simple passive implementation can operate down to extreme low-voltage power supply conditions, and can easily meet very high linearity requirements.

C. Low-Voltage Comparator

The injection of pseudorandom noise sequence required for calibration is implemented in the 1.5-bit sub-ADC which includes two SC comparators. One straightforward way to realize this function is to select different reference voltages for the comparators based on the value of pseudorandom sequence. However, this becomes very difficult to realize in this low-voltage design. This would require that the reference voltages of the comparator be very close to power supplies to enable the use of NMOS or PMOS switches. To solve this issue, separate capacitors are used to inject the pseudorandom noise to the comparators in this prototype design. Fig. 11 shows the resulting fully differential SC comparator design. It has several parallel signal paths to accommodate the input signal, the reference/threshold voltage, and dither signal (for calibration). The effective threshold voltage can be adjusted by $\pm(1/8)V_{\rm REF}$ depending the value of pseudorandom sequence. Note two extra capacitors $C5$ and $C6$ are added to adjust the common-mode level. This is because the common-mode level of input signal changes from opamp virtual ground $((1/8)V_{\rm DD})$ potential in the resetting phase to $((1/2)V_{\rm DD})$ in the sampling phase. The operation of $C5$ and $C6$ can cancel this variation and maintain a constant common-mode level at the input of the latched comparator core. The sizes of all capacitors are carefully scaled to reduce the spread ratio and to avoid large amplitude scaling of input signal due to the capacitive voltage division. Note that there are no floating switches in the signal paths. This is to enable the ultra-low-voltage opamp-reset-equivalent operation. Two resistors are inserted at the differential input path to reduce the kick-back noise seen by the MDAC.

The low-voltage latched comparator design is shown in Fig. 12. A simple single-stage static comparator scheme is adopted. The static current consumption is about 100 μA. The combination of PMOS input differential pair and NMOS latch has the advantages of smaller offset and faster latching. The typical latching time is about 800 ps. Two dummy PMOS transistors M1 and M2 are added to reduce the differential kick-back noise.

D. Pseudorandom Sequence Generator

Two pseudorandom sequence generator are used in this prototype algorithm ADC. Each of them is shared between two stages within each ADC channel. The on-chip pseudorandom sequence generator is shown in Fig. 13. It consists of 33 D-flip-flops and one XOR gate. The output sequence will not repeat itself until 2^{33} clock cycles. Note that the clock frequency of this block is the same as the sampling frequency which is the ADC's clock frequency divided by the number of cycles to process each input sample. The minimum allowed sizes are chosen for these

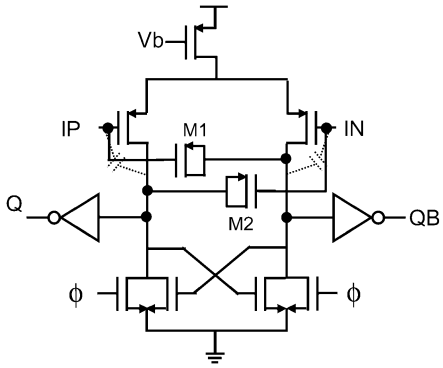

Fig. 12. Static latched comparator.

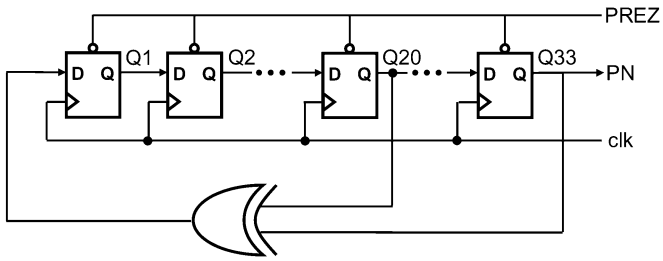

Fig. 13. Pseudorandom noise sequence generator.

flip-flops and XOR gate to minimize power consumption and digital noise.

For evaluation convenience, the radix extraction algorithm is realized off-chip in a computer. The straight-forward on-chip implementation of the radix extraction algorithm would require two multipliers, several adders, a number of registers, as well as some control logic circuitry. Among these circuits, the multiplier will be the most power- and area-hungry component. If we apply some standard optimization to the algorithm, so that the multiplier can be replaced by an adder and a look-up table, then the overhead of the digital supporting circuitry would be about 20% of the overall ADC (thanks to the ultra-low-voltage operation and fine-geometry process).We believe this overhead can be reduced further, given an in-depth study in the efficient implementation of on-chip digital calibration function.

IV. Experimental Results

The prototype ADC was fabricated in a 0.18 μm CMOS process. The die photograph is shown in Fig. 14. The active die area is 1.4 mm^2. The total power consumption is 12 mW at 0.9-V supply and 5 MHz sampling frequency (30 MHz clock frequency).

Before calibration, the measured DNL and INL are 1.1 LSB and 19 LSB at 12-bit level as shown in Fig. 15. After calibration, the DNL and INL are reduced to 0.6 LSB and 1.4 LSB, respectively, as shown in Fig. 16. Fig. 17 shows a typical measured frequency spectrum with 80 kHz input and 30 MHz clock (5 MSPS). Before calibration, the measured SFDR, SNR, and SNDR were 48 dB, 47 dB, and 44 dB, respectively. After calibration, the SFDR, SNR and SNDR are improved to 77 dB, 50 dB, and 50 dB, respectively. The measured SNR is much lower than what we expected, as the target SNR was in the

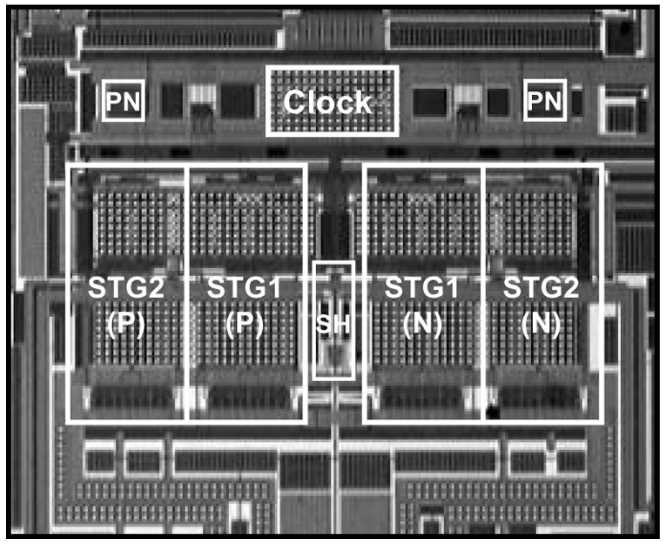

Fig. 14. Die photograph of the prototype ADC.

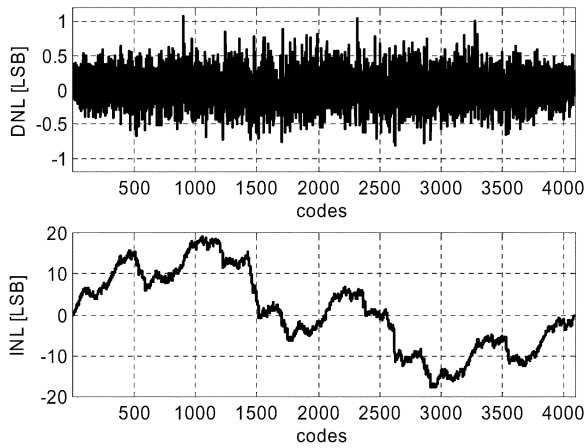

Fig. 15. DNL and INL before calibration.

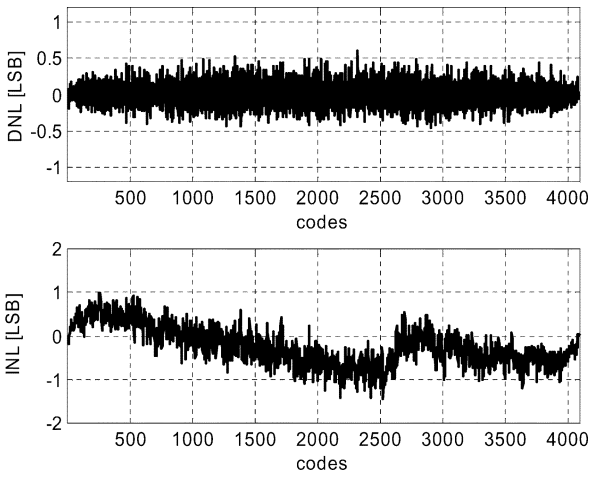

Fig. 16. DNL and INL after calibration.

mid-60s dB. Several factors may have contributed to this unexpected higher noise level. First, we underestimated the opamp noise contribution. Second, the pseudodifferential architecture does not have very good common-mode noise rejection, as well

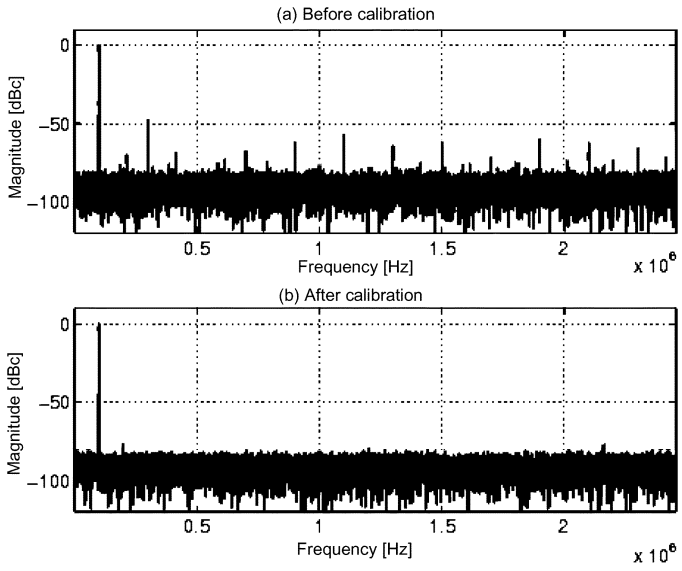

Fig. 17. Measured ADC output spectrum at 5 MSPS.

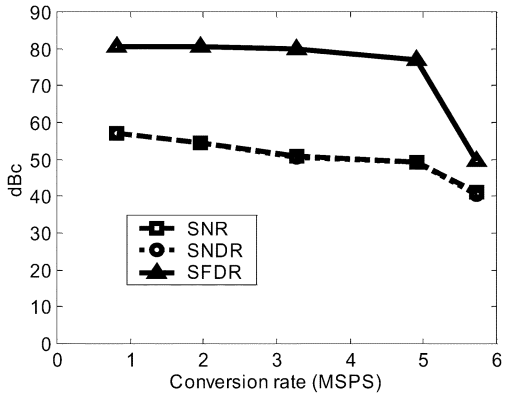

Fig. 18. Dynamic performance versus conversion rate.

as less than desired power supply noise and substrate noise rejection. Third, the input sampling process of the algorithmic ADC may have been disturbed by the switching noise of ADC stages. These issues are worthy of continued study, and we believe they can be solved with greater attention to the details of circuit design and layout.

Fig. 18 shows the dynamic performance versus conversion rate (clock frequency is six times the conversion rate). The SFDR remains better than 80 dB up to 3.2 MSPS and degrades to 77 dB at 5 MSPS. After that, the SFDR drops quickly (limited by opamp slew rate). The best SNDR/SNR of 58 dB is achieved at 1-MSPS operation. Fig. 19 shows the dynamic performance versus power supply voltage (measured at 2 MSPS). In the range of 0.9 V to 1.3 V power supply voltage, the dynamic performance is steady and slightly better at higher supply voltage because of larger headroom and signal swing. The measured ADC performance is summarized in Table II for 5 MSPS operation.

V. Conclusion

The CMOS design of a 0.9-V 5-MSPS (30 MHz clock) algorithmic ADC demonstrating 77-dB SFDR was presented. A passively cascaded track-and-reset circuit was employed

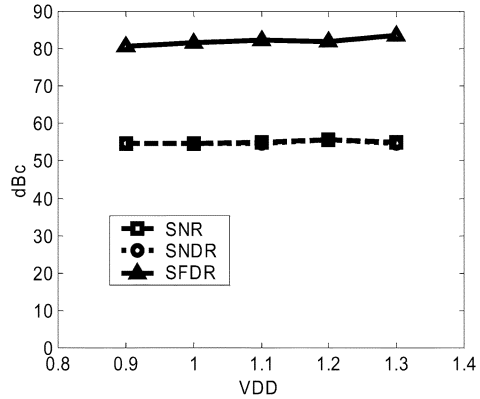

Fig. 19. Dynamic performance versus power supply voltage.

TABLE II
ADC Performance Summary

Resolution	12 bits
Conversion Rate	5MSPS
Technology	0.18μm CMOS
Supply Voltage	0.9V
Power Consumption	12mW
DNL/INL	1.1LSB/19LSB (before cal.) 0.6LSB/1.4LSB (after cal.)
SFDR/SNR/SNDR	48dB/47dB/44dB (before cal.) 77dB/50dB/50dB (after cal.)

to drive the first-stage MDAC. The overall linearity of the ADC was greatly enhanced by applying a novel background digital calibration. The minimal addition of analog hardware for calibration keeps the original ADC design essentially unchanged. An unprecedented combination of linearity and ultra-low-voltage operation for pipelined/algorithmic ADC was reported. The prototype IC was fabricated in a 0.18 μm CMOS process, and the ADC occupying 1.4 mm^2 of active die area dissipates 12 mW at 0.9-V power supply. It would be reasonable to assume that this design can be migrated to a straight pipeline ADC design operating at 30 MSPS (same 30 MHz clock) with about 30-mW power consumption (with bias current scaling down the pipeline) at 0.9 V power supply.

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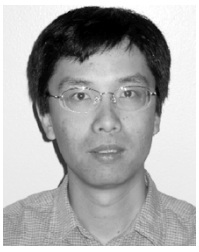
References

[1] E. Bidari *et al.*, "Low-voltage switched capacitor circuits," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 2, May 1999, pp. 49–52.
[2] M. Keskin, U. Moon, and G. Temes, "A 1-V 10 MHz clock rate 13-bit CMOS modulator using unit-gain-reset opamps," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 817–823, Jul. 2002.
[3] D. Chang, L. Wu, and U. Moon, "A 1.4-V 10-bit 25-MS/s pipelined ADC using opamp-reset switching technique," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1401–1404, Aug. 2003.
[4] D. Chang and U. Moon, "A 0.9 V 9 mW 1 MSPS digitally calibrated ADC with 75 dB SFDR," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2003, pp. 461–464.
[5] J. Wu, Y. Chang, and K. Chang, "1.2-V CMOS switched-capacitor circuits," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1996, pp. 388–389.

[6] A. Abo and P. Gray, "A 1.5-V 10-bit 14.3 MS/s CMOS pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.
[7] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349–355, Mar. 2001.
[8] J. Crols and M. Steyaert, "Switched opamp: An approach to realize full CMOS SC circuit at very low supply voltage," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936–942, Aug. 1994.
[9] J. Li and U. Moon, "Background calibration techniques for multistage pipelined ADC's with digital redundancy," *IEEE Trans. Circuits Syst. II*, vol. 50, no. 9, pp. 531–538, Sep. 2003.
[10] H. Lee, D. Hodges, and P. Gray, "A self-calibrating 15-b CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 6, pp. 813–819, Dec. 1984.
[11] Y. Lin, B. Kim, and P. Gray, "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3 μm CMOS," *IEEE J. Solid-State Circuits*, vol. SC-26, no. 4, pp. 628–636, Apr. 1991.
[12] S. Lee and B. Song, "Digital-domain calibration of multistep analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1679–1688, Dec. 1992.
[13] A. Karanicolas and H. Lee, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, Dec. 1993.
[14] S. Lee and B. Song, "Interstage gain proration technique for digital-domain multistep ADC calibration," *IEEE Trans. Circuits Syst. II*, vol. 41, no. 1, pp. 12–18, Jan. 1994.
[15] H. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE J. Solid-State Circuits*, vol. 29, no. 4, pp. 509–515, Apr. 1994.
[16] T. Shu, B. Song, and K. Bacrania, "A 13-b, 10-Msample/s ADC digitally calibrated with oversampling delta-sigma converter," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1866–1875, Dec. 1997.
[17] J. Ingino and B. Wooley, "A continuously calibrated 12-b 10-Ms/s 3.3-V A/D converter," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1920–1931, Dec. 1998.
[18] U. Moon and B. Song, "Background digital calibration techniques for pipelined ADCs," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 2, pp. 102–109, Feb. 1997.
[19] S. Kwak, B. Song, and K. Bacrania, "A 15-b, 5-Msample/s low-spurious CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1866–1875, Dec. 1997.
[20] O. Erdogan *et al.*, "A 12-b digital-background-calibrated algorithmic ADC with -90 dB THD," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1812–1820, Dec. 1999.
[21] J. Ming and S. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1489–1497, Oct. 2001.
[22] E. Siragusa and I. Galton, "Gain error correction technique for pipelined analog-to-digital converters," *Electron. Lett.*, vol. 36, pp. 617–618, Mar. 2000.
[23] B. Murmann and B. Boser, "A 12-b 75 MS/s pipelined ADC using open-loop residue amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.
[24] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 629–633, Dec. 1983.



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