Noise-Shaping Techniques Applied to Switched-Capacitor Voltage Regulators

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***Abstract*—A delta-sigma control loop for a buck-boost dc-dc converter with fractional gains is presented. This technique reduces the tones caused by the traditional pulse-frequency modulation regulation. The prototype regulator was fabricated in a 0.72-μm CMOS process and clocked at 1 MHz. It achieved suppression of tones up to 55 dB in the 0–500-kHz range. The input voltage range was 3–5 V. The output voltage ranged from 1.8 to 4 V for load currents up to 150 mA.**

***Index Terms*—Boost, buck, dc–dc converter, delta-sigma, noise shaping, voltage regulators.**

I. Introduction

SMALL electronic devices are commonly powered by batteries, which allow them to be portable. However, as battery use continues, the battery voltage drops, sometimes gradually and sometimes suddenly, depending on the type of battery and type of electronic device. Such variations in the battery voltage may have undesirable effects on the operation of the device powered by the battery. Also, the battery voltage may not be optimal for the device. Consequently, dc–dc converters are used to provide a stable output supply voltage of suitable magnitude from the battery to the electronic device.

For many years, the inductive conversion topology has been the standard way to provide a stable voltage from a battery. With the continued shrinking of handheld devices such as cell phones, PDAs, pagers and laptops, the use of inductive regulators is becoming less attractive. A compact switched-capacitor (SC) regulator is preferable to the bulky inductive regulator. SC power conversion offers reduced physical volume, less radiated EMI, as well as efficiency and cost advantages over inductive based structures. A fixed gain SC dc–dc *boost converter* may have a gain greater than or equal to one, while a fixed gain SC dc–dc *buck converter* may have a gain less than or equal to one.

In addition to increasing or decreasing the battery voltage, voltage regulation is required to maintain the battery voltage at a constant desired value. A conventional method to regulate voltage in a SC converter is to use pulse-frequency modulation (PFM) or burst-mode operation. These control techniques suffer from tones in the frequency spectrum. The tones are difficult to filter out, as their frequencies vary with load and input voltage. As a result, circuits that use the regulated voltage are susceptible to tones in the frequency region of operation. Furthermore, these tones can mix with unwanted signals outside the band of interest and modulate into the desired signal band.

In this paper, an alternate control technique using a delta-sigma loop is presented [1], which spreads the tones of the conventional SC regulator. The charge pump used to convert the input voltage acts as a D/A converter in the loop, and its output ripple is frequency shaped by the delta-sigma control loop, which also provides the pulse-frequency modulation needed for the conversion. We have applied the new control loop architecture successfully to an existing buck-boost fractional-gain regulator [2]. We could potentially inject a long pseudo-random sequence into the existing PFM loop but we then have no control over the PFM part of it. We cannot randomly make the regulator "skip" or "pump" based on a pseudo-random sequence. We would need some information of the output and input (for gain selection between the 7 different switch capacitor gains), and that will then introduce tones as it will be similar to the PFM type architecture. Using the delta-sigma control makes it possible to incorporate the gain selection into the control loop, thus providing noise shaping along with PFM control in a very small area. The measured results indicated that the tones generated by the burst-mode regulation circuitry can be reduced by as much as 55 dB by embedding the dc–dc converter in a delta-sigma loop. This verified the usefulness of the proposed scheme. It should be noted that the tones are reduced by 55 dB with respect to the noise floor of the PFM pump. The noise floor of the regulator with the delta-sigma control will be higher, because the total noise power remains the same as we do not filter the noise shaped spectrum (as done in a conventional delta-sigma modulator). The idea however is to convert the tones to white noise and prevent them from modulating into the audio band. The experimental results confirm the validity of the method [1].

II. Fractional Gain Setting Charge Pump Architecture

The block diagram of a widely used burst-mode switched-capacitor dc–dc voltage regulator [2] is shown in Fig. 1. The circuit contains two feedback loops. One of them is the PFM loop which compares the output voltage $V_{\rm out}$ with the desired output value $V_{\rm desired}$, and turns the gated clock signal *on* or *off* depending on the result of the comparison. The other loop performs gain hopping. It sets the gain G to a value that it is sufficiently large to prevent reverse current flow into the battery, but

Manuscript received August 21, 2003; revised April 6, 2004. This work was supported by the National Semiconductor Corporation.

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Digital Object Identifier 10.1109/JSSC.2004.840986

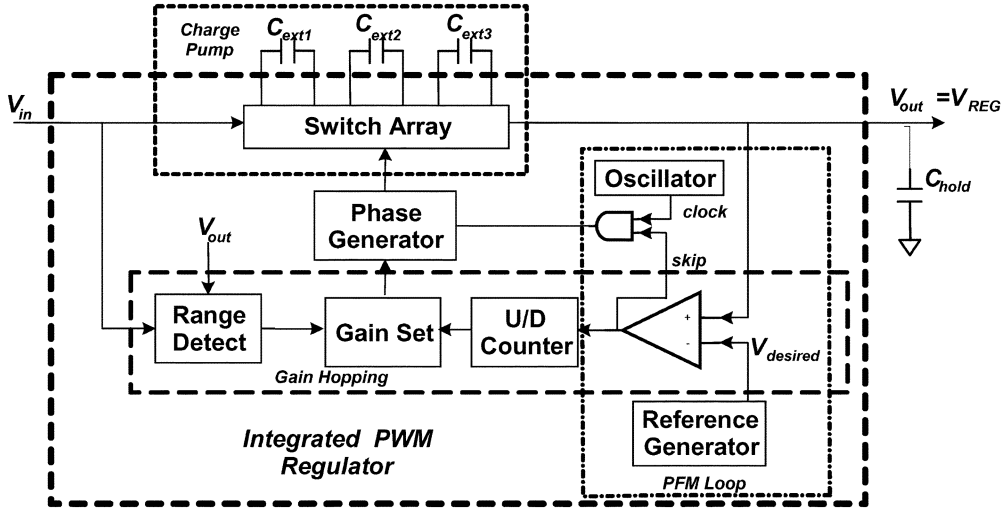

Fig. 1. Burst-mode switched-capacitor dc–dc regulator.

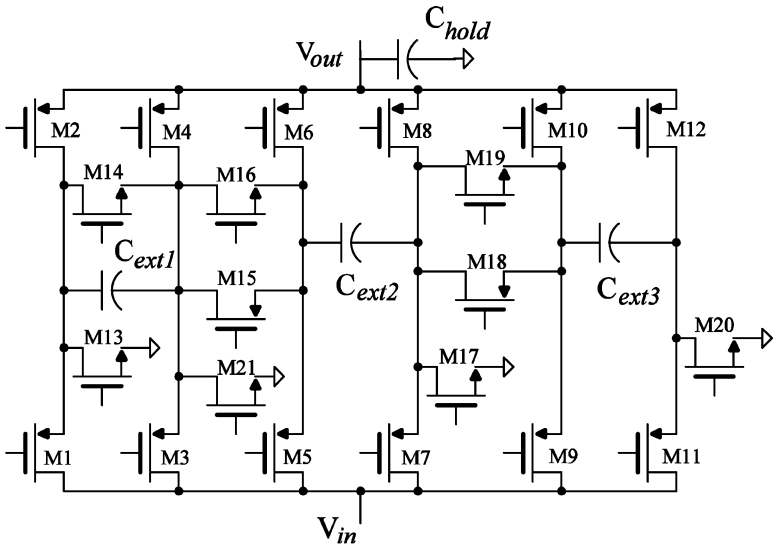

Fig. 2. Switch array with external capacitors.

not too large because then the regulator must drop the voltage by a large amount, reducing the power efficiency. The gain hopping loop requires a fractional gain setting circuit, to be discussed next.

Fractional gains can be realized by connecting external capacitors to an on-chip switch array, as shown in Fig. 2 [2]. The switch array can provide seven different gains $G = 1/2, 2/3, 3/4, 1, 4/3, 3/2$, and 2. Each gain is implemented in the two phases of a 1-MHz clock. For example, Fig. 3 shows the configuration used to implement $G = 3/2$.

To guarantee that current does not flow into the battery, we have to ensure that $G > V_{\rm REG}/V_{\rm IN}$, where $V_{\rm REG}$ is the desired output voltage, and $V_{\rm IN}$ is the unregulated battery voltage. Also, to maximize efficiency, G must be as close to $V_{\rm REG}/V_{\rm IN}$ as possible. The gain that satisfies these conditions is defined as the minimum gain $G_{\rm MIN}$.

When the pump provides the gain $G_{\rm MIN}$, the largest current that it can deliver to the load is approximately

$$I_{\max} \cong (G_{\min} V_{\rm in} - V_{\rm reg})/R_{\rm out} \quad (1)$$

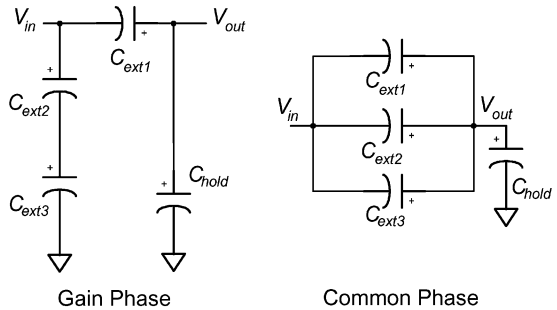

Fig. 3. Capacitor configuration for gain $= 3/2$.

where $R_{\rm OUT}$ is the equivalent output impedance of the switch array. Each gain configuration has a unique $R_{\rm OUT}$, which is a function of the switching frequency, capacitor size and the switch impedance. Selecting a gain larger than $G_{\rm MIN}$ increases $I_{\rm MAX}$. By increasing the gain only when needed, power is delivered more efficiently. The *gain-hopping* loop (Fig. 1) controls the gain based on a measure of the load current, and sets the

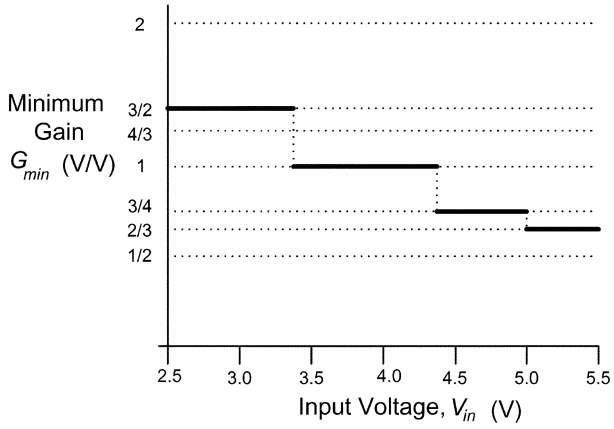

Fig. 4. $G_{\rm MIN}$ versus $V_{\rm IN}$ (for $V_{\rm REG} = 3.3$ V).

value of $G_{\rm MIN}$ as a function of $V_{\rm IN}$. Fig. 4 illustrates the minimum gain versus $V_{\rm IN}$ for $V_{\rm REG} = 3.3$ V. The *gain-hopping* loop consists of an up-down counter, gain-set block, and a comparator. The up-down counter integrates the pulse sequence at the comparator output and directs the gain-set block to increase or decrease the gain.

The PFM loop in Fig. 1 contains a voltage reference $V_{\rm desired}$, an analog comparator, and an oscillator. When $V_{\rm REG}$ is below the voltage reference, the switch array delivers current to the load. Alternately, when $V_{\rm REG}$ is above the reference, the switch array rests. By controlling the switching, the output impedance is modulated to provide the regulation. Also, for a given gain configuration, the pulse density of the comparator is proportional to $I_{\rm LOAD}$. If $I_{\rm LOAD}$ is constant, the duty cycle of the output is fixed, resulting in a highly tonal frequency spectrum.

III. Modelling the Switched-Capacitor Regulator

In order to simulate the regulator at the system level, closed-loop expressions must be found for each of the gain configurations. That helps to predict the time-domain behavior of the regulator to a first-order approximation without simulating any real circuit components. The expressions that follow are all based on the assumption that the switches have zero on-resistance $R_{\rm on}$. The output impedance of the regulator is a function of $R_{\rm on}, C_{\rm ext}$, and f (switching frequency). The assumption of $R_{\rm on}$ to be zero in the closed form expression predicts lower output impedance for the pump. This is similar to using a larger value of $C_{\rm ext}$ on the actual regulator.

A typical time-domain output of a given gain configuration $(G = 1/2)$ is shown in Fig. 5. The two phases are $\Phi 1$ (gain phase) and $\Phi 2$ (common phase). The four voltages V_h, V_m, V_{m1}, and V_l at the boundaries of the two phases are of importance. Since a constant load $I_{\rm load}$ was assumed, the values of V_h, V_m, V_{m1}, and V_l repeat after every cycle in the steady state. By applying conservation of charge, one can compute the value of the output voltage V_m sampled at the end of phase $\Phi 2$ [3]:

$$V_m = \frac{V_{\rm in}}{2} - \frac{I_{\rm load}(C_{\rm hold}+C)}{8fC(2C+C_{\rm hold})}\left[1+\frac{C_{\rm hold}+C}{3C+C_{\rm hold}}\right] - \frac{I_{\rm load}}{2f(3C+C_{\rm hold})} \quad (2)$$

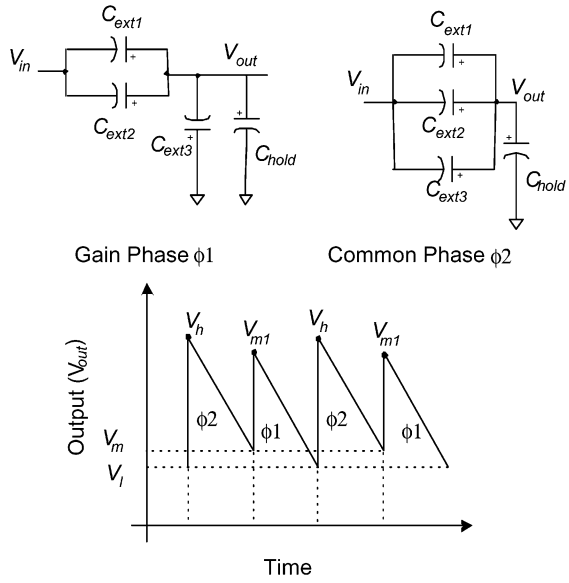

Fig. 5. Ideal time domain response for $G = 1/2$.

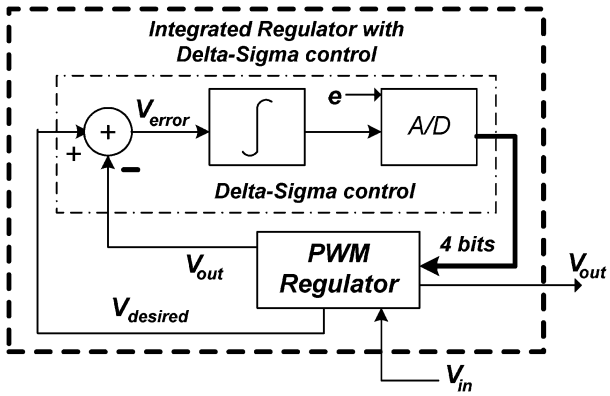

Fig. 6. Block diagram of the first-order $\Delta\Sigma$ control loop.

where $f = \text{switching frequency}$ and $\mathrm{C} = \mathrm{C}_{\rm ext1,2,3}$, as all three capacitors are nominally of equal size. Clearly, if $I_{\rm load}$ is zero, the output voltage is $V_{\rm in}/2$, as expected. The above expression was simulated in MATLAB and compared with SPICE simulations. They were found to be in agreement.

One can also compute $V_m(n)$, the output voltage at the nth sample [3] for a time-varying input voltage $V_{\rm in}(n)$:

$$V_m(n) = aV_m(n-1) + bV_{\rm in}(n) \quad (3)$$

where

$$a = \frac{(C+C_{\rm hold})^2}{(3C+C_{\rm hold})^2}$$

and

$$b = \frac{C}{(3C+C_{\rm hold})}\left[1+\frac{C_{\rm hold}+C}{3C+C_{\rm hold}}\right]. \quad (4)$$

This suggests that the charge pump can be modeled as a lossy integrator with a pole at $a < 1$ and constant gain b. It should be mentioned that this model represents the charge pump in a single gain setting and does not model the dynamic variations between the different gain settings. The key idea is to be able to simulate the regulator to a first-order approximation, and to

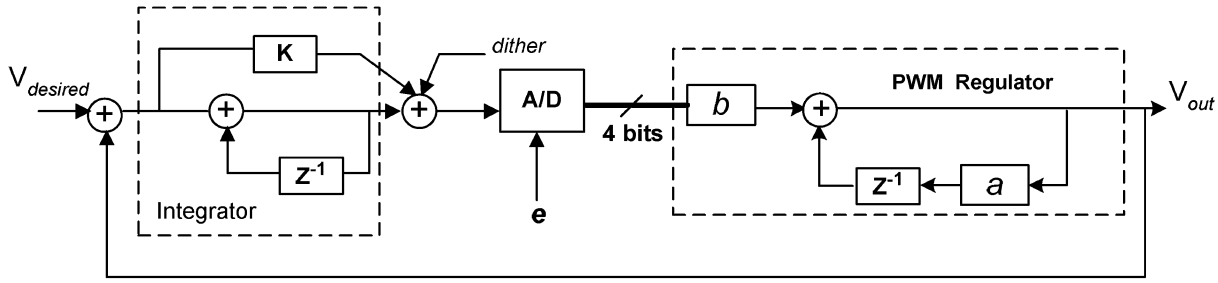

Fig. 7. Discrete time model of the regulator with the $\Delta\Sigma$ control loop.

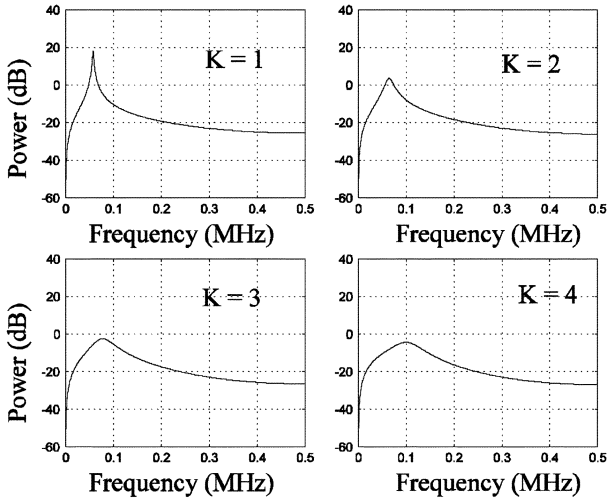

Fig. 8. Variation of the NTF with feedforward factor K.

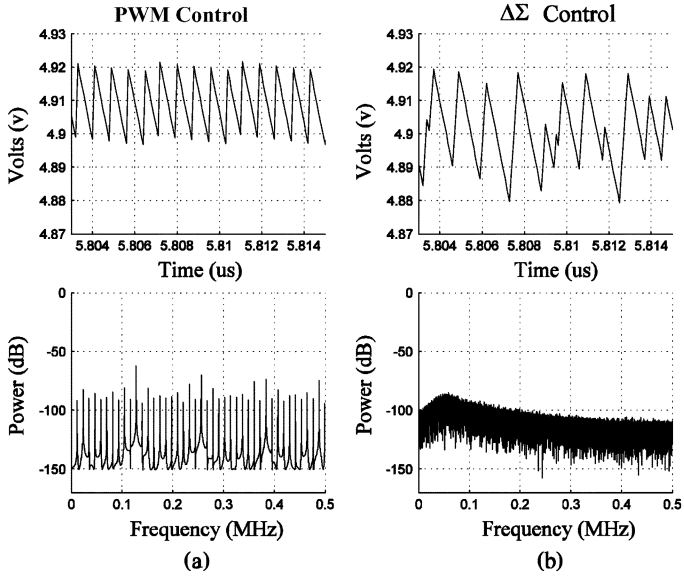

Fig. 9. Time and frequency-domain output plots for the regulator with and without the $\Delta\Sigma$ control loop.

predict the time- and frequency-domain responses without circuit-level simulation.

The efficiency of the charge pump can also be computed. The power dissipated at the output, $\mathrm{P_{out}}$, can be found, as we know V_{out} and I_{load}. To compute the power $\mathrm{P_{in}}$ supplied by the battery, we need to find the average current delivered by the input in each of the gain configurations. Then, the efficiency can be obtained from

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_{\mathrm{in}} I_{\mathrm{in}}}. \tag{5}$$

To calculate the average current I_{in} supplied by the input, we must find the charge supplied by V_{in} in every cycle. Since we know the value of V_{out} at the beginning and end of each clock phase [3], we can compute the amount of charge transferred and calculate the current supplied by V_{in} in every cycle. These computations do not take into account the nonzero switch resistance and the power dissipation in the other regulator circuits. The predicted efficiency given by the closed form expression will be close to the actual measured results. However, the closed form expression does not include the losses due to switching of parasitic capacitors associated with the big switches, nor the switching losses and I_q of the regulator. It is also inaccurate in the prediction of the efficiency when the regulator is hopping from one gain to another.

IV. Delta-Sigma Control Loop

As mentioned earlier, the burst-mode (PFM) control mechanism leads to a tonal spectrum for the output ripple, which may introduce excessive noise into the signal band of the device powered by the regulator. The tones may be converted into filtered pseudo-random noise by incorporating the complete regulator as the feedback DAC into a delta-sigma loop, as shown in Fig. 6. We assume that the quantization error $e[n]$ can be modeled as an additive white noise which is independent of the input, is uniformly distributed in $[-\Delta/2, \Delta/2]$ where Δ is the step size of the quantizer, and has a white power spectral density [4]. Then $e[n]$ can be represented as an additional input to the linearized system. The output of the modulator $\mathrm{Y}(z)$ can be expressed as

$$Y(z) = \mathrm{STF}(z)U(z) + \mathrm{NTF}(z)E(z) \tag{6}$$

where $\mathrm{STF}(z)$ is the signal transfer function, and $\mathrm{NTF}(z)$ is the noise transfer function. For the first-order $\Delta\Sigma$ modulator

$$\mathrm{STF}(z) = \left.\frac{Y(z)}{U(z)}\right|_{E(z)\equiv 0} = \frac{H(z)}{1+H(z)} \tag{7}$$

$$\mathrm{NTF}(z) = \left.\frac{Y(z)}{E(z)}\right|_{E(z)\equiv 0} = \frac{1}{1+H(z)}. \tag{8}$$

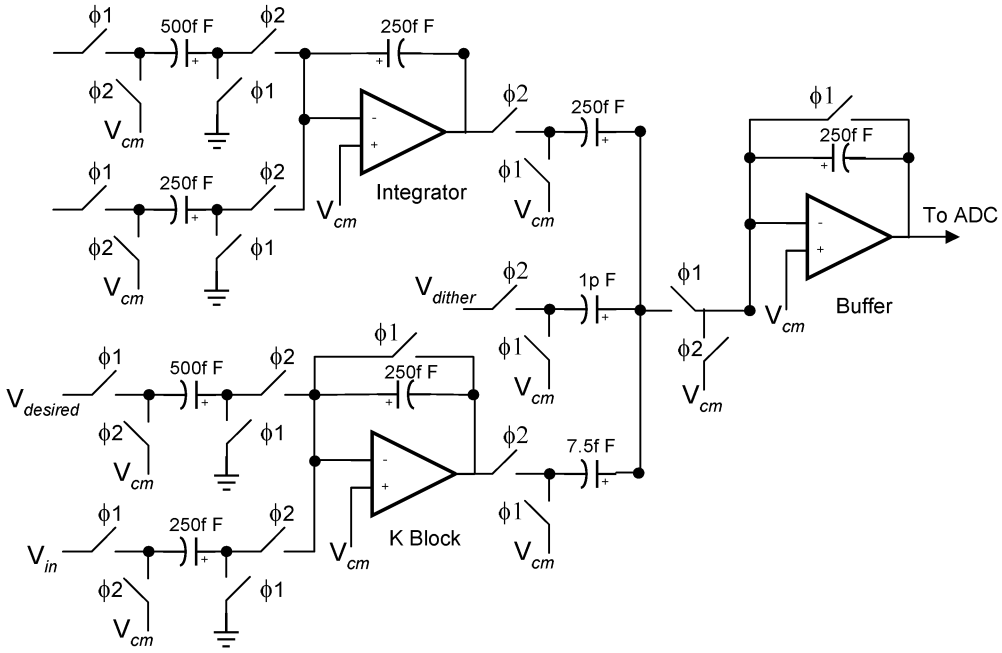

Fig. 10. Delta-sigma control implementation.

Equation (8) illustrates that if H(z) is a low-pass function with a high low-frequency gain, the quantization noise is high-pass filtered.

A. Delta-Sigma Control Loop

The simplified model of the modified regulator with a delta-sigma control loop is shown in Fig. 6. The $\Delta\Sigma$ loop provides a 3-bit word necessary for gain selection, plus the 1-bit *skip* signal for the PFM operation. The $\Delta\Sigma$ loop contains an integrator and a 4-bit analog-to-digital converter (ADC). The charge pump acts as the digital-to-analog converter (DAC) in the loop. The output of the DAC is the regulated voltage.

The error between the desired voltage and the output voltage is integrated and fed to the 4-bit ADC. As the output voltage approaches the desired voltage, the error signal decreases, reducing the input to the ADC. This causes a smaller gain to be chosen, until the minimum gain is reached. Since the $\Delta\Sigma$ control is a first-order loop, dither must be injected to avoid tone generation [5], [6].

The 3 MSBs from the A/D select one of the seven gain levels, and the LSB controls the PFM operation. Since there are seven possible gain settings, the 3 bits are sufficient to control all possible gains.

B. Discrete-Time Model of the Delta-Sigma Control Loop

Fig. 7 illustrates the discrete-time model of the $\Delta\Sigma$ control loop with the regulator. The delta-sigma loop is a first-order loop and by itself it is unconditionally stable. As mentioned earlier, the charge pump can be modeled as a lossy integrator which creates an additional pole and may make the loop unstable. In order to stabilize the loop, a feedforward path was added around

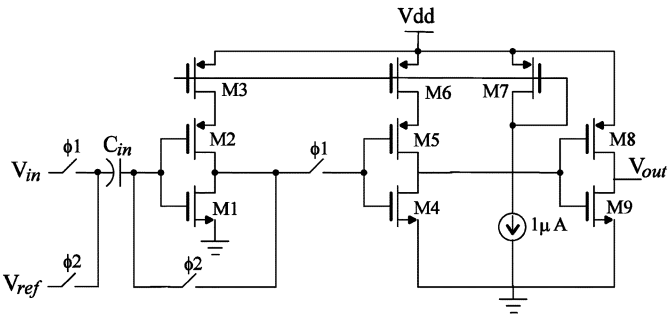

Fig. 11. Clocked CMOS comparator.

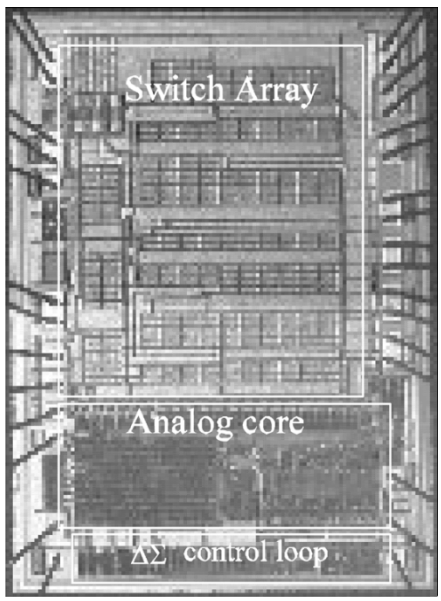

Fig. 12. Die photograph of regulator with $\Delta\Sigma$ control loop.

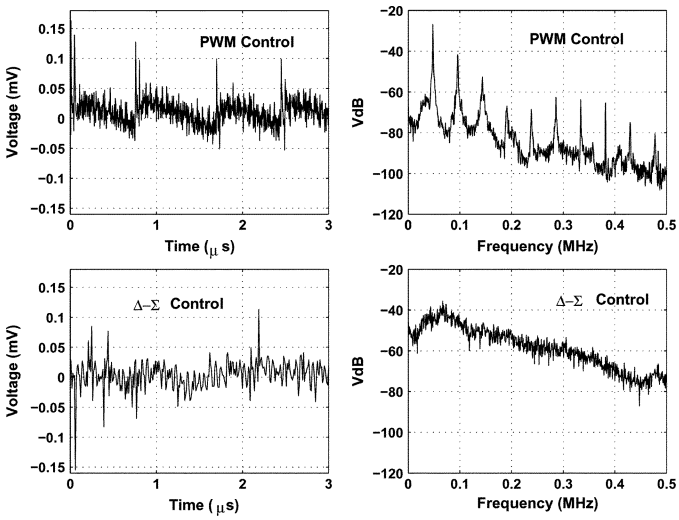

Fig. 13. Measured output ripple and output spectrum with PWM control and $\Delta\Sigma$ control for $I_{\rm load} = 50$ mA, $V_{\rm out} = 3.2$ V and $V_{\rm in} = 3.7$ V.

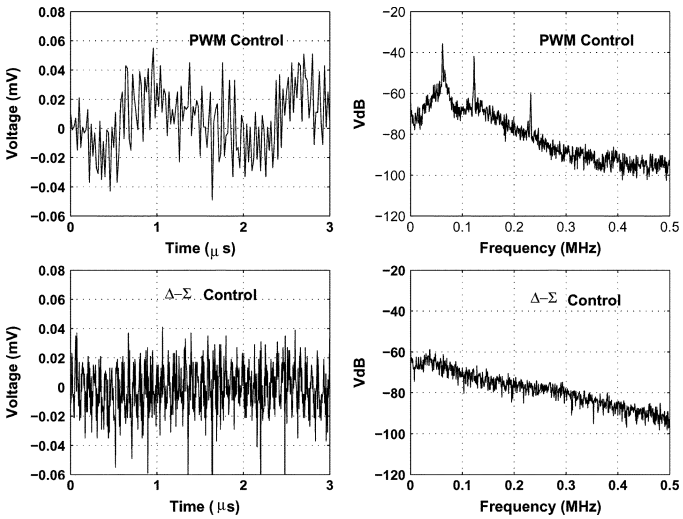

Fig. 14. Measured output ripple and output spectrum for PWM control and $\Delta\Sigma$ control loop for $I_{\rm load} = 150$ mA, $V_{\rm out} = 3.2$ V and $V_{\rm in} = 3.7$ V.

the integrator with a gain K. The NTF for the system shown in Fig. 8 is given below:

$$\mathrm{NTF}(z) = \frac{V_{\rm out}}{E} = \frac{b(1-z^{-1})}{1 - z^{-1}[1 + a - (K+1)b] + z^{-2}(a - Kb)} \quad (9)$$

where E is the quantization error of the ADC. This is valid for a specific value of the input and output voltages and load current, and assumes that the system is settled. It does not represent the dynamic behavior of the system, but gives a good estimate of the stability of the system. We see peaking in the NTF which indicates some instability in the loop when the delta-sigma control is wrapped around the regulator.

The NTF is shown in Fig. 8 for different feedforward gains. As K increases, the pole-Q reduces, making the system more stable. This can be intuitively explained as the feedforward path reduces the effect of the delay through the integrator. We have not been able to come up with a closed form expression for stability for the entire system, but MATLAB simulations indicated that adding a feedforward reduces the peaking in the NTF, and a feedforward factor (K) greater than 4 does not benefit stability. The time-domain output and the output spectrum of the regulator with and without the $\Delta\Sigma$ loop are compared in Fig. 9. Both architectures were simulated using the closed-form equations [3] (corresponding to the time-domain response of Fig. 5). For the simulation $C_{\rm hold}$ was 30 μF, while $C_{\rm ext1,2,3}$ was 0.33 μF and $V_{\rm in}$ was 5.2 V. The simulated curve matches closely the calculated NTF.

As Fig. 9 shows, $\Delta\Sigma$ control causes a slightly higher ripple. This can be attributed to the increased delay in the loop. However, the spectral properties are very much improved: instead of high-level tones, the output spectrum contains lower-level slightly colored noise, which is much less harmful in most applications.

V. Circuit Implementation

Since the $\Delta\Sigma$ loop (Fig. 6) controls only the gain selection, and is not a part of the signal path, it was kept very simple. The loop control circuitry is shown in Fig. 10. All the circuitry was single-ended since the LSB was large (150 mV). The integrator and the gain block were standard switched-capacitor stages. The unit capacitance used was 250 fF. A simple two-stage Miller-compensated operational amplifier, with an open-loop gain of 65 dB, a unity-gain frequency of 17 MHz and a phase margin of 55 degrees was used. The ADC/quantizer in the delta-sigma control loop was implemented as a conventional 4-bit flash structure [7].

A clocked CMOS comparator was used, as shown in Fig. 11. The LSB of the ADC is large, so an inverter based comparator could be used. The inverters contain current sources to limit the current flow and hence the power dissipation. A resistor ladder sets the reference voltage levels. The total resistance of the ladder is 220 kΩ. The dither circuit is a pseudo-random number generator using flip-flops and XOR gates. The voltage reference block consists of a bandgap reference, a D/A converter and an E^{2}PROM block. This generates the $V_{\rm desired}$ values ranging from 3 to 5 V. The E^{2}PROM allows post-package trimming of the bandgap voltage and $V_{\rm REG}$ adjustments through the DAC.

VI. Experimental Results

A prototype regulator incorporating the delta-sigma control loop was implemented in a 0.72-μm CMOS technology. The die photo is shown in Fig. 12. The active die area is 2.45×3.1 mm^2. The area of the control loop is 2.45 mm $\times$ 0.4 mm. The fabricated chip was tested through the input range of 3–5 V for several loads and output voltages. Typical measured output ripple and spectrum curves for load currents of 150 and 50 mA, an output voltage 4.7 V, and input voltage 3.4 V are shown in Figs. 13 and 14. The measurement bandwidth was 500 kHz. We can see that the PFM control has larger noise spikes at lighter loads and lesser spikes at heavier loads. This can be attributed to the fact that the PFM control "skips" less at higher loads. For

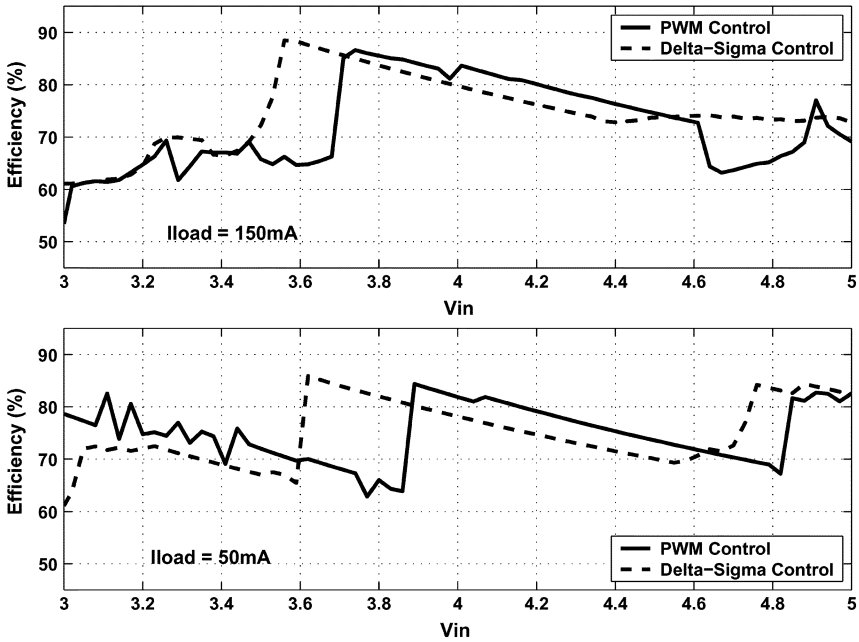

Fig. 15. Measured efficiencies for PWM control and Delta-Sigma control for $V_{\rm out} = 3.2$ V and $V_{\rm in} = 3.7$ V.

this reason the noise floor of the regulator with delta-sigma control is higher in the light loads then at heavier loads (as the total noise is not removed).

The efficiencies of the PFM and $\Delta\Sigma$ architectures are plotted in Fig. 15. With the delta-sigma control loop the efficiency curves are smoother than with the PFM control loop. The $\Delta\Sigma$ control loop selects a lower gain faster than a traditional PFM control loop. However, once the minimum gain has been chosen, the efficiencies are comparable for the two architectures.

VII. Conclusion

A pulse-frequency-modulation voltage regulator with a $\Delta\Sigma$ control loop was designed and fabricated. The test results indicate that the suppression of noise tones is possible using this technique. The additional delay through the loop increased the ripple and caused slightly poorer regulation, but gave much better spectral behavior.

Acknowledgment

The authors would like to thank the following people for their technical help and support: M. Fraley, R. Batten, B. Chatterjee, M. Keskin, J. Silva, J. Parry, T. Glad, S. Close, P. Wong, and R. Perigny.

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Dr. Temes was an Associate Editor of the *Journal of the Franklin Institute*, Editor of the IEEE TRANSACTIONS ON CIRCUIT THEORY, and Vice President of the IEEE Circuits and Systems Society. In 1968 and in 1981, he was co-winner of the Darlington Award of the IEEE Circuits and Systems Society. In 1981, he received the Outstanding Engineer Merit Award of the Institute for the Advancement of Engineering. In 1982, he won the Western Electric Fund Award of the American Society for Engineering Education, and in 1984 received the Centennial Medal of the IEEE. He received the Andrew Chi Prize Award of the IEEE Instrumentation and Measurement Society in 1985, the Education Award of the IEEE Circuits and Systems Society in 1987, and the Technical Achievement Award of the same Society in 1989. He is the recipient of the 1998 IEEE Graduate Teaching Award and the IEEE Millennium Medal, as well as the IEEE CAS Golden Jubilee Medal in 2000.