A 0.8-V Accurately Tuned Linear Continuous-Time Filter

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***Abstract*—An accurately tuned low-voltage linear continuous-time filter is presented in this paper. Accurate tuning is achieved using time-constant matched master–slave tuning combined with power-up mismatch calibration. A low-pass biquad designed for a corner frequency of 115 kHz achieves better than −80-dB total harmonic distortion with a 250-mV_{PP} 10-kHz input signal. The prototype implemented in 0.18-μm CMOS process occupies an area of 0.4 mm^2 and dissipates 4.6 mW (2.6 mW for the filter and 2 mW for tuning) of power.**

***Index Terms*—Continuous-time filter, linear, low-voltage, master–slave tuning, power-up mismatch calibration, R-MOSFET-C.**

I. Introduction

ADVANCES in CMOS technology have led to aggressive scaling of transistors, thus enabling integration of all of the system functions on the same chip. Most of the signal processing required to implement these functions is performed in the digital domain. However, since the real world is inherently analog in nature, interface circuits such as analog filters and data converters are of paramount importance for the proper functioning of the overall system. Both feature size and supply scaling, primarily guided by the performance improvements in digital circuits, have made the design of analog interface circuits very challenging. In this paper, we focus on the design of one such interface circuit, namely the continuous-time filter under very low supply voltage constraints.

The need for filtering arises very often in many applications such as telecommunication circuits. These filters are mainly implemented either by a switched-capacitor (SC) circuit or a continuous-time (CT) circuit. The corner frequency in an SC filter is set by capacitor ratios and can therefore provide a very accurate cutoff frequency [1] but suffer from several drawbacks. First, due to their inherent sampled nature, input anti-aliasing and output smoothing filters are required. Second, circuit nonidealities such as clock feedthrough and charge injection degrade the linearity of the filter. Above all, they suffer from limited headroom at low supply voltages due to the floating switch requirement [2]. CT filters offer an attractive alternative for the design of low-voltage wide-dynamic-range filters without requiring additional anti-aliasing and smoothing filters. One of the most critical issues in the design of practical CT filters is the corner frequency variation due to variations in process, voltage, and temperature (PVT). The corner frequency of a CT filter is set by the absolute value of the *RC* time constant. However, both resistor and capacitor values can vary by more than 25% in modern-day CMOS technologies. This results in a prohibitively wide variation of the corner frequency of the filter, thus mandating component trimming or on-chip automatic tuning [3] to correct for capacitor and resistor variations. However, the implementation of the existing automatic tuning methods under a low supply voltage poses a formidable design challenge. In this paper, we focus on overcoming the corner frequency variation and low-voltage issues in CT filters. We propose a tuning technique to accurately set the corner frequency while operating with high linearity at a sub-1-V supply voltage. The paper is organized as follows. Section II briefly describes various tuning methods and highlights the basic mismatch problem in one of the widely used tuning techniques. Low-voltage CT filter design issues are also summarized. The proposed tuning technique to compensate for corner frequency variation is presented in Section III. Circuit design of the complete system is presented in Section IV, and Section V presents experimental results of the fabricated chip.

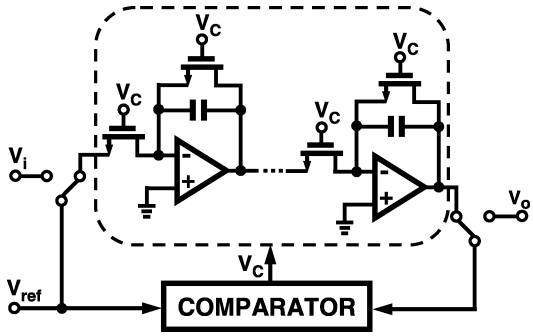

Fig. 1. Direct frequency tuning method.

II. Tuning CT Filters

Many tuning techniques have been proposed to compensate for the corner frequency variation [3]–[10]. These techniques can be broadly classified into two categories—direct tuning and indirect tuning. As depicted in Fig. 1, direct tuning is performed by comparing the filter's output to a known reference input and correcting for the corner frequency error typically by adjusting a tunable element in the filter. For example, a fixed resistor in an active *RC* filter is replaced with a MOS transistor which acts as a tunable voltage-controlled resistor. This method requires disrupting the normal filter operation during the tuning process and is therefore also referred to as the foreground method. Due to the

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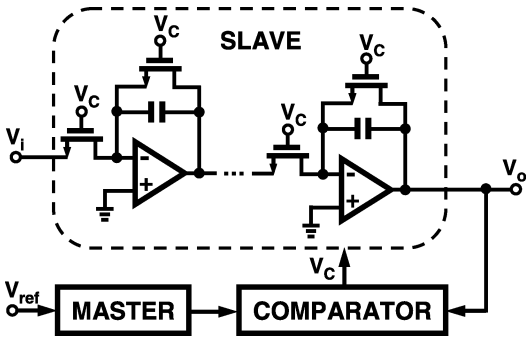

Fig. 2. Indirect frequency tuning method.

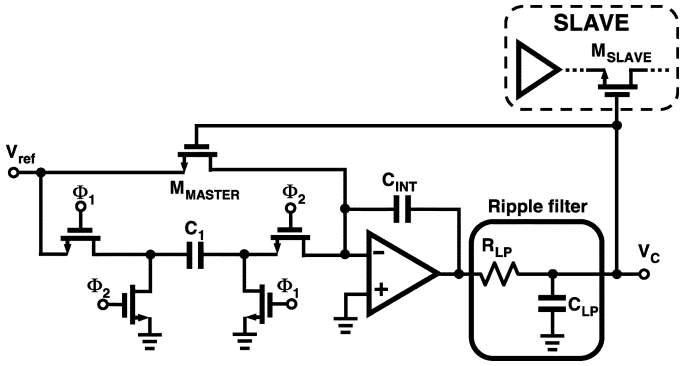

Fig. 3. Master–slave tuning circuitry.

direct measurement of the corner frequency error, this technique has the benefit of extremely accurate tuning. However, since the tuning is only performed once on power-up, component variations due to temperature and aging leads to change in *RC* time constant (corner frequency). The readjustment of the circuit parameters to correct for time-dependent variations requires interrupting the filter operation.

As opposed to direct tuning, in indirect tuning, the corner frequency error is measured indirectly without disrupting the normal filter operation and, therefore, tuning can be performed in the background. Of the existing indirect tuning methods, the master–slave tuning technique is the most popular one. As shown in Fig. 2, the corner frequency of the slave filter is set by the master filter (which models the slave) whose corner frequency in turn is typically set by a PVT invariant element. Fig. 3 depicts a well-known master–slave tuning scheme [4] in which an SC resistor clocked at a frequency $F_{\rm CK}$ is used as the reference element. The time constants of the SC resistor and the filter resistor branches are equal to $C_{\rm INT}/(F_{\rm CK}C_1)$ and $R_{\rm MASTER}C_{\rm INT}$, respectively. The negative feedback adjusts the gate voltage of the MOS resistor $\boldsymbol{M}_{\rm MASTER}$ by integrating the error current generated due to the mismatch between the time constants of the two branches. Due to the large dc loop gain, the error current approaches zero at steady state, thus resulting in matched time constants. Note that the time constant of the SC branch is independent of PVT, since the clock frequency $F_{\rm CK}$ can be defined and the capacitor ratio $(C_1/C_{\rm INT})$ can be designed with better than 0.1% matching. This approach suffers from two drawbacks. First, the PVT variations in the slave filter are annulled by the PVT-invariant master filter only in the ideal case. In practice, however, the mismatch between

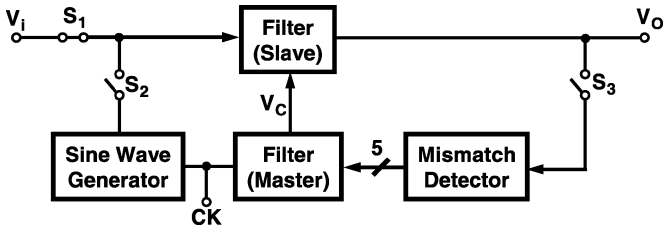

Fig. 4. Combined master–slave and power-up direct frequency tuning.

the master and the slave limits the accuracy of this tuning scheme to about 5% [7]. Second, for low-voltage operation, the tuning range is severely limited by the threshold voltage of the $M_{\rm MASTER}$ (and $M_{\rm SLAVE}$) transistor. For the MOSFET to be operational $V_{\rm GSMIN} > V_{\rm TH}$ and to prevent gate oxide stress-related reliability issues $V_{\rm GSMAX} < V_{\rm DD}$ [11], thus V_G can at most be varied between $V_{\rm TH}$ and $V_{\rm DD}$ which translates to a very small tuning range. In the next section, we present an alternate tuning scheme to circumvent these two issues.

Linearity of CT filters is an important requirement in many modern-day applications. The most popular tunable filters are the MOSFET-C filters because of their simplicity. However, the overall linearity of these filters is typically limited to 40–60 dB by the nonlinearity of the MOSFET itself. The linearity of MOSFET-C filters can be improved by using the R-MOSFET-C technique, obtained by replacing a MOSFET with an R-MOSFET combination [7]. Due to the higher linearity advantage, we focus on tuning the R-MOSFET-C structure.

III. Proposed Tuning Scheme

The system-level block diagram of the proposed tuning scheme is shown in Fig. 4. This scheme combines the advantages of both the direct and indirect tuning methods described earlier. The master reference tunes the slave filter continuously to the required frequency, while the power-up direct tuning cancels the master–slave mismatch, thus resulting in a very accurately tuned filter. The overall tuning is performed as follows. On power-up, switches S_1 and S_2 are turned ON while S_3 is turned OFF. A digitally synthesized sine wave of desired frequency (typically the $-$3-dB frequency of the filter) is applied to the slave filter. Master–slave mismatch manifests itself as the inaccurate $-$3-dB output amplitude of the filter and is therefore used to detect and correct for the mismatch. The filter is switched back to its normal mode of operation after the mismatch is suppressed within the required accuracy by turning off S_2 and S_3 and turning on S_1. The circuit implementation details are presented in the next section.

As mentioned earlier, the distortion in MOSFET-C filters is dominated by the MOSFET nonlinearity. A technique to circumvent this problem is the well-known R-MOSFET-C approach in which the nonlinear MOSFET is split into a linear polysilicon resistor and the MOSFET, thus reducing the contribution of the MOSFET nonlinearity. An SC tuning scheme in conjunction with linearity enhanced R-MOSFET-C filter adopted in this work is shown in Fig. 5. The tuning loop sets the control voltage (V_c) so that the sum of the M_1 resistance and R matches the reference SC resistance $1/(F_{\rm CK}C_1)$. Even though

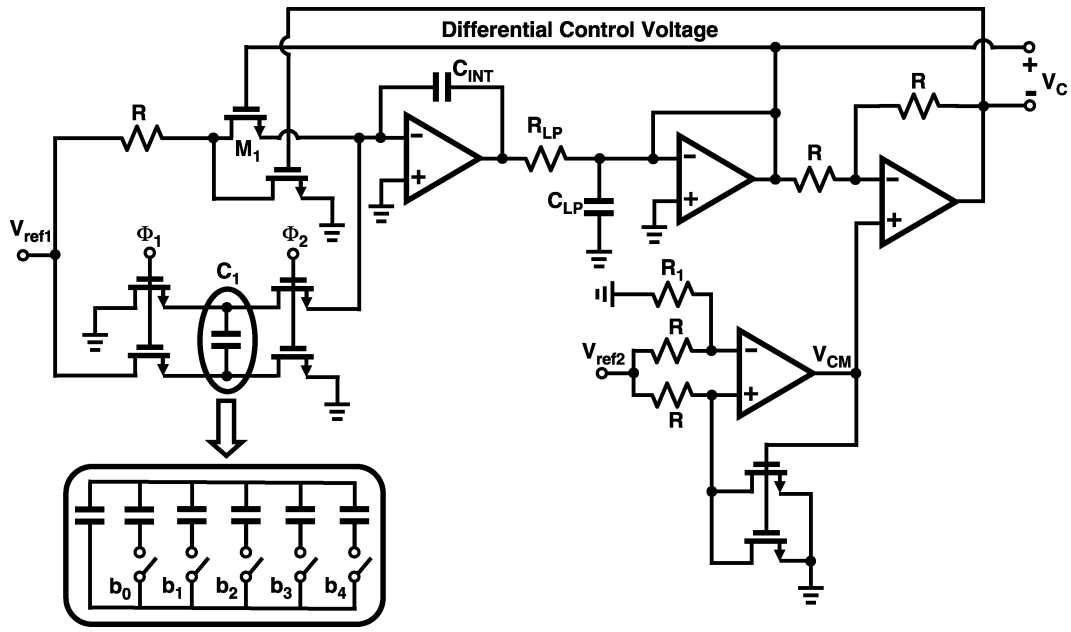

Fig. 5. Digitally programmable master–slave tuning circuitry.

it has been shown in [7] that this scheme tracks PVT variations, the absolute accuracy of the corner frequency is limited by the master–slave matching. In this work, capacitor C_1 is self-calibrated during power-up to correct for this mismatch *directly*. In order to perform this calibration, capacitor C_1 is replaced by a digitally controlled bank of capacitors, as shown in Fig. 5, and the calibration is done as follows. A digitally synthesized sine wave is applied to the filter and the peak filter output ($-$3-dB value) is determined and compared with the reference $-$3-dB peak value. The output of this comparison determines whether the mismatch is positive or negative, thereby enabling the mismatch correction block to increase or decrease the capacitance value in the SC resistor. This system is designed to accommodate for $\pm 10\%$ mismatch between the master and the slave. Once the mismatch minimization is performed, the control word is set such that the effective capacitance of the reference switched capacitor is adjusted to accommodate for the master–slave mismatch.

The general problem of limited tuning range in CT filters is further exacerbated by the low supply voltage. This problem can be circumvented either by using low $V_{\rm TH}$ devices or thick oxide devices. Thick oxide devices are readily available in most submicron technologies allowing $V_{\rm GS}$ to exceed $V_{\rm DD}$. Since these transistors are used as resistors, using thick oxide devices does not levy any speed penalty on the overall filter.

IV. Prototype Implementation

Shown in Fig. 6 is the implemented R-MOSFET-C low-pass Butterworth biquad with a corner frequency of 115 kHz that is capable of operating with less than a 1-V power supply. Time-constant matching master–slave tuning, with digitally trimmed capacitors for power-up mismatch calibration shown in Fig. 5, is employed for frequency tuning. Furthermore, the nonlinear MOSFET is placed inside a feedback loop, suppressing the distortion by the loop gain. Since the proof-of-concept prototype

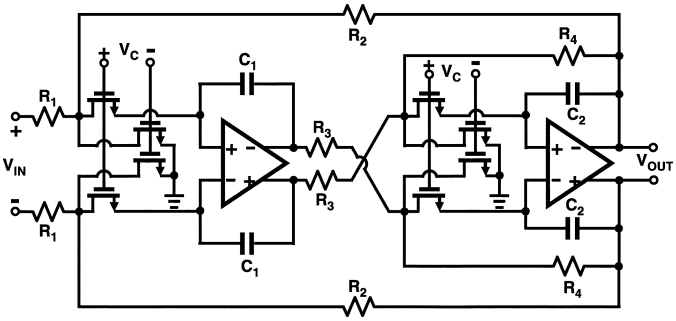

Fig. 6. Low-pass Butterworth biquad.

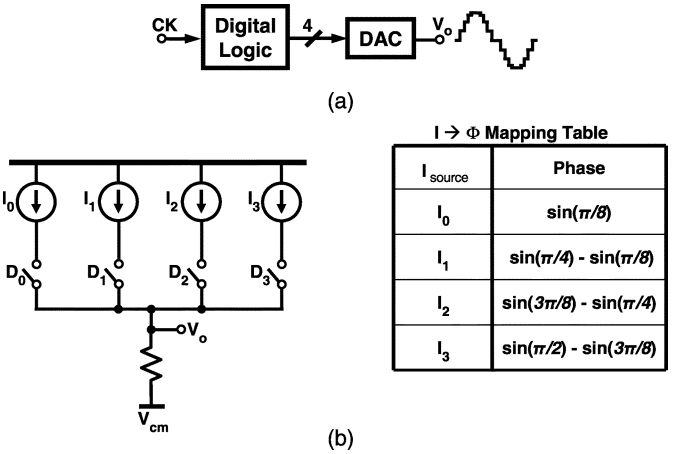

Fig. 7. Digital synthesis of a sine wave. (a) Block diagram. (b) Current-mode DAC and I-to-Φ mapping table.

is designed in a 1.8-V process, the tuning circuit uses a 1.8-V supply to accommodate a wide tuning range. However, as mentioned earlier, thick oxide devices can be used in true sub-1-V processes to prevent gate oxide stress. A high-gain two-stage miller compensated operational amplifier is used in the filter. The opamp employs a folded cascode first stage for low input

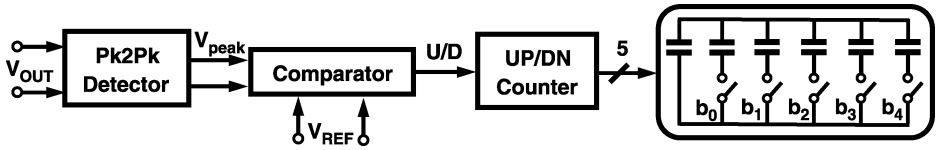

Fig. 8. Mismatch detection and correction scheme.

common-mode and high gain while the common-source second stage enables wide output swing. The simulated opamp gain is greater than 80 dB, thus providing excellent suppression of the MOSFET nonlinearity. We will briefly describe various building blocks required to implement the frequency tuning circuitry.

A. Sine-Wave Generation

The sine wave required to perform master–slave mismatch minimization is generated using a simple digital synthesis scheme shown in Fig. 7(a). The sine wave is synthesized using a digital state machine and a *nonlinear* digital-to-analog converter (DAC). The state machine generates the control word D[3:0], and the current-mode DAC converts the digital word to the corresponding analog value. The current sources in the DAC are scaled nonlinearly to accommodate the nonuniform step size required to generate the sine wave without indulging in a large number of current sources. The 4-element DAC and the current-to-phase mapping table is shown in Fig. 7(b). The generated sine wave is then applied to the filter and the master–slave mismatch is detected and corrected as described below.

B. Mismatch Detection and Correction

The mismatch detection and correction scheme is shown in Fig. 8 and is performed as follows. The peak filter output is detected by a peak detector and is compared with the reference peak voltage. The error signal indicates the mismatch between the master and the slave. The 1-b error signal (U/D) representing the mismatch is integrated by the counter and is then used to drive the capacitor bank in the SC resistor. The operation of the peak detector shown in Fig. 9 is as follows. The output capacitors are charged to V_o when the comparator determines if $V_o > V_{\rm peak}$. As long as the input remains less than $V_{\rm peak}$, the comparator's output is low and the transmission gate (TG) is off. As soon as the input goes above $V_{\rm peak}$, the TG turns back on and the new peak voltage is stored on the capacitor. The hold capacitor is reset periodically to enable the circuit to detect a new peak each cycle. This is very critical because, when the control word of the switched capacitor resistor is updated, the filter output changes and the peak detector should be able to provide the comparator with the updated peak value. A differential difference comparator shown in Fig. 10 compares the peak-to-peak values of the output ($V^+_{\rm peak} - V^-_{\rm peak}$) and the reference ($V^+_{\rm ref} - V^-_{\rm ref}$), and provides the 1-b error signal.

Since accurate tuning is achieved by running both the indirect and direct tuning loops simultaneously, it is of prime importance to guarantee that these two loops do not interact, resulting in a potentially unstable system. Stability can be guaranteed by choosing appropriate bandwidths of the two loops. For example, the mismatch minimization loop (digital control word) should be run such that the background tuning loop settles before the next update occurs. In other words, the mismatch minimization loop (digital control) should be slower than the background (continuous) tuning loop.

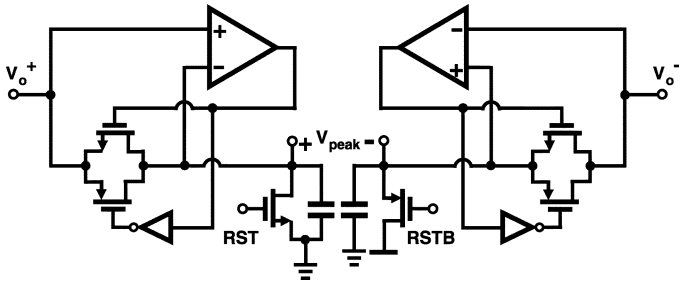

Fig. 9. Peak detector.

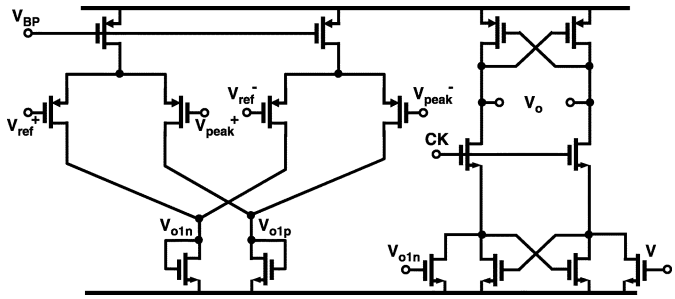

Fig. 10. Differential difference comparator.

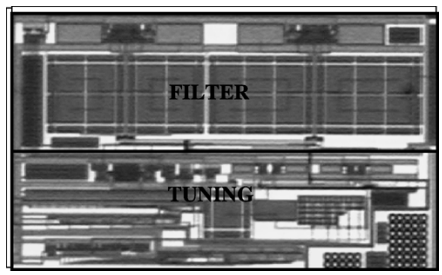

Fig. 11. Die photograph.

V. Experimental Results

A 115-kHz corner frequency second-order low-pass filter along with the proposed tuning scheme was implemented in 0.18-μm CMOS technology. A die photograph of the prototype is shown in Fig. 11. Shown in Fig. 12 is the measured output spectrum with a 10-kHz 250-m$V_{\rm pp}$ input signal for the filter operating with a 0.8-V power supply. The measured signal-to-noise ratio (SNR) is 56 dB and the total harmonic distortion (THD) is better than -80 dB. The overall SNR is lower than expected mainly due to the unaccounted flicker ($1/f$) noise of the opamp, which is reinforced by the -10-dB/dec

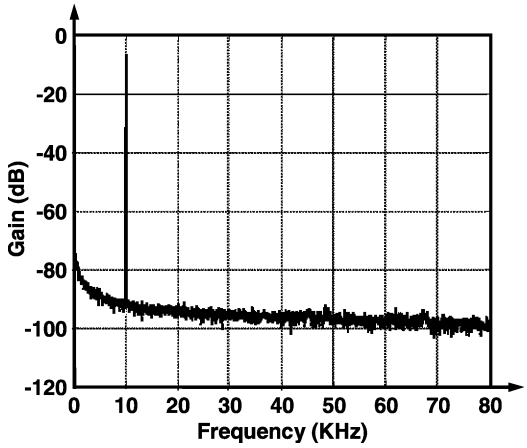

Fig. 12. Measured output spectrum with a 10-kHz 250-mV_{pp} input signal.

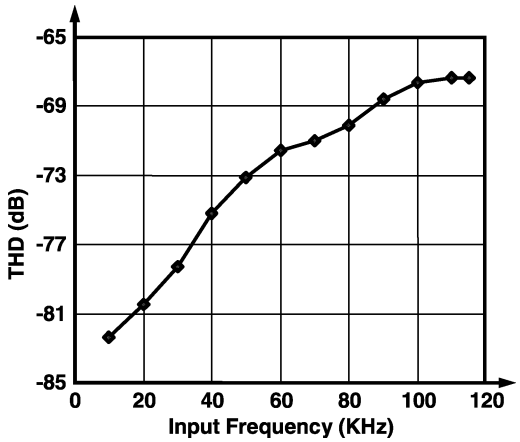

Fig. 13. THD versus input frequency.

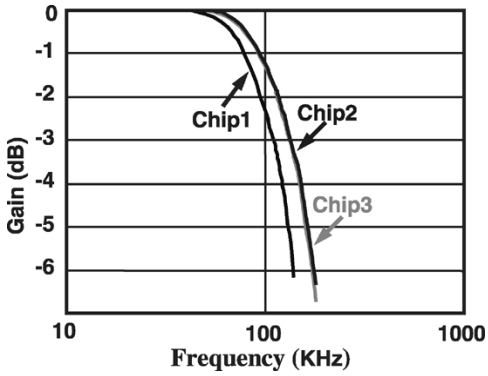

Fig. 14. Frequency responses of three chips with power-up mismatch calibration OFF. $f_{-3\,\mathrm{dB1}} = 106$ kHz, $f_{-3\,\mathrm{dB2}} = 129$ KHz, $f_{-3\,\mathrm{dB3}} = 130$ kHz.

slope of the noise floor at lower frequencies. The measured SNR excluding the flicker noise is about 84 dB. Fig. 13 shows THD for different input frequencies. The THD degradation at high frequencies is mainly due to the fact that the loop gain decreases as the bandwidth of the filter is approached, which results in less suppression of the nonlinearities for the MOSFET resistors used in the filter.

Figs. 14 and 15 show the measured frequency response of three chips with the power-up mismatch minimization scheme

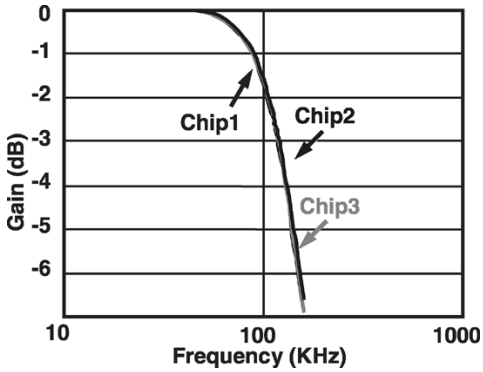

Fig. 15. Frequency responses of three chips with power-up mismatch calibration ON. $f_{-3\,\mathrm{dB1}} = 117$ kHz, $f_{-3\,\mathrm{dB2}} = 119$ kHz, $f_{-3\,\mathrm{dB3}} = 120$ kHz.

turned off and turned on, respectively. It is clear that the filter is tuned to an accurate corner frequency (115 kHz) when the power-up mismatch minimization scheme is on. A finite error in the corner frequency still exists after the mismatch minimization is performed due to the offsets of the comparators used in the system. Offset cancellation can be performed on the comparators to achieve higher accuracy in the corner frequency of the filter.

VI. Conclusion

A foreground tuning technique used at power-up in conjunction with a master–slave-based background tuning scheme is presented to track PVT variations and to minimize inherent mismatches between the master and slave filter. Challenges encountered in the design of truly low-voltage filters are discussed and techniques to improve linearity are presented. A 115-kHz low-pass second-order Butterworth filter implemented in 0.18-μm CMOS technology achieves a total harmonic distortion of -80 dB with a 10-kHz 250-mV_{pp} input signal at a supply voltage of 0.8 V. Measured results indicate good tuning accuracy in the corner frequency when both direct and indirect tuning schemes are employed.

Acknowledgment

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