# The Effect Of Power Supply Noise On Ring Oscillator Phase Noise

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Abstract—Low phase noise monolithic oscillators are in high demand in this age of wireless communications. Although LC oscillators generally have better phase noise performance, there is motivation to design ring oscillators with comparable phase noise compared to LC oscillators. The advantages of ring oscillators include significantly less die area and generally wider tuning range. Ring oscillator phase noise analysis and simulation, however, often ignore power supply noise which is a major and possibly dominant contributor of phase noise. This paper presents a method of determining a given oscillator's sensitivity to *both* intrinsic and power supply noise sources and provides a means for comparing different oscillator architectures based on this information.

### I. INTRODUCTION

Ring oscillators have several advantages over LC oscillators that make them desirable; namely, smaller die area and generally wider tuning range. On the other hand, LC oscillators generally have better phase noise performance. In order to realize high performance oscillators in highly integrated systems for which die area is at a premium, circuit designers must find a way to either reduce inductor size or reduce ring oscillator phase noise. This paper is intended to help circuit designers with the latter pursuit by showing why *both* intrinsic and power supply noise must be considered when designing a ring oscillator. Previous work on power supply noise in oscillators [1] has represented random noise as deterministic sinusoids and has relied on quasi-static assumptions. Such simulations are incapable of quantitatively comparing the contributions of power supply noise and intrinsic noise.

Section II gives a review of ring oscillators and classifies them into two broad categories based on the type of delay cell used in the oscillator. The advantages and disadvantages of each type of delay cell are explained. Section III discusses the use of available simulation tools to measure the effect of power supply noise on phase noise. Example simulations were run using the SpectreRF phase noise simulator and models for a 0.18  $\mu$ m process. The resulting plots are shown and discussed in Section IV. Conclusions are drawn in Section V.

## II. BASIC DELAY CELLS

This paper will compare two types of ring oscillators: those using traditional differential pair gain stages with resistive loads as delay cells and those using full swing inverters as delay cells. Before we are able to make comparisons, however, we must have practical, transistor-level implementations of each class of oscillator. We will use the popular Maneatis delay



Fig. 1. Maneatis partial-swing delay cell.

cell [2] to represent the partial-swing class and the Lee/Kim delay cell [3] to represent the full-swing class. These delay cells are shown in Fig. 1 and Fig. 2, respectively. The resistive load in the Maneatis cell is implemented with two transistors providing symmetric I-V characteristics which approximate differential resistor matching. The inverter in the Lee/Kim cell is implemented as a pseudo-differential positive feedback latch. Since the former is designed using partial-swing design principles and the latter is a full-swing circuit, we will refer to them as partial-swing and full-swing oscillators for the rest of the paper.

Partial-swing ring oscillators are designed as linear feedback systems. If three or more delay cells are cascaded, the phase shift around the loop exceeds 360° and sinusoidal oscillation can occur according to Barkhausen's criteria [4]. Although the nonlinearity of the delay cell means the output is not perfectly sinusoidal, it is important to know that the output is closer to a sine wave than a square wave. The amplitude of the output for a partial-swing oscillator depends on the load resistance and the tail current.

Another concept discussed in [2] is self biasing. Self biasing for the Maneatis oscillator is shown in Fig. 3. The feedback loop sets the lower end of the voltage swing so that the symmetric load transistors never leave the region in which they approximate matched resistors. A useful artifact of self



Fig. 2. Lee/Kim full-swing delay cell.



Fig. 3. Self-biasing circuit for the Maneatis partial-swing delay cell.

biasing is that the loop continually adjusts the tail current bias voltage, tracking  $V_{SS}$  variations and decreasing sensitivity to  $V_{SS}$ .

As mentioned, full-swing ring oscillators are designed as full swing inverter delay cells. Besides inverting the input, the positive feedback of the load causes the delayed transition edge to be sharp, creating an almost square wave output. The amplitude of the output is rail-to-rail.

These two attributes, fast transitions and rail-to-rail swing, cause the full-swing ring oscillator to reject intrinsic noise better than a partial-swing ring oscillator. It is well known that noise injections at transitions cause more phase error than when the output is saturated [5], [6]. Fast transitions cause this window of sensitivity to be very small. Rail-to-rail swing causes the charge swing at the oscillator output to be maximum. When the signal charge is maximum, the charge injection from noise sources is relatively smaller [5]. On the other hand, the partial-swing oscillator has smaller charge swing and slow transitions leading to poor intrinsic noise rejection.

The partial-swing oscillator rejects power supply variations



Fig. 4. Circuit to generate band-limited power supply noise.

well, though. As long as the resistor matching is good, the differential structure isolates  $V_{DD}$  from the output. The large output impedance of the tail current source isolates the output from  $V_{SS}$  and the self-biasing loop further increases this impedance. Unlike the partial-swing oscillator, the full-swing oscillator does not have any mechanisms besides the basic pseudo-differential structure to minimize power supply noise conversion to phase noise.

In sum, we expect the full-swing oscillator to have better intrinsic noise rejection and the partial-swing oscillator to have better power supply rejection. Although this qualitative explanation has value, a method for quantifying the effect of *both* sources of phase noise is necessary for comparison between different oscillator topologies. The next section discusses how this comparison can be made.

# III. POWER SUPPLY NOISE SIMULATION

Although the statistics of power supply noise are hard to predict without knowing the environment, we can make a fair comparison between oscillators by injecting noise with identical statistics into two oscillators and comparing the phase noise degradation that results. The power supply noise can be modeled as a band-limited white noise source and implemented in a circuit simulator as shown in Fig. 4 where the resistor  $R_0$  generates the white noise and the  $R_1C$  filter limits bandwidth of the noise.

We use a figure of merit (FOM) to be sure that comparisons are fair. The FOM normalizes phase noise by power and oscillation frequency so that good phase noise performance is truly a result of circuit structure and not simply caused by burning more power or oscillating at a slower frequency. The equation for FOM is [7]:

$$FOM = 20\log(f_0) - \mathcal{L}(\Delta\omega) - 10\log(P) \tag{1}$$

where  $f_0$  is the oscillation frequency in Hz,  $\mathcal{L}(\Delta \omega)$  is the phase noise in dBc/Hz at an offset frequency  $\Delta \omega$  and P is the power in watts. Although this equation does normalize for oscillation frequency, we still designed the oscillators to run at the same frequency of 1GHz since the normalization is not perfect. Therefore, the FOM is valuable mostly for power normalization and rough comparison to other oscillator designs (e.g. LC oscillators).



Fig. 5. Figure of merit vs. power supply variance for the partial-swing oscillator.

In order to quantify both the intrinsic and power supply noise we sweep the variance of the power supply noise by increasing  $R_0$  and then measure the phase noise at a fixed offset frequency of 1MHz using SpectreRF. The FOM will be dominated by intrinsic noise for low amounts of power supply noise, but at some point will be degraded by the power supply noise. Fig. 5 shows a plot of FOM vs. power supply variance for the partial-swing oscillator. There are two curves shown, FOM vs. V<sub>DD</sub> noise variance and FOM vs.  $V_{SS}$  noise variance. The plot is analogous to the familiar gainbandwidth plot. Since the intrinsic noise dominates for small amounts of power supply noise, good intrinsic noise rejection corresponds to high "DC gain". Likewise, good power supply noise rejection corresponds to "bandwidth". Although these terms are misnomers, we will continue to use them for their intuitive value.

Fig. 6 shows the FOM vs.  $V_{DD}$  and FOM vs.  $V_{SS}$  curves for the full-swing oscillator. Notice that the intrinsic noise rejection or "DC gain" is better for the full-swing oscillator as we expected. Also, the power supply noise rejection or "bandwidth" is better for the partial-swing oscillator.

### **IV. SIMULATION RESULTS**

A thorough analysis of phase noise must consider three main sources of phase noise in ring oscillators:  $V_{DD}$  noise,  $V_{SS}$  noise, and intrinsic noise. It would be counterproductive to design an oscillator that rejects  $V_{DD}$  noise and then use it in an environment that is dominated by  $V_{SS}$  noise. Through parametric sweeps, we show in this section how the simulation method described in Section III can be used to determine which oscillator performs best for various amounts of each of these three noise sources. These results allow a designer to make an informed choice of a ring oscillator if the designer knows the noise environment of the application. The results also verify qualitative explanations given earlier.



Fig. 6. Figure of merit vs. power supply variance for the full-swing oscillator.

In this section, we compare the oscillators explained in Section II because they are representations of the two general classes of ring oscillators. Note, however, that we could compare any oscillators of interest, including LC oscillators.

In Figs. 5 and 6 we showed an FOM vs. power supply noise variance plot. In that plot, the noise was injected on the  $V_{DD}$  side while  $V_{SS}$  was noiseless and vice versa. Since we are interested in finding the overall FOM with both  $V_{DD}$  and  $V_{SS}$  noise we fix the amount of noise on  $V_{SS}$  to  $10^{-6} V^2$ and sweep  $V_{DD}$  noise variance as before. The resulting plot is shown in Fig. 7 along with the  $V_{DD}$  and  $V_{SS}$  noise curves from before. This plot is intuitively satisfying since for small values of  $V_{DD}$  noise, the FOM equals the  $V_{SS}$  noise only FOM and for large values of  $V_{DD}$  noise, the FOM follows the  $V_{DD}$  noise only FOM curve. This tells us that the FOM for all amounts of  $V_{DD}$  and  $V_{SS}$  noise can be extrapolated from the two  $V_{DD}$  and  $V_{SS}$  noise only curves. We verified this by repeating the simulation for various amounts of  $V_{SS}$ noise and matching it to extrapolated data.

Fig. 8 shows which oscillator has the best FOM for various amounts of  $V_{DD}$  and  $V_{SS}$  noise. The curve shows where the partial-swing oscillator FOM is equal to the full-swing oscillator FOM. Towards the top left (low  $V_{SS}$  noise, high  $V_{DD}$  noise) the full-swing oscillator has better performance and towards the bottom right (high  $V_{SS}$  noise, low  $V_{DD}$  noise) the partial-swing oscillator performs better. Notice that for this range of reasonable amounts of supply noise, the full-swing oscillator has a larger region where it outperforms the partialswing oscillator.

#### V. CONCLUSION

This paper has demonstrated a method to quantitatively compare the phase noise performance of ring oscillators in the presence of both intrinsic and power supply noise. Power supply noise is often a significant contributor of phase noise and cannot be ignored. Furthermore, the power supply noise



Fig. 7. Figure of merit vs.  $V_{DD}$  variance with fixed  $10^{-6}\ V^2\ V_{SS}$  noise variance.



Fig. 8. Comparison plot of oscillator FOM for various amounts of both  $V_{DD}$  and  $V_{SS}$  noise. The line shows where the partial-swing and full-swing FOM are equal.

comes from both  $V_{DD}$  and  $V_{SS}$ . An analysis that focuses on  $V_{DD}$  noise while ignoring  $V_{SS}$  noise would be misleading.

#### ACKNOWLEDGMENT

This work is supported by the Air Force Research Laboratory, Space Vehicles Directorate, Kirtland AFB, NM under Contract F29601-02-2-0209, entitled "Mixed-Signal Electronics Technology for Space," and by the Semiconductor Research Corporation under contract 2003-HJ-1076.

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