# A 6.39GHz-14GHz Series Resonator Mode-Switching Oscillator with 186-188dB FoM and 197dB FoMA in 65nm CMOS

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Abstract — CMOS LC voltage-controlled oscillators (VCO) with octave frequency tuning-range (FTR) are attractive for wideband radios. An area and power-efficient resonant mode-switching approach is presented that enables wide-FTR oscillators without compromising inductor Q, resulting in low phase noise and high VCO Figure-of-Merit (FoM). The proposed series resonator mode-switching approach results in a 6.4GHz to 14GHz VCO (74.6% FTR) in 65nm CMOS that achieves 186dB-188dB FoM. The scalability of this approach towards achieving even larger FTR is also demonstrated by a triple-mode 2.2GHz to 8.7GHz (119% FTR) VCO.

### I. INTRODUCTION

A VCO with octave frequency tuning range (FTR) can be used in conjunction with dividers to generate all frequencies below its highest oscillation frequency. Additionally, quadrature-LO generation in integrated transceivers is simplified with a VCO operating at  $2f_{LO}$  followed by a divide-by-2. Therefore, CMOS VCOs with 6GHz to 12GHz FTR are attractive for multi-standard wireless radios targeting prevalent wireless standards between 400MHz to 6GHz [1]. The targeted FTR can be achieved by multiplexing two or more LC oscillators however, a single octave-FTR LC VCO that achieves similar performance can potentially result in smaller area.

Simultaneously achieving low phase noise and wide FTR in an LC VCO with switched-capacitor tuning requires unrealistically small inductor sizes, leading to low tank impedance [2]. In addition, the inductor quality-factor (Q) is frequency dependent which can further decrease the lower impedance at low oscillation frequencies. Alternate topologies with switches in series with inductors or across transformers have been proposed for wide FTR, but the phase noise is limited by switch losses, particularly at high frequencies.

A transformer-based resonator mode-switching VCO that enables lossless mode-switching is proposed in [2], achieving excellent phase noise and VCO figure-of-merit(FoM) across an octave FTR up to 5.62GHz. This approach ensures low area overhead by placing one transformer coil inside another - however the mutual coupling that underlies the approach degrades inductor Q. An extension to three resonant modes is proposed in [3] in order to achieve octave FTR at higher oscillation frequency (~13GHz). However, this leads to a tradeoff between increased VCO area and higher power



Fig. 1. Schematic of proposed series resonator mode-switching CMOS VCO with octave tuning range (6.39GHz to 14GHz).

consumption [3]. In both these schemes, inductor Q is lowered due to coupled coils and crossovers. Parallel resonator mode-switching approaches that avoid inductor Q tradeoffs are proposed in [4], [5]. Octave FTR up to 8.45GHz is demonstrated in [4]. However, this approach utilizes four inductors, each with an inductance of  $L_T$ (570pH) with the parallel mode-switching resulting in  $L_T/4$  and  $L_T/2$  inductances. The use of multiple parallel inductors to achieve smaller inductance reduces the area benefits of using a single wide-FTR LC VCO.

# II. SERIES RESONATOR MODE-SWITCHING VCO

Fig. 1 shows the schematic of the proposed dual-mode series resonator mode-switching CMOS VCO that achieves 6.39GHz to 14GHz FTR (2.2x). Similar to other dual-mode schemes, [2]–[5], [7], this approach provides high impedance in both low-frequency (LB) and high-frequency (HB) modes (Fig. 2(a)), while also achieving excellent FoM and ensuring area efficiency.

The core VCO consists of two symmetric inductor structures,  $S_1$  and  $S_2$ , placed in series and loaded by cross-coupled pairs,  $-G_{M,LB}$ ,  $-G_{M,HB1}$  and  $-G_{M,HB2}$  (Fig. 1). Each of the symmetric sections,  $S_1$  and  $S_2$ , consist of two metal wires,  $W_1$  and  $W_2$ , with  $20\mu m$  widths and  $2\mu m$  spacing between them. The inductor sections are connected to the  $-G_M$  cells and to the supply at P1, P2, P3, P4 and  $X_1$ ,  $X_2$ ,  $X_3$  respectively (Fig. 1). The



Fig. 2. (a) Simulated resonator impedance in HB and LB modes, (b) Current distribution in inductor structure -  $W_2$  carries less current than  $W_1$  in HB Mode, while the effective width is  $W_1 + W_2$  in LB mode [6], (c) Simulated inductor Q in LB and HB modes.



Fig. 3. Resonator properties in HB and LB modes for series resonator mode-switching.

VCO drives PMOS buffers whose output is provided to the open-drain NMOS differential output stages.

In the high-frequency mode (HB), the low-band cross-coupled pair ( $-G_{M,LB}$ ) is disabled while the high-band cross-coupled pairs,  $-G_{M,HB1}$  and  $-G_{M,HB2}$ , are enabled. Due to the short between P2 and P3, the two LC oscillators are tightly coupled to each other. As shown in Fig. 3, in the HB mode, the voltages on P1 and P2 are anti-phase and the voltages on P1 and P4 are in-phase, hence capacitance,  $C_{LB}$ , does not load the resonators. Therefore, the oscillation frequency in HB mode,  $\omega_{HB} = \frac{1}{\sqrt{L_{HB}C_D}}$  where  $L_{HB}$  is the inductance of each inductor section ( $L_{HB} = L_{S1} = L_{S2}$ ). Since the  $-G_{M,HB1}$  and  $-G_{M,HB2}$  cells are tightly-coupled in HB mode, the 2x increase in power consumption also provides 2x lower phase noise leading to the same VCO FoM.

In the low-frequency mode (LB),  $-G_{M,HB1}$  and  $-G_{M,HB2}$  are disabled and  $-G_{M,LB}$  is enabled. Consequently, the signals at P1 and P4 are forced to be anti-phase and hence  $C_{LB}$  appears across the resonator in addition to  $C_D$  (Fig. 3). In LB mode, the oscillator operates with a higher inductance ( $L_{LB} = L_{S1} + L_{S2}$ ) leading to oscillation frequency,  $\omega_{LB} < \omega_{HB}$  (Fig. 3). Thus, tank inductance goes from  $L_{HB} = 191pH$  in HB mode to  $L_{LB} \approx 2L_{HB} = 360pH$  in LB mode. The mutual coupling between  $S_1$  and  $S_2$  is negligible (< 0.1) which is confirmed by the near-doubling in inductance between modes. Simulations confirm the theoretically predicted minimal impact on phase noise due to the enable transistors in the  $-G_M$  cells, demonstrating that resonant-mode switching is more effective than inductor switching for achieving wide FTR.

The  $\sim 2x$  increase in inductance in LB leads to high resonator impedance both modes (Fig. 2(a)), ensuring low power consumption across FTR. Inductor Q is proportional to  $\sqrt{Area}$  to the first-order [8] and hence, the Q achieved by operating inductors in parallel is lower than the Q that can be achieved by a single inductor occupying the same area and having the same effective inductance. Notably, series mode-switching utilizes area proportional to the resonator inductance in both LB and HB modes and hence can result in area-efficient wide-FTR VCOs.

The proposed switching scheme can also address the problem of inductor Q variation in wide FTR VCOs. Tradeoffs between substrate loss and resistive loss lead to a peak inductor Q frequency that is dependent on conductor width and inductor area for single-turn inductors. EM simulations (Fig. 2(b)) confirm that in HB mode, identical voltages at P1 and P4 result in small current through  $W_2$  whereas in LB mode, the two wires  $W_1$  and  $W_2$  operate with an effective width of  $W_1+W_2$ . This change in effective inductor width causes a desirable shift in the peak inductor Q frequency across LB and HB modes ensuring high inductor Q across FTR (Fig. 2(c)).

Frequency tuning is achieved in both modes using a 6-bit digitally switched capacitor bank,  $C_D$  with an NMOS varactor providing frequency overlap (Fig. 3). Switched capacitors,  $C_{LB}$ , provides additional 2-bits of tuning in LB mode. Parasitic-aware layout of the switched capacitors minimizes parasitic inductance and resistance due to routing.



Fig. 4. Broadband inductor model to evaluate impact of supply-switch parasitics on VCO.

A broadband model for the inductor structure is used to study the impact of supply switch parasitics in the VCO (Fig. 4). In LB mode, the center of the inductor structures,  $X_2$ , acts as virtual ground and therefore supply for  $-G_{M,LB}$  is connected to  $X_2$ . The virtual ground shifts to  $X_1$  and  $X_3$  in HB mode and therefore supply for  $-G_{M,HB1}$  and  $-G_{M,HB1}$  is provided through those nodes. The supply switch is sized while considering the tradeoff between increased phase noise due to high on-resistance and the capacitive loading associated with large switch size, which affects LB mode operation. Simulations based on the model in Fig. 4 show < 1dB degradation in phase noise due to switch parasitics.

# A. Extension to VCO with higher number of modes

The proposed series mode-switching approach can be extended to higher number of modes to achieve wider FTR. Fig. 5 shows the schematic of a triple-mode 2.2GHz to 8.7GHz ( $\sim$ 4x FTR) VCO that can switch between three resonant modes, high-band (LB), mid-band (MB) and low-band (HB) with increasing inductance, and hence high impedance across modes. The principle of operation is similar to that of the dual-mode VCO shown in Fig. 3.

### **III. MEASURED PERFORMANCE**

The dual-mode and triple-mode VCOs are implemented in a 9-metal GP 65nm process with  $3.4\mu m$  thick top



Fig. 5. Schematic of a 2.2GHz-8.7GHz VCO that extends the proposed series resonant mode-switching approach to 3 modes.



Fig. 6. Die photo of dual-mode (6.4GHz-14GHz) and triple-mode (2.2GHz-8.7GHz) VCO.



Fig. 7. Measured triple-mode VCO phase noise and FoM.

metal layer (Fig. 6). VCO phase noise is measured using a Keysight 5052B Signal Analyzer and Keysight 5053A 26GHz downconverter.

The triple-mode VCO achieves 2.2GHz to 8.7GHz FTR while consuming 3.5mW in the LB(one active  $-G_{M,LB}$  cell) and 37mW in the HB(four active  $-G_{M,HB}$  cells). The phase noise varies from -136 to -148dBc/Hz (at 10MHz offset) across the FTR (Fig. 7). The triple-mode VCO FoM matches expectations in high band but is lower than simulated in the low-band and mid-band due to a biasing error. However, the VCO still achieves >183dB phase-noise FoM from 3.5GHz to 8.7GHz (Fig. 7).

The dual-mode VCO operates with a supply voltage of 0.45V to 0.6V and consumes  $\sim$ 2.2mW in LB mode and 10mW in the HB mode. The measured VCO FTR (6.4GHz to 14GHz) is shown in Fig. 8 with 500MHz overlap between LB and HB modes. Fig. 9 plots the measured phase noise across offset frequencies at four different VCO frequencies and Fig. 10 plots the measured dual-mode VCO phase noise and FoM at 1MHz and 10MHz offset frequencies. The dual-mode VCO phase noise varies from -130dBc/Hz to -137dBc/Hz at 10MHz offset frequencies and the measured 186-188dB FoM is comparable to that achieved by VCOs at lower frequencies (Table I), particularly when the lower Q of

 TABLE I

 MEASURED PERFORMANCE SUMMARY AND COMPARISON TO STATE-OF-THE-ART.

|      | Freq.      | Power    | Area               | PN            | $\Delta f$ | FoM         | FoMT     | FoMA     | CMOS  |
|------|------------|----------|--------------------|---------------|------------|-------------|----------|----------|-------|
|      | [GHz]      | [mW]     | [mm <sup>2</sup> ] | [dBc/Hz]      | [MHz]      | [dBc/Hz]    | [dBc/Hz] | [dBc/Hz] | Tech. |
| This | 6 30 14    | 2 2 10 3 | 0.126              | 130 3/ 137 7  | 10         | 188 186     | 205 203  | 107 105  | 65nm  |
| Work | 0.39-14    | 2.2-10.5 | 0.120              | -150.5/-157.7 | 10         | 100-100     | 203-203  | 197-195  | 0.5mm |
| [7]  | 2.75-6.25  | 5.8-9.4  | 0.35               | -129/-118     | 1          | 184-188.2   | 201-206  | 189-193  | 65nm  |
| [4]  | 3.24 8.45  | 20       | 0.324              | -150.2/-144.4 | 10         | 188.6-189.3 | 208      | 194-194  | 40nm  |
| [9]  | 2.4-5.3    | 4.4-6    | 0.253              | -149/-139     | 10         | 187-189     | 205-207  | 193-195  | 65nm  |
| [3]  | 5.12-12.95 | 5-10     | 0.33               | -122.9/-122   | 1          | 184.5-189.7 | 204-208  | 190-195  | 180nm |
| [2]  | 2.48-5.62  | 9.8-14.2 | 0.294              | -156.6/-151.7 | 20         | 188.8-193.7 | 207-211  | 195-199  | 65nm  |

 $FoM = -PN + 10\log\left\{\left(\frac{f_0}{\Delta f}\right)^2 \left(\frac{1mW}{P_{DC}}\right)\right\}; FoMT = FoM + 20\log\left(\frac{FTR}{10}\right); FoMA = FoM - 10\log\left(\frac{Area}{1mm^2}\right)$ 



Fig. 8. Measured dual-mode VCO FTR (500MHz band overlap).



Fig. 9. Measured VCO phase noise across offset frequency.

the capacitor switch bank at  $\sim 2.5x$  higher frequency is considered. As described in Section II, the series resonator mode-switching scheme achieves significant improvement in FoMA which normalizes VCO area [8].

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Fig. 10. Measured dual-mode VCO phase noise and FoM.

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