21.6 A 1.2cm² 2.4GHz Self-Oscillating Rectifier-Antenna Achieving -34.5dBm Sensitivity for Wirelessly Powered Sensors

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Ubiquitous Internet-of-Everything (IoE) applications require low-cost, miniature sensors with long lifetimes. Wirelessly-powered ICs that harvest energy from an RF beacon or from existing wireless signals can address challenges associated with battery size, capacity and replacements [1-5]. Given FCC transmit power limits, the operating range of wirelessly-powered sensors is limited by rectifier sensitivity rather than by communication link budgets. In this work, we present area-constrained antenna-rectifier architectures that leverage electrically-small antennas and rectifier circuits to achieve -34.5dBm sensitivity for 1.6V output with 1.8MΩ load (CC topology) and -24dBm sensitivity for 2.5V output with 100KΩ load (CP topology), representing a >5× improvement in sensitivity (>2× improvement in range) over current state-of-the-art and >1V output voltage [1]. Notably, this improvement is obtained even for cold-start with the typical rectifier storage capacitor as the only off-chip component, resulting in a very compact 1.2cm² complete 2.4GHz antenna-rectifier system area.

The proposed rectifier concept is depicted in Fig. 21.6.1. State-of-the art rectifier performance in prior work [1,2] had been achieved using an electrically-small antenna that resonates rectifier input capacitance, thereby providing a passive voltage boost and hence improving sensitivity. However, the sensitivity for a given load resistance, R_L, and target output voltage are ultimately limited by transistor threshold voltage and reverse leakage. The architecture proposed here is based on two observations: firstly, a self-V_{TH}-cancellation rectifier stage can be redrawn as a complementary cross-coupled oscillator (Fig. 21.6.1) – in this case, RF energy at nodes X_P and X_N is rectified and stored on the capacitor at node Y. Secondly, since the loop antenna used to resonate rectifier capacitance is electrically small, it is highly inductive and has a high Q (~120), particularly when compared to an on-chip inductor. In this work, rectifier operation is divided into two phases (Fig. 21.6.1). In *Phase 1*, the rectifier uses the input RF signal to build voltage, $V_{RECT} \approx V_{C1}$, on capacitors, C_1 and C_2 (PMOS S_1 is enabled at cold start where $V_{C1} = 0$). When $V_{RECT} > V_H$, S_1 is disabled and S_2,S_3 are enabled, initiating *Phase 2*. In this phase, the stored rectifier voltage is applied to the first rectifier stage (through S_2), and the complementary cross-coupled pair creates a negative resistance at RF that appears in parallel with the high-Q inductive antenna and rectifier capacitance. The resulting 2.4 GHz self-oscillation in the rectifier-antenna (which is assisted by the RF beacon) leads to large voltage swing at the rectifier input, adding an active boost in addition to the passive boost. The higher voltage swing at the rectifier input in *Phase 2* leads to higher rectifier output voltage on R_L, (through switch S_3) for the same RF input power. Capacitor C_1 discharges during this phase and when its voltage falls below voltage V_L, S_2 and S_3 are disabled and S_1 is enabled, returning the rectifier back to *Phase 1* operation. The architecture in Fig. 21.6.1 can further be viewed as a DC-DC converter that reuses the rectifier's 1st-stage, where antenna inductance enables DC-RF conversion while the rectifier performs RF-DC conversion. In general, for wirelessly-powered sensors limited by rectifier maximum distance of operation, the sensitivity and efficiency at minimum sensitivity are more critical than the peak efficiency. Additionally, optimal sensitivity is only achieved *when RF input signal is present during Phase 2*. Active boost during *Phase 2* ensures that voltage V_H on capacitor C_1 is translated to 3-5× larger V_{RECT} on C_2. Hence, for a given target V_{RECT}, the sensitivity for cold start is only limited by input power required to achieve the much smaller V_H resulting in >5× improvement in rectifier sensitivity *at cold start*, particularly when practical load currents for power-on-reset and power management circuits are considered.

Two implementations of the proposed architecture optimized for different load currents are described in the following. Figure 21.6.2 shows the schematic of an implementation with a complementary cross-coupled pair (CC) performing the active boost as described previously. In the CC implementation, M_{1-4} are small transistors to improve efficiency in *Phase 1*. It is important to ensure that rectifier loading during *Phase 1* is minimal in order to achieve best sensitivity. Therefore a sub-100nA comparator $COMP_1$ (with asymmetric rise time on the two inputs to avoid false trigger) can be used to detect voltage on C_1 and initiate *Phase 2*. The level shifters ensure that the highest voltage (V_{RECT}) is applied to the enable/disable switches – however, since the gate voltage is limited to V_H initially during cold-start, V_H must be sufficiently high to ensure switch operation. In the case of sensors operating with low supply voltages, the 3-5× boost implies that logic operation rather than output voltage targets determines the minimum acceptable V_H. Therefore, in this implementation, V_H is set to 450mV, which leads to V_{RECT} > 1.5V in *Phase 2*. *Phase 2* is disabled when V_{C1} is discharged to 380mV (controlled by hysteresis in $COMP_1$).

Reusing the first rectifier stage in the CC topology avoids an increase in rectifier capacitance and consequent sensitivity degradation during *Phase 1*. However, in *Phase 2*, M_{1-4} (Fig. 21.6.2) operate with waveforms similar to Class-A which can limit peak efficiency – note that the CC implementation is optimized to improve *efficiency at sensitivity* rather than peak efficiency. The peak simulated steady-state efficiency (assuming constant V_{C1} and including switch losses) for the selected device sizes is 32% for R_L = 500KΩ, V_{C1} = 0.4V corresponding to V_{RECT} = 1.35V. In order to improve efficiency for larger load currents, a PMOS-only cross-coupled-pair-based "CP" topology is shown in Fig. 21.6.3. Rectifier operation in *Phase 1* is similar to the CC topology. However, *Phase 2* is divided into two sub-categories – *Phase 2a* and *Phase 2b*. As shown in Fig. 21.6.3, two cross-coupled pairs are added at the input of the rectifier – with relatively large device sizes for M_{3-4}. Following *Phase 1*, $V_{C1} > V_{H1}$ enables Phase 2a where initially M_{1-2} provide an active boost that results in higher V_{RECT}. In *Phase 2a*, the band-gap and comparators are also enabled for accurate transitions. When $V_{RECT} > V_{H2}$, *Phase 2b* is initiated by enabling switches S_{5-7}. The large M_{3-4} devices switch completely during *Phase 2b* with Class-D like waveforms, thereby improving efficiency (~25%) for load resistances of the order of ~5kΩ. In the CP topology in Fig. 21.6.3, the differential loop antenna provides a relatively simple DC path to ground without impacting rectifier RF performance, even after accounting for any ground-loop inductance.

The CC and CP topologies were implemented in a 65nm CMOS process with 3.4um thick top metal layer. The ICs are packaged with antennas on a Rogers 4350B PCB. Rectifier sensitivity is defined in terms of the power available to an isotropic antenna, $P_{AV,ISO}$ [1,2]. Figure 21.6.4 summarizes the measured performance of the CP topology. Phase-1 operation is demonstrated by observing the measured transient voltages on V_{C1} and V_{RECT} where the rectifier charges V_{C1} to 450mV before initiating *Phase 2* which increases V_{RECT} to 1.6V. As shown in Fig. 21.6.4, V_{RECT} and V_{C1} measurements during *Phase 1* and *Phase 2* demonstrate >3× increase in V_{RECT} for the same RF input power. Measurements of V_{RECT} across $P_{AV,ISO}$ demonstrate -34.5dBm sensitivity to initiate *Phase 2* and achieve V_{RECT}>1V. Measured sensitivity at 2.4GHz demonstrates ~3dB variation across the ISM band for the CC topology.

The measured sensitivity and performance across frequency of the CP topology from cold-start are summarized in Fig. 21.6.5 for load resistance of 1.8MΩ. The larger transistor sizes lead to ~2.5V V_{RECT} when *Phase 2a* and subsequently *Phase 2b* are triggered at 0.45V V_{C1}. Stand-alone efficiency in *Phase 2b* is measured by applying an external V_{C1} while varying R_L. Peak efficiency of 27.7% is observed for R_L = 5kΩ and V_{C1}= 0.6V with V_{RECT} achieving 2.2V. Performance of the CC and CP rectifier-antenna topologies is summarized and compared to prior art in Fig. 21.6.6. The rectifier circuits occupy only 0.018mm² (CC) and 0.015mm² (CP) while capacitors and logic occupy 0.6 mm² (Fig. 21.6.7).

Acknowledgements:
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References:
[1] J. Kang et al., "A 3.6 cm² Wirelessly-Powered UWB SoC with -30.7dBm Rectifier Sensitivity and Sub-10cm Range Resolution," *IEEE Radio Frequency Integrated Circuits Symp.,* May 2015.
[2] M. Stoopman et al., "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," *IEEE J. Solid-State Circuits,* vol. 49, no. 3, pp. 622-634, Mar. 2014.
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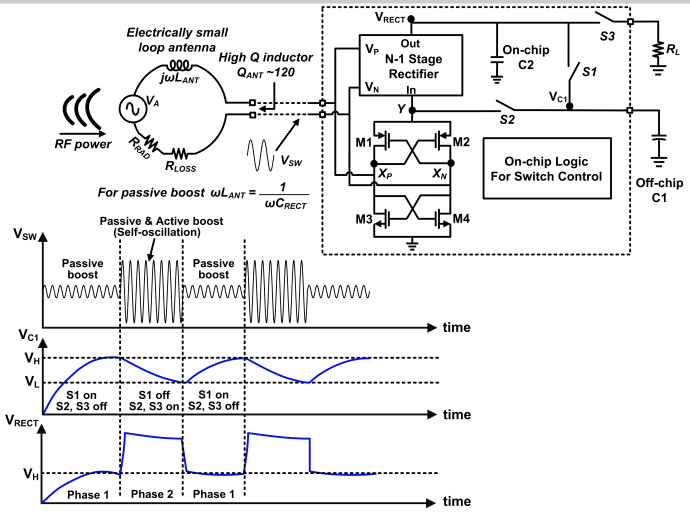


Figure 21.6.1: Rectifier-antenna architecture that leverages electrically-small, high-Q antenna to achieve self-oscillation: following initial charging in Phase 1, self-oscillation boosts V_{RECT} in Phase 2.

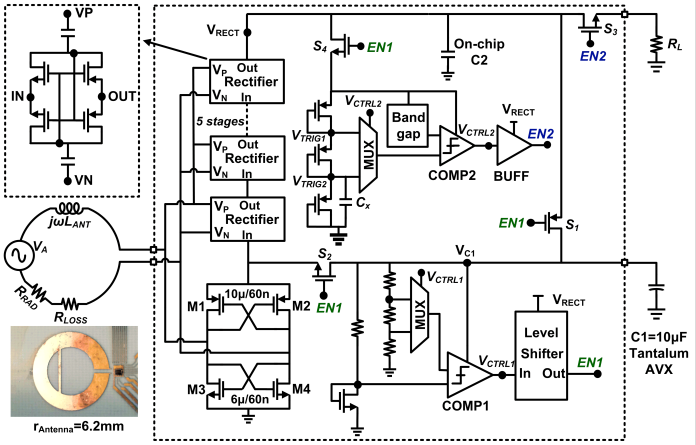


Figure 21.6.2: Schematic of rectifier-antenna and logic circuits that control Phase-1 and Phase-2 transitions for complementary cross-coupled (CC) topology.

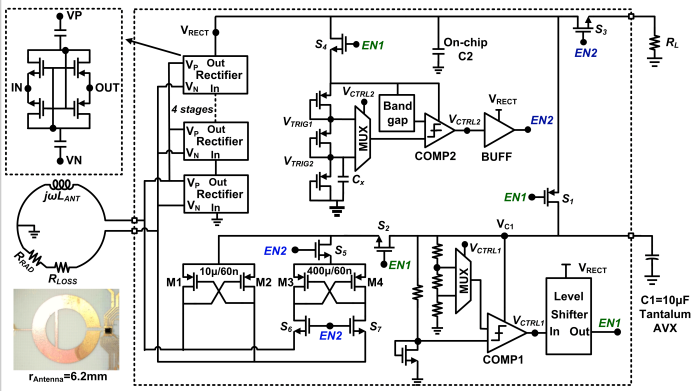


Figure 21.6.3: Schematic of rectifier-antenna and logic circuits for cross-coupled PMOS (CP) topology: the larger M3 and M4 transistors are enabled in Phase 2b resulting in higher efficiency for small load resistances.

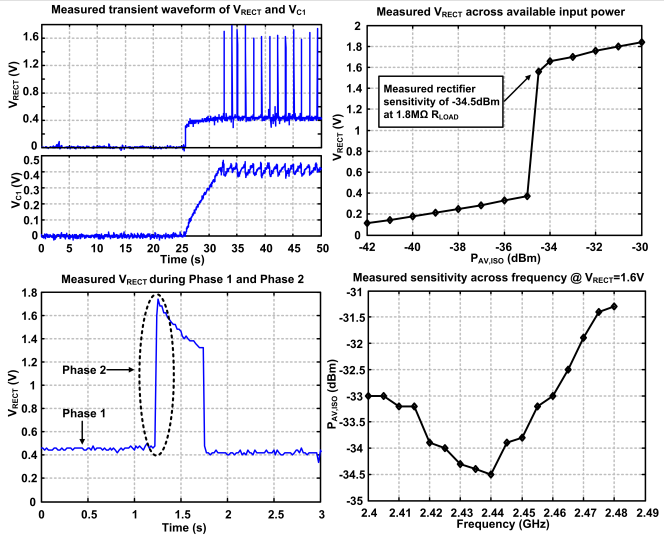


Figure 21.6.4: Measured transient voltages, sensitivity and performance across the 2.4GHz band for CC rectifier-antenna topology.

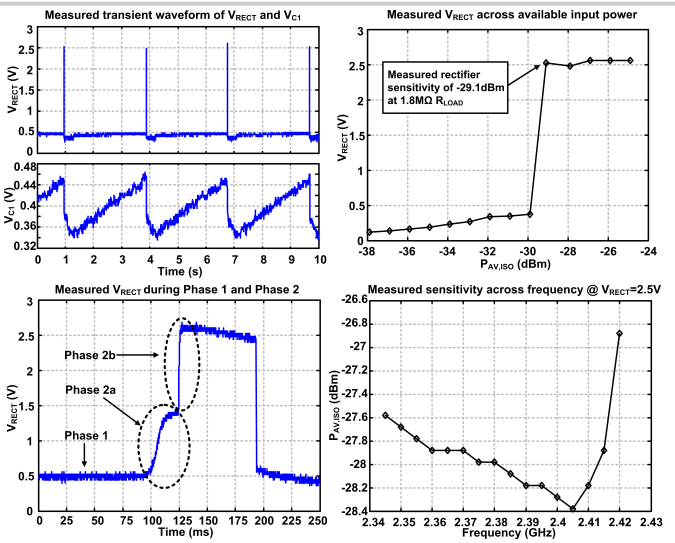
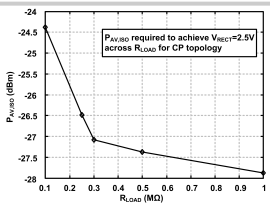


Figure 21.6.5: Measured transient voltages, sensitivity and performance across the 2.4GHz band for CP rectifier-antenna topology.



	Tech.	Antenna Area	Sensitivity (dBm)	V_{RECT}@ Sensitivity	R_{LOAD}@ Sensitivity	Freq.	Requirement
This work (CC)	65nm CMOS	1.21cm²	-34.5	1.6V	1.8MΩ	2.4 GHz	Deep N-Well
This work (CP)	65nm CMOS	1.21cm²	-26.5	2.5V	250K	2.4 GHz	Deep N-Well
RFIC 15 [1]	65nm CMOS	1.33cm²	-30.7	1	∞	2.4 GHz	Deep N-Well
RFIC 15 [1]	65nm CMOS	1.33cm²	-27	1	1.8MΩ	2.4 GHz	Deep N-Well
JSSC 14 [2]	90 nm CMOS	12cm²	-27	1	∞	868 MHz	Control Loop
JSSC 14 [2]	90 nm CMOS	12cm²	-25	1	1.8MΩ	868 MHz	Control Loop
JSSC 11 [3]	90um CMOS	No antenna	-24	1	∞	915 MHz	Deep N-Well
JSSC 08 [4]	0.25um CMOS	30cm²	-22.6	2	∞	906 MHz	External Pre-charge
TCAS-I 07 [5]	0.18um CMOS	37.4cm²	-18	0.8	∞	970 MHz	-

Figure 21.6.6: Performance summary of CC and CP rectifier-antenna topologies and comparison to state-of-art.

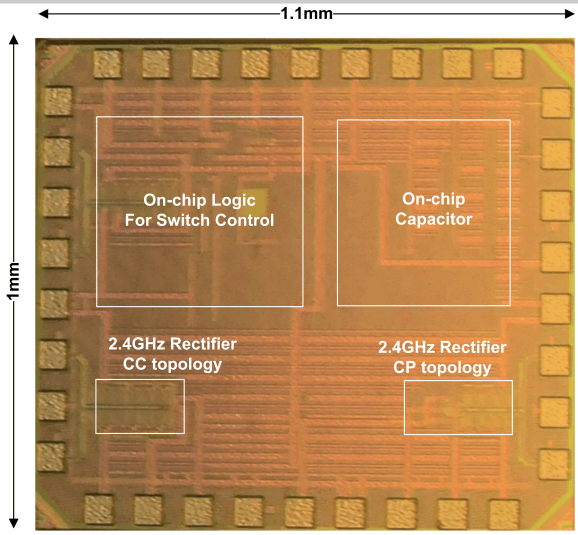


Figure 21.6.7: Die micrograph of 2.4GHz Self-Oscillating Rectifier-Antenna and on-chip logic for switch control implemented in 65nm CMOS.

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