A Survey on Application Specific Processors

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Topics Covered

• Introduction to Application Specific Processors
• Digital Signal Processors
• Application Specific Instruction Set Processors
• Application Specific Integrated Circuits
• Field Programmable Gate Arrays
Application Specific Processors

- Application specific processors emerged as a solution for high performance, cost effective, and low power consumption processors.
- Devices such as TVs, cell phones, and GPSs they all have a form of application specific processors.
- Application specific processors can be classified into three major categories:
  - DSPs
  - ASIPs
  - ASICs
Application Specific Systems

- Application specific systems can be designed using:
  - GPP
  - ASIC
  - ASIP

<table>
<thead>
<tr>
<th></th>
<th>GPP</th>
<th>ASIP</th>
<th>ASIC</th>
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<tbody>
<tr>
<td>Performance</td>
<td>low</td>
<td>high</td>
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</tr>
<tr>
<td>flexibility</td>
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<td>good</td>
<td>poor</td>
</tr>
<tr>
<td>HW design</td>
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<td>very large</td>
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<tr>
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<tr>
<td>power</td>
<td>large</td>
<td>medium</td>
<td>small</td>
</tr>
<tr>
<td>reuse</td>
<td>excellent</td>
<td>good</td>
<td>poor</td>
</tr>
<tr>
<td>market</td>
<td>very large</td>
<td>relatively large</td>
<td>small</td>
</tr>
<tr>
<td>cost</td>
<td>mainly on SW</td>
<td>SOC</td>
<td>volume sensitive</td>
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Field Programmable Gate Arrays

- An integrated circuit designed to be configured by the customer or designer
- Generally specified using a hardware description language
- FPGAs can be used to implement any logical function that an ASIC could perform
- ASIC became more rare due to the flexibility of FPGAs
Digital Signal Processors

Yousef Qassim
Introduction

- Specialized microprocessors optimized for the needs of digital signal processing
- Data-intensive applications such as video and internet browsing on mobile devices
- High performance, low cost, and low power consumption
- Nowadays, more than 68% of DSPs are used in the wireless sector precisely in the mobile handsets and base stations
Background and History

- The concept of DSP was introduced in mid 1970s
- The rise in interest for DSPs is the result of how to solve real world problems using digital systems
- Few years later a toy by the name of Speak and Spell was created using a single integrated circuit to synthesize speech
- DSPs differ from other microprocessors is that DSP intend to do complex math while guaranteeing real-time processing
Background and History

- Early DSPs
  - Dual/multiple data buses
  - Logic to prevent over/underflow
  - Single cycle complex instructions
  - Hardware multiplier
  - Little to no support of interrupt
  - Support of special instructions to handle signal processing
DSP Improvements
Modern DSP Architecture

- Hardware modulo addressing, allowing circular buffers to be implemented without having to constantly test for wrapping.
- Memory architecture designed for streaming data, using DMA extensively.
- Driving multiple arithmetic units may require memory architectures to support several accesses per instruction cycle.
- Separate program and data memories (Harvard architecture), and sometimes concurrent access on multiple data busses.
Modern DSP Architecture

- Special SIMD (single instruction, multiple data) operations
- Some processors use VLIW techniques so each instruction drives multiple arithmetic units in parallel
- Special arithmetic operations, such as fast multiply-accumulates (MACs).
- Bit-reversed addressing, a special addressing mode useful for calculating FFTs
Program Flow

- Floating-point unit integrated directly into the datapath
- Pipelined architecture
- Highly parallel multiplier–accumulators (MAC units)
- Hardware-controlled looping, to reduce or eliminate the overhead required for looping operations
Instruction set

- Multiply–accumulate (MAC, including fused multiply–add, FMA) operations
- Instructions to increase parallelism: SIMD, VLIW, superscalar architecture
- Specialized instructions for modulo addressing in ring buffers and bit-reversed addressing mode for FFT cross-referencing
- Digital signal processors sometimes use time-stationary encoding to simplify hardware and increase coding efficiency.
General Multicore DSP
Multicore DSPs Classifications

- Heterogeneous and homogenous
- Hierarchical and mesh topologies
Multicore DSPs Examples

TI TNETV3020

Freescale MSC8156
Study Case: TI TMS320C6x

- TI TMS320C66x Processor
Application Specific Instruction Set Processors
Definition

- Application-Specific Instruction set Processor
- ASIP is a programmable architecture that is designed in a specific way to perform specific tasks better
Instruction Set

- The Application requirements and the architecture shapes the instruction-set format
- ASIP can use configuration registers with constant operands in addition to general purpose registers
- Instruction set:
  - Static
  - Configurable
Network Processors

- Evolution of networking systems
  - **First Generation (1980s):** GPP running network services at the application layer
  - **Second Generation (mid 1990s):** Semi-specialized hardware components & faster switching fabric
  - **Third Generation (late 1990s):** Utilization of ASIC in addition to micro controllers on each interface to accommodate excessive data flows
Network Processors

- Network applications
  - Table lookup
  - Pattern matching
  - Address translation
  - Queuing management
- Classifications
  - Data Plane
  - Control Plane
Network Processors

- Architecture
  - In 2003 there were more than 30 different proprietary devices sold as network processor*

Network Processors

- Alchemy Semiconductor, Augmented RISC

- This processor was basically augmented with special instructions and I/O interfaces to speed packet processing.
Network Processors

- Parallel Processors Plus Co-processors AMCC
- Parallel processors and coprocessors dedicated for packets processing tasks
Network Processors

- Hybrid Architectures
  - Parallel Pipelines of Homogeneous Processors (Cisco)
  - Pipeline of Parallel Heterogeneous Processors (EZchip)
Cisco QuantumFlow Processor (QFP)

- Announced in 2008
- A non-pipelined, multi core processor with centralized shared memory
- Capable of providing up to 100+ Gbps of packet processing bandwidth
QFP

- Packet Processor Engines (PPE)
- Buffering, Queuing and Scheduling Engine (BQS)
- ANSI-C based Software architecture
QFP

- Packet Processor Engines (PPE)
  - 40 x 4-way, 32-bit RISC Processor
  - Max clock speed of 1.2 GHz
  - 16 KB of layer 1 cache which is shared across all 4 threads of the same PPE
  - 2x256 KB layer 2 cache which are shared across 40 PPEs
  - Cache coherence is implemented at hardware level
  - 20 Mb SRAM
  - 800 MHz DDR memory
QFP

- Buffering, Queuing and Scheduling Engine (BQS)
  - 128,000 queues of Real-time hardware scheduling
  - 70 Mb SRAM
  - 800 MHz DDR memory.
Application Specific Integrated Circuits

Pradyumna Janga
History and Background

- The term 'ASIC' stands for 'Application-Specific Integrated Circuit'. An ASIC is basically an integrated circuit designed specifically for a special purpose or application.

- The first ASIC's were introduced in 1980. They used gate Array Technology known as uncommitted logic array or ULA's. They had few thousand gates; they were customized by varying the mask for metal interconnections. Thus, the functionality of such a device can be varied by modifying which nodes in the circuit are connected and which are not.
Classification

- **Full Custom**: The use of predefined masks for manufacturing leaves no option for circuit modification after fabrication.

- **Semi-Custom**: Unlike full-custom ASIC's, semi-custom ASIC's are designed to allow a certain degree of modification after the manufacturing process.

- **Structured or Platform**: The Degree of modification is higher.

- **Gate Array**: These use predefined pattern of transistors on silicon wafer.
Design Flow Overview
Applications

- An IC that encodes and decodes digital data using a proprietary encoding/decoding algorithm.
- A medical IC designed to monitor a specific human biometric parameter.
- An IC designed to serve a special function within a factory automation system.
- An amplifier IC designed to meet certain specifications not available in standard amplifier.
- An IC that's custom-made for a particular automated test equipment.
Crypto processor

- The special needs for secure communications are triggered not only in traditional sectors such as military and government services but also in all aspects of everyday life, in both business and private transactions.

- Software Encryption Methods could be a good choice since they have low cost and require a short development time. But the performance of Software is very low. This is the reason for evolution of Crypto Processors.

- Crypto Processors implement Hardware Encryption Systems which has higher performance when compared to the Software Methods and is also faster.
Implementation

- A Crypto Processor can be introduced either through ASIC or FPGA. Both of them support High Data Rates, although such designs are more time consuming and expensive compared with the software alternative.

- After the comparison between ASIC and FPGA implementations, it has been found that hardware solutions are better in most of the cases than the software alternatives. The main advantages of software are the low cost and the short time to market. Low performance is a fundamental drawback of software integrations.
## ASIC vs. FPGA

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<thead>
<tr>
<th></th>
<th>Software</th>
<th>FPGA</th>
<th>ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Performance</strong></td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td><strong>Power Consumption</strong></td>
<td>Depends</td>
<td>Very High</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Logic Integration</strong></td>
<td>Low</td>
<td>Low</td>
<td>High Integration</td>
</tr>
<tr>
<td><strong>Tool Cost</strong></td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Test Development Complexity</strong></td>
<td>Very Low</td>
<td>Very Low</td>
<td>High</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>High</td>
<td>Very Low</td>
<td>High</td>
</tr>
<tr>
<td><strong>Design Efforts</strong></td>
<td>Low-Medium</td>
<td>Low-Medium</td>
<td>High</td>
</tr>
<tr>
<td><strong>Time Consumed</strong></td>
<td>Short</td>
<td>Short</td>
<td>High</td>
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<tr>
<td><strong>Size</strong></td>
<td>Small-Medium</td>
<td>Small</td>
<td>Large</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>Fine</td>
<td>Fine</td>
<td>Fine</td>
</tr>
<tr>
<td><strong>Flexibility</strong></td>
<td>High</td>
<td>High</td>
<td>-</td>
</tr>
<tr>
<td><strong>Time to Market</strong></td>
<td>Short</td>
<td>Short</td>
<td>High</td>
</tr>
<tr>
<td><strong>Run Time Configuration</strong></td>
<td>-</td>
<td>High</td>
<td>-</td>
</tr>
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</table>
Architecture
Case Study: Hifn 7902

• The HiFn 7902 is a high performance pipelined security processor that integrates a math processor and a random number generator. These blocks provide additional features to support public key cryptography.

• The integrated algorithms support standard network security protocols. With a minimum amount of external logic, the Hifn 7902 can be interfaced with standard processors also.
Architecture

Internal Packet Memory
Packet buffers, commands, results, context

RNG
Public Key
Registers

Packet Engine
- Compression
- Padding
- Encryption

CPU Interface

RAM Interface (Optional)
Features of Hifn 7902

- Single chip multi-algorithm acceleration (LZS, 3-DES, SHA, Public Key & more)
- Public Key processing unit (2048-bit key lengths) and true random number generator
- Concurrent symmetric and Public Key processing
- Compression (LZS and MPPC)
- Uses SHA-1 and MD5 for Authentication
- Multi-protocol support: IPSec, IPPCP (IPCOMP), PPTP, L2TP, PPP, and IKE
Benefits of Hifn7902

- Offloads compute-intensive work from CPU.
- Delivers top security protection and breaks performance bottlenecks.
- Concurrent Operations.
- Improves system throughput.
- VPN at full broadband speeds.
Field Programmable Gate Arrays
Motivation

Automated Electricity Billing Design – (Prepaid Energy Meter)
Introduction

- An integrated circuit that can be used to implement any logical function.
- Contain programmable logic components called "logic blocks”.
- Simple logic gates like AND & XOR.
- Simple flip-flops or more complete blocks of memory
Spartan®-6 FPGA SP605 Kit

- Developing broadcast, wireless communications, automotive.
- Integration of hardware, software and IP.
- A flexible environment for higher-level system design
- Implement features such as PCI Express®, DVI, and/or DDR3.
Architecture

- An array of programmable logic blocks
  - General Logic
  - Memory
  - Multiplier blocks
  - Programmable routing fabric that allows blocks to be programmably interconnected
  - Input/output blocks that connect the chip to the outside world.

- The FPGA logic block consists of a
  - 4-input look-up table (LUT),
  - A flip flop.
  - Only one LUT output.
  - A clock input.
Interconnect

- Tree-Based interconnect - Two unidirectional networks.
- The downward network uses a “Butterfly Fat Tree” topology
  - DMSBs (Downward Miniswitch Blocks) -> LBs inputs.
  - The upward network connects LBs outputs to the DMSBs at each level.
- Used UMSBs (Upward MSBs) to allow LBs outputs to reach a large number of DMSBs and to reduce fan-out on feedback lines.
Memory

- **Arbiter:** Determines which port currently has priority for accessing the memory device.
- **Controller:** Requests made at the user interface -> necessary instructions and sequences required to communicate with the memory.
- **Datapath:** Handles the flow of write and read data between the memory device and the user logic.
- **Physical Interface (PHY):** Controller instructions -> actual timing relationships.
- **Calibration Logic:** Calibrates the PHY for optimal performance and reliability.

- Simplifies the task of interfacing Spartan devices.
- Higher performance, reduced power consumption, and faster development times.
FPGA’s in DSP

- **The SRAM-based FPGA**
  - Arithmetic, Fast Fourier Transform’s (FFT’s), convolutions, and other filtering algorithms.

- The parallel structures and arithmetic algorithms to minimize resources.

- **Distributed Arithmetic for array multiplication**
  - Increase data bandwidth and throughput

- **An In-System Programmable (ISP) FPGA**
  - This feature means a minimal chip solution can be transformed to perform multiple functions.
  - Suppose, for instance, one function is to compress a data stream in transmit mode and another function is to decompress the data in receive mode.
  - The FPGA can be reconfigured on-the-fly to switch, or toggle, from one function to another.
  - This capability of the FPGA adds functionality and processing power to a minimum-chip DSP system controlled with an internal or an external controller.
The Viterbi Decoder algorithm required 360 nsec [(24-clock cycles) x (15 nsec)] of processing time.

Limiting factors for this DSP-based design.

- First, the wait state requires two 15 nsec clock cycles for each memory access. Data Bus transfer requires 30 nsec for each data transaction.
- Secondly, each Add/Subtract and MUX stage had to be performed sequentially with additional wait-states. The Add/Subtract stages required four additional operations with multiple instructions.
FPGA Based Viterbi

- Process parallel data paths within the FPGA takes advantage of the parallel structures.
- The FPGA based Viterbi Decoder requires 135 nsec [(9-clock cycles)•(15 nsec)] of total processing time (this includes all of the outputs) compared to the 360 nsec required for the partial output data by the DSP.
- This enhancement equates to 37.5% of the original DSP processing time or 62.5% better processing performance.