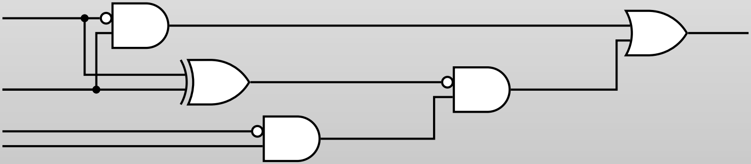
Garbled Circuits
For Secure Computation

Mike Rosulek
Oregon State University OSU



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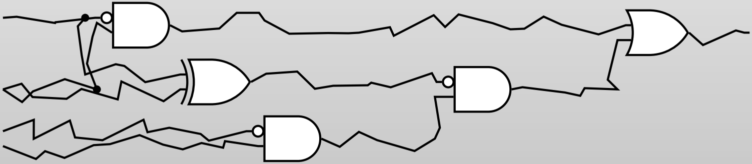

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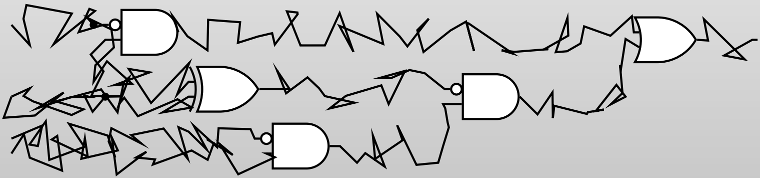


Roadmap

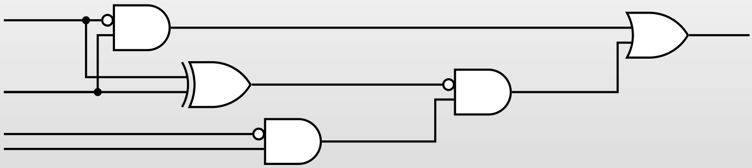
1 **Standard garbled circuits:** core concepts & constructions

- Yao's construction, security definitions, optimized constructions (row reduction, free XOR, half-gates)

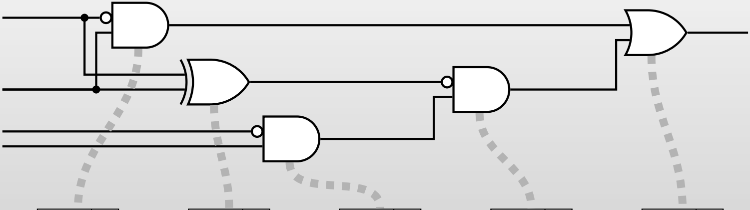
2 **New directions** beyond boolean circuits

- Garbled arithmetic circuits & RAM programs

Garbled circuit framework [Yao86]



Garbled circuit framework [Yao86]



0	0	0
0	1	1
1	0	0
1	1	0

0	0	0
0	1	1
1	0	1
1	1	0

0	0	0
0	1	1
1	0	0
1	1	0

0	0	0
0	1	1
1	0	0
1	1	0

0	0	0
0	1	1
1	0	1
1	1	1

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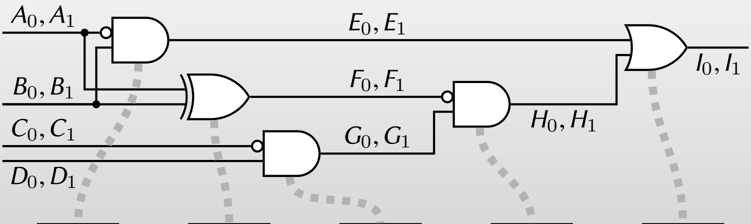

0	0	0
0	1	1
1	0	0
1	1	0

0	0	0
0	1	1
1	0	1
1	1	0

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0	1	1
1	0	0
1	1	0

0	0	0
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Garbling a circuit:

- Pick random **labels** W_0, W_1 on each wire

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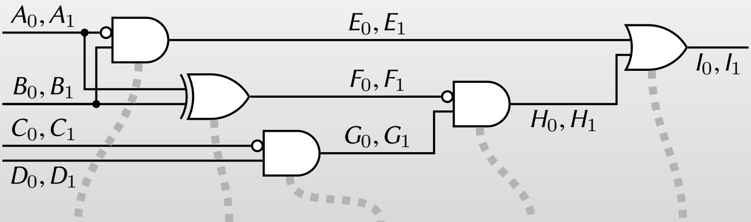

A_0	B_0	E_0
A_0	B_1	E_1
A_1	B_0	E_0
A_1	B_1	E_0

A_0	B_0	F_0
A_0	B_1	F_1
A_1	B_0	F_1
A_1	B_1	F_0

C_0	D_0	G_0
C_0	D_1	G_1
C_1	D_0	G_0
C_1	D_1	G_0

F_0	G_0	H_0
F_0	G_1	H_1
F_1	G_0	H_0
F_1	G_1	H_0

E_0	H_0	I_0
E_0	H_1	I_1
E_1	H_0	I_1
E_1	H_1	I_1

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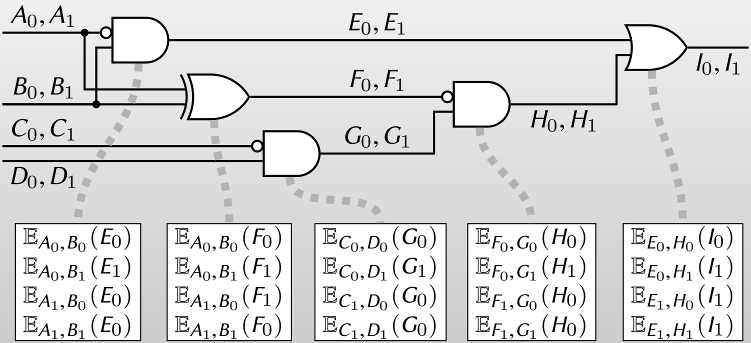

Garbling a circuit:

- Pick random **labels** W_0, W_1 on each wire
- "Encrypt" truth table of each gate

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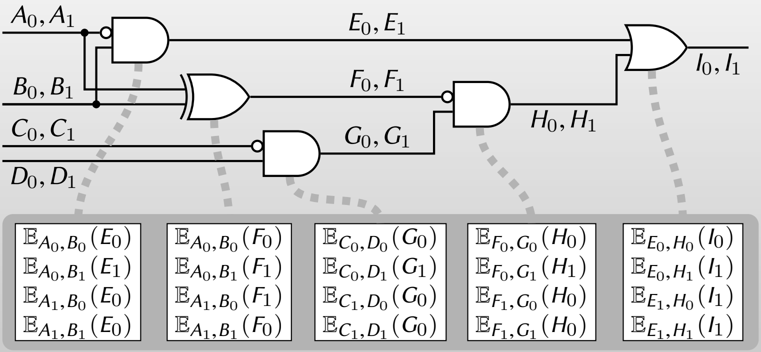

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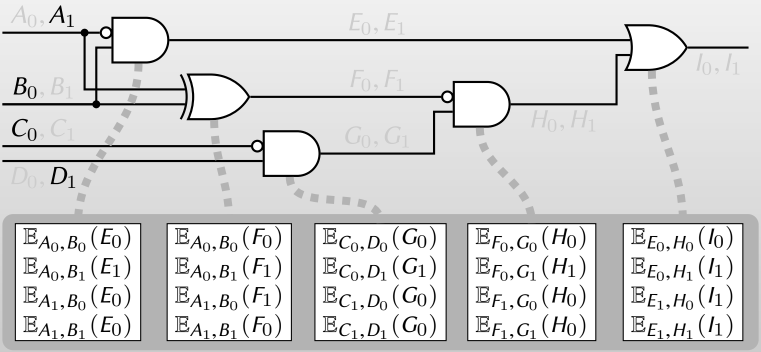

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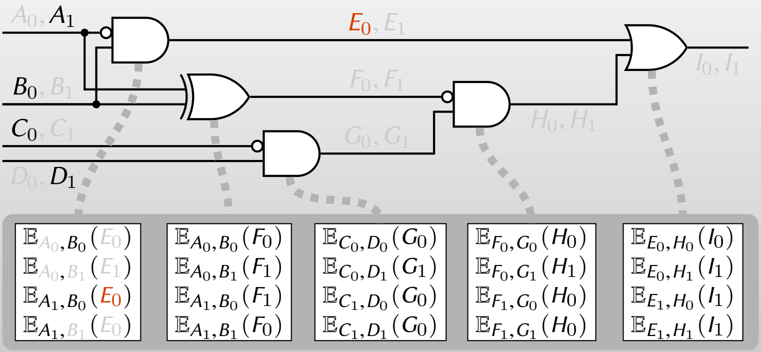

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Garbled evaluation:

- Only one ciphertext per gate is decryptable

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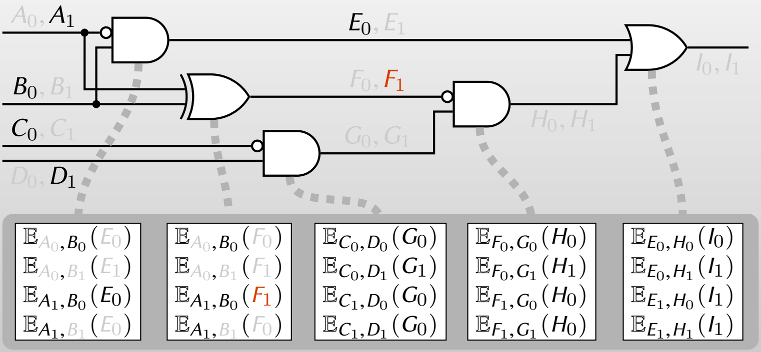

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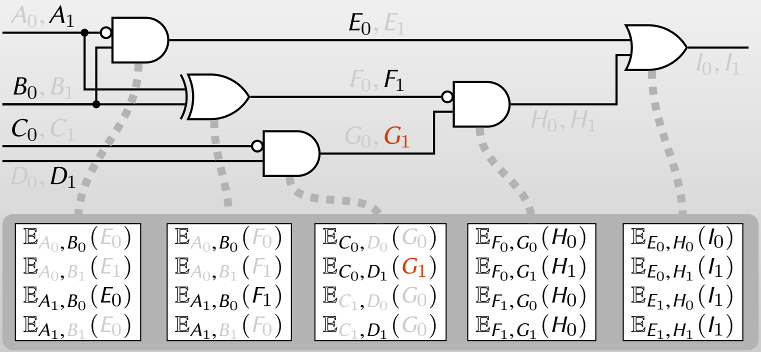

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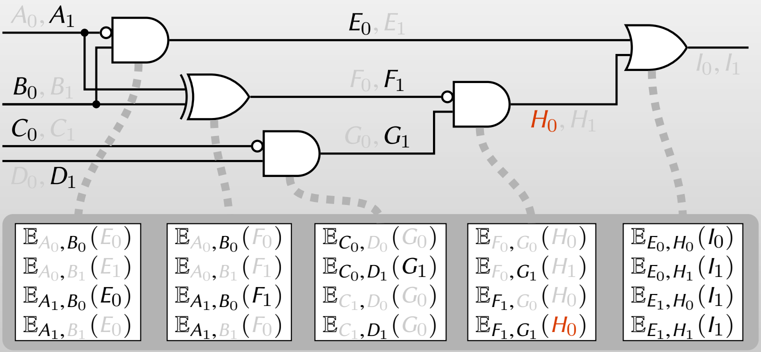

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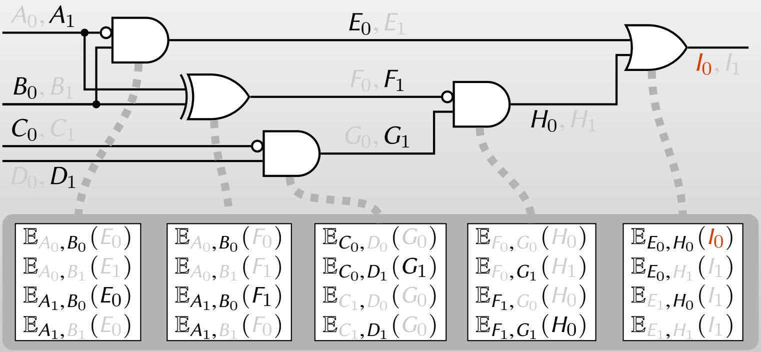

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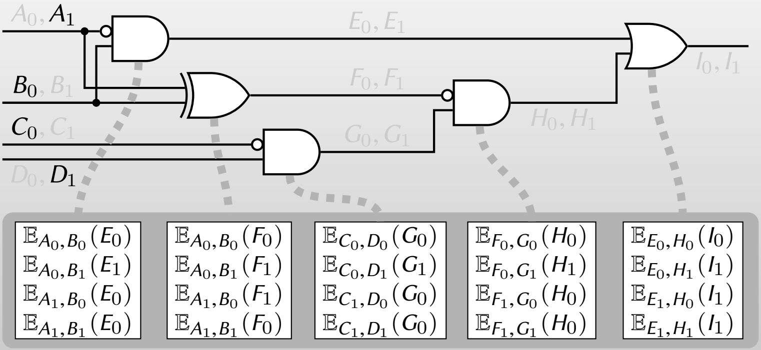
Syntax & Security (informal)



Key idea: Given garbled circuit + garbled input . . .

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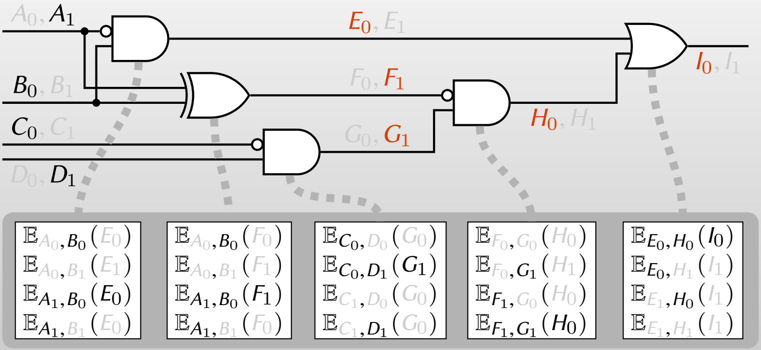

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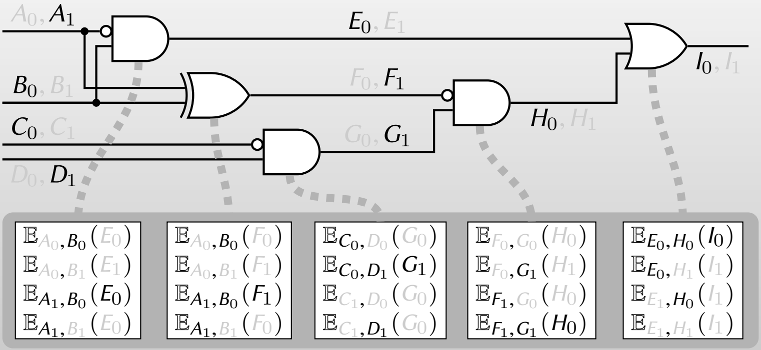
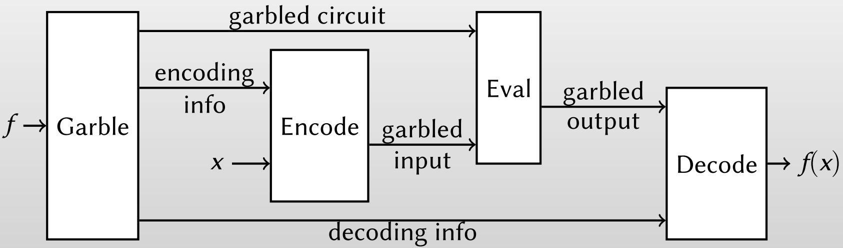


Key idea: Given garbled circuit + garbled input ...

- ... Only thing you can do is **(blindly) evaluate circuit** on that input
- Learn only 1 label per wire: hard to guess "complementary" label
- Seeing a single label hides logical value on wire, although ...
- Revealing both labels on *output wires* leaks *only* circuit output

Syntax & Security [BellareHoangRogaway12]



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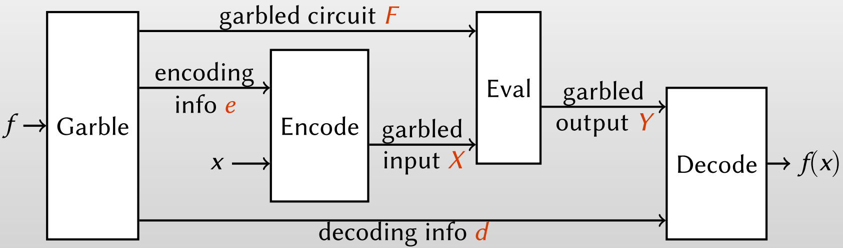

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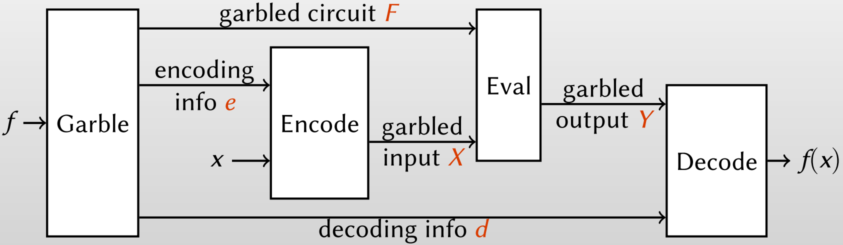

Formal security properties:

Privacy: (F, X, d) reveals nothing beyond f and $f(x)$

Obliviousness: (F, X) reveals nothing beyond f

Authenticity: given (F, X), hard to find $\widetilde{Y}$ that decodes $\notin \{f(x), \perp\}$

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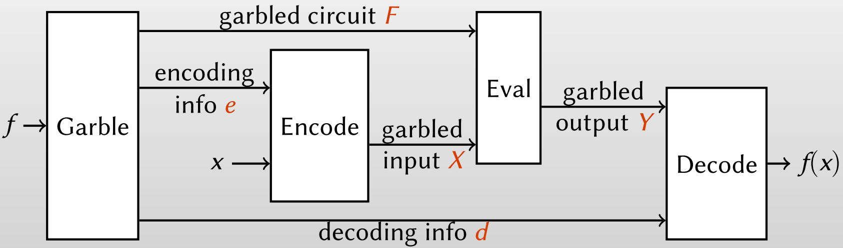

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Other interesting notions we won't discuss:

Adaptive security: choice of input can depend on *garbled* circuit

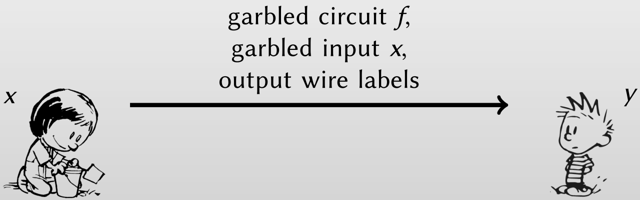
Gate-hiding: (F, X, d) reveals nothing beyond *topology of f* and $f(x)$

Yao's Protocol

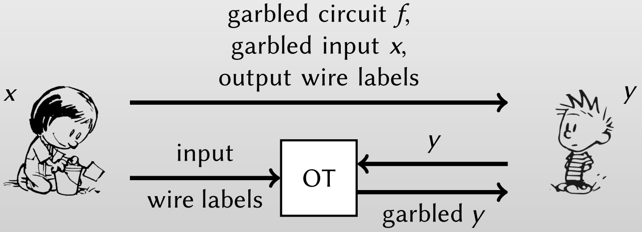
x

y

Yao's Protocol

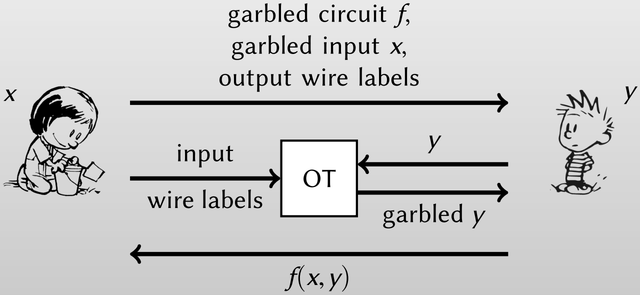


Yao's Protocol



- **Oblivious transfer:** Alice has m_0, m_1; Bob has b and learns m_b

Yao's Protocol



- **Oblivious transfer:** Alice has m_0, m_1; Bob has b and learns m_b
- Given garbled f + garbled inputs + all output labels ⇒ Bob learns **only** $f(x, y)$

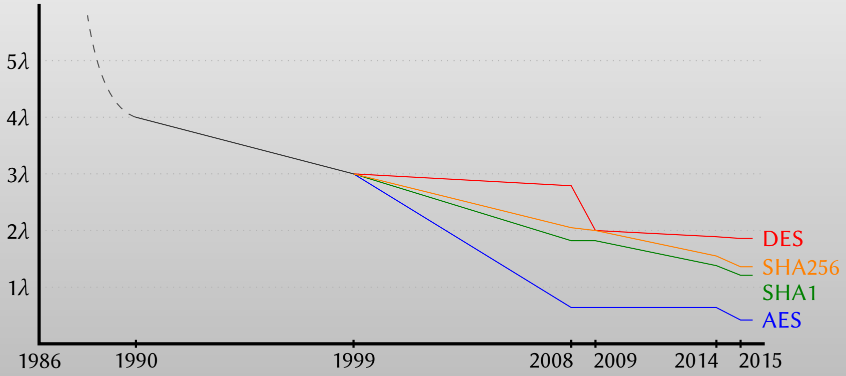
Optimizing garbled circuits

Size of garbled circuits . . .

. . . is the most important parameter

- Applications of garbled circuits are **network-bound**
- Garbled circuit computations are very fast (typically hardware AES)

Average bits per garbled gate



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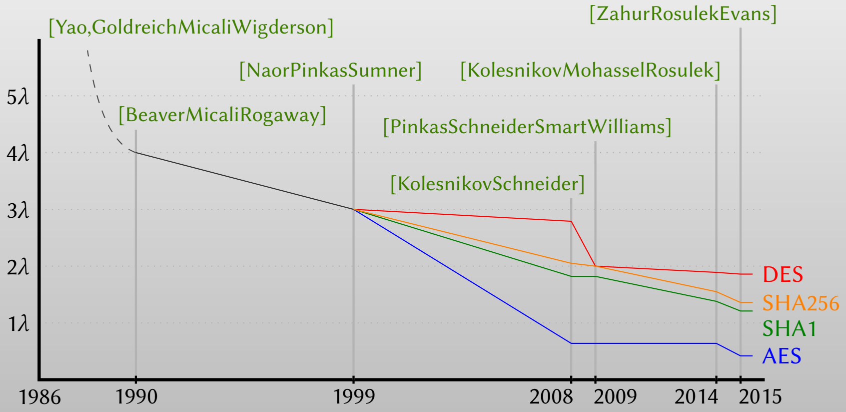
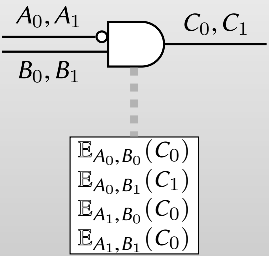


Ciphertext expansion [Yao86]



Position in this list leaks semantic value!

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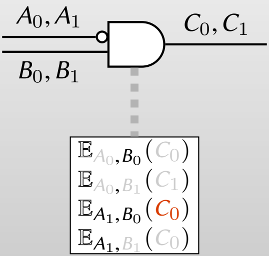

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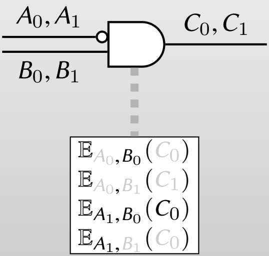

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$\Rightarrow$ Need to randomly permute ciphertexts

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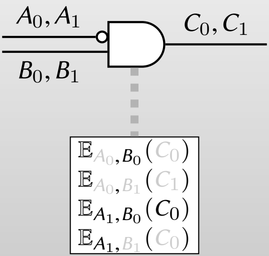

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$\Rightarrow$ Need to **detect** [in]correct decryption

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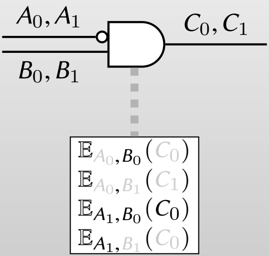


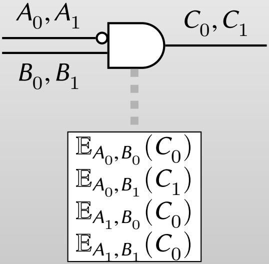
Position in this list leaks semantic value!

$\Rightarrow$ Need to randomly permute ciphertexts

$\Rightarrow$ Need to **detect** [in]correct decryption

$\Rightarrow$ Need encryption scheme with *ciphertext expansion* (size doubles)

Point-and-permute [BeaverMicaliRogaway90]



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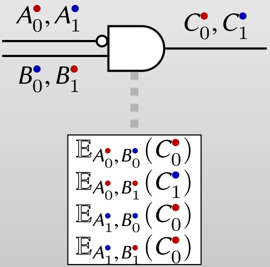

- Assign color bits • & • to wire labels
- Association between (•, •) ↔ (T, F) is random for each wire
- A wire label reveals its own color (e.g., as last bit)

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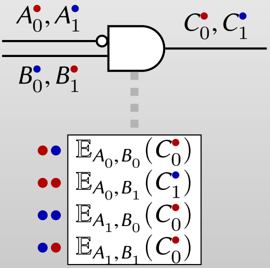

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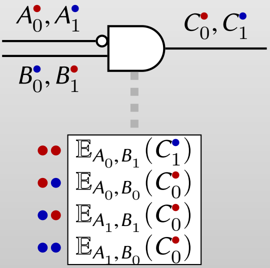

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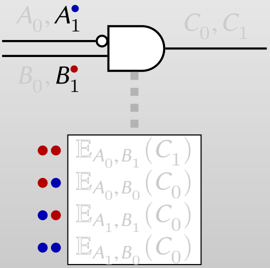

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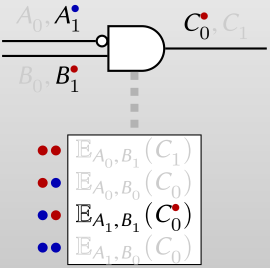

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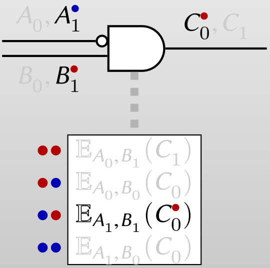


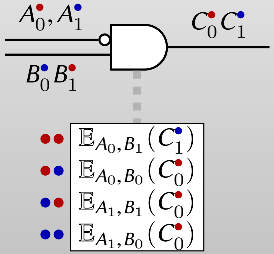
- Assign color bits ● & ● to wire labels
- Association between (●, ●) ↔ (T, F) is random for each wire
- A wire label reveals its own color (e.g., as last bit)
- Order the 4 ciphertexts canonically, by color of keys
- Evaluate by decrypting ciphertext indexed by your colors

No need for trial decryption ⇒ no need for ciphertext expansion!

Scoreboard

	size ($\times\lambda$)	garble cost	eval cost
Classical [Yao86,GMW87]	8	4	2.5
P&P [BeaverMicaliRogaway90]	4	4	1

Garbled Row Reduction [NaorPinkasSumner99]



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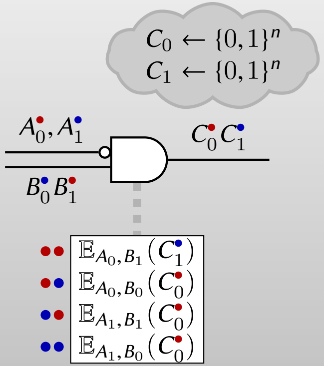

- Instead of choosing all wire labels uniformly . . .

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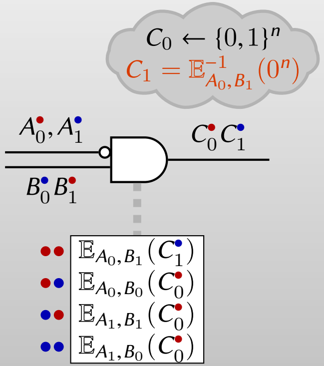

- Instead of choosing all wire labels uniformly ...
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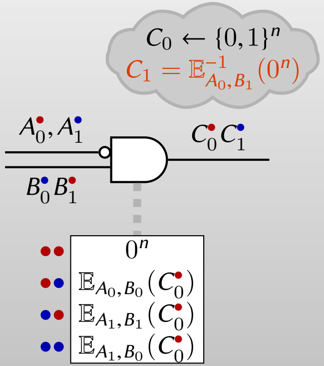

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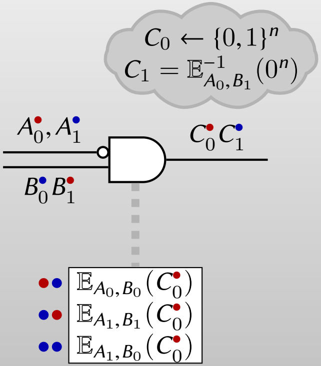

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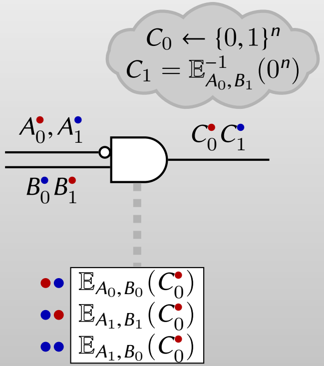
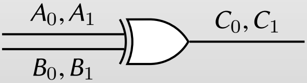


- Instead of choosing all wire labels uniformly ...
- ... choose so that first ciphertext is 0^n
- No need to include 1st ciphertext in garbled gate
- To evaluate, just imagine ciphertext 0^n if you have label combination ●●.

Scoreboard

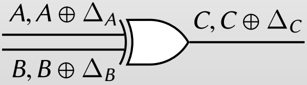
	size ($\times\lambda$)	garble cost	eval cost
Classical [Yao86,GMW87]	8	4	2.5
P&P [BeaverMicaliRogaway90]	4	4	1
GRR3 [NaorPinkasSumner99]	**3**	**4**	**1**

Free XOR [KolesnikovSchneider08]



- Define **offset of a wire** ≡ XOR of its two labels

Free XOR [KolesnikovSchneider08]



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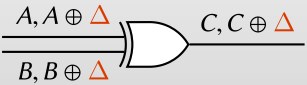

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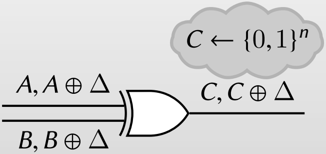

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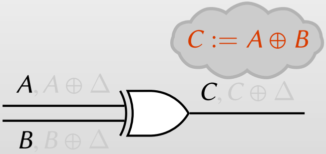

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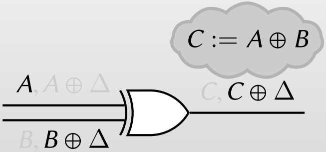

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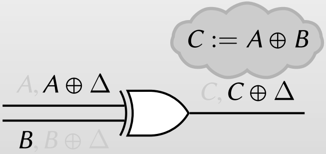

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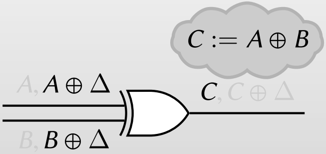

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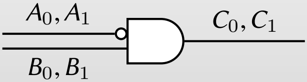
Scoreboard

	size ($\times\lambda$)		garble cost		eval cost	
	XOR	AND	XOR	AND	XOR	AND
Classical [Yao86,GMW87]	8	8	4	4	2.5	2.5
P&P [BeaverMicaliRogaway90]	4	4	4	4	1	1
GRR3 [NaorPinkasSumner99]	3	3	4	4	1	1
Free XOR [KolesnikovSchneider08]	**0**	**3**	**0**	**4**	**0**	**1**

Row reduction ×2 [PinkasSchneiderSmartWilliams09]

Garble a gate @ 2 ciphertexts per gate:



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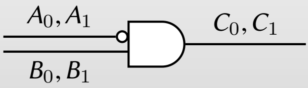

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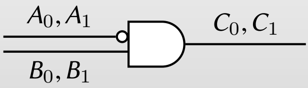

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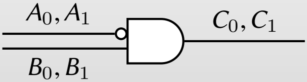

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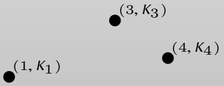

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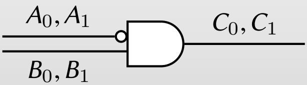

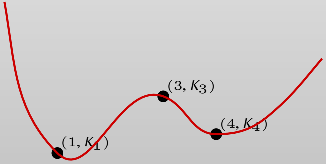

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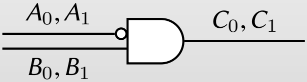

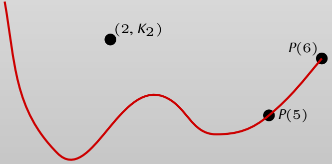

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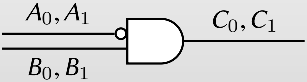

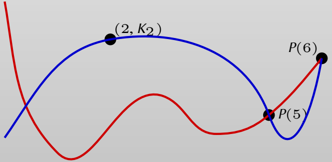

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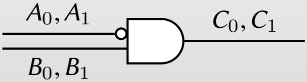

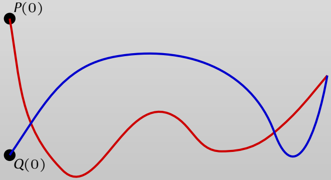

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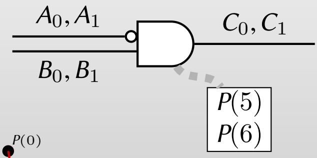

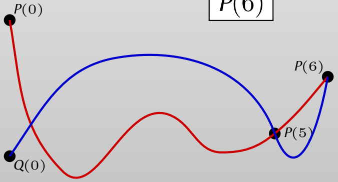

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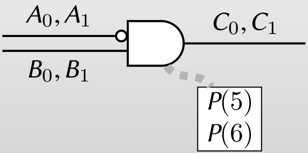

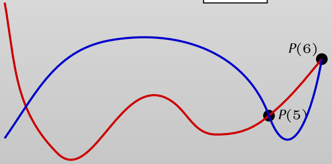

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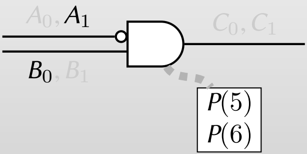

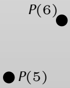

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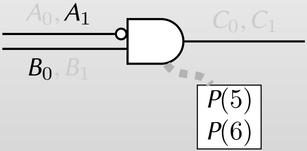

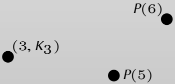

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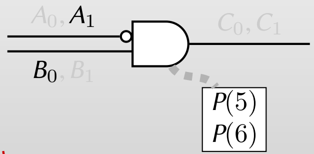

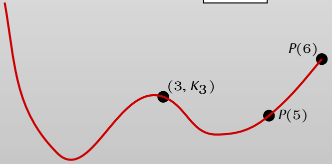

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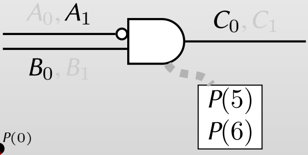

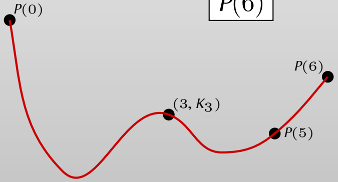

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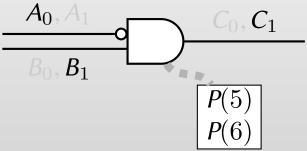
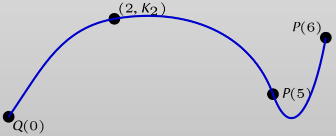


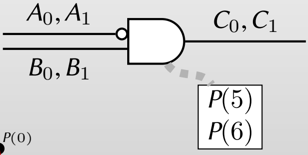


$P =$ uniq deg-2 poly thru $(1, K_1), (3, K_3), (4, K_4)$

$Q =$ uniq deg-2 poly thru $(2, K_2), (5, P(5)), (6, P(6))$

Row reduction ×2 [PinkasSchneiderSmartWilliams09]

$C_0 = P(0); C_1 = Q(0)$



Garble a gate @ 2 ciphertexts per gate:

Idea: Evaluator can know exactly one of:

$$K_1 = \mathbb{E}^{-1}_{A_0,B_0}(0^n) \rightsquigarrow \text{learn } C_0$$
$$K_2 = \mathbb{E}^{-1}_{A_0,B_1}(0^n) \rightsquigarrow \text{learn } C_1$$
$$K_3 = \mathbb{E}^{-1}_{A_1,B_0}(0^n) \rightsquigarrow \text{learn } C_0$$
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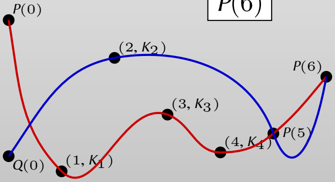

To evaluate a gate:

- Compute relevant K_i & interpolate:

$$(i, K_i), (5, P(5)), (6, P(6))$$

- Evaluate polynomial at zero

$P =$ uniq deg-2 poly thru $(1, K_1), (3, K_3), (4, K_4)$

$Q =$ uniq deg-2 poly thru $(2, K_2), (5, P(5)), (6, P(6))$

Scoreboard

	size ($\times\lambda$)		garble cost		eval cost	
	XOR	AND	XOR	AND	XOR	AND
Classical [Yao86,GMW87]	8	8	4	4	2.5	2.5
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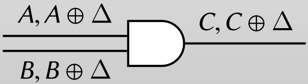
- Depending on circuit, either Free-XOR or GRR2 may be better
- Two techniques are **incompatible!** (can't guarantee $C_0 \oplus C_1 = \Delta$)

Half Gates [ZahurRosulekEvans15]

What if garbler knows in advance the truth value on one input wire?



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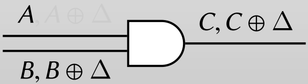

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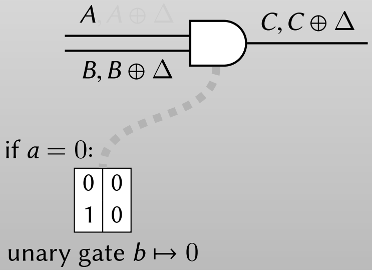

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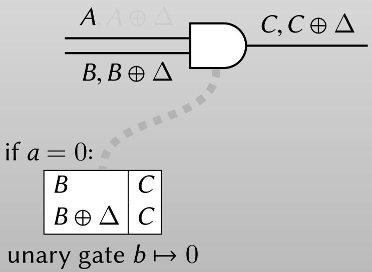

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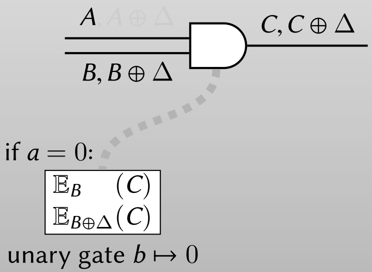

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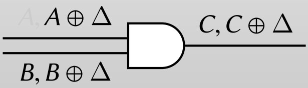

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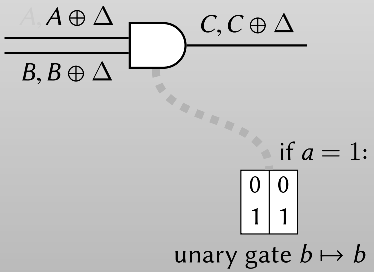

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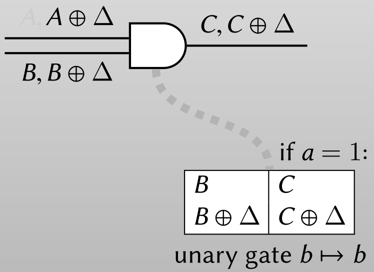

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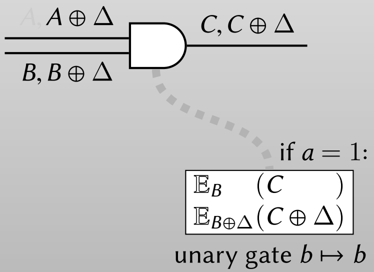

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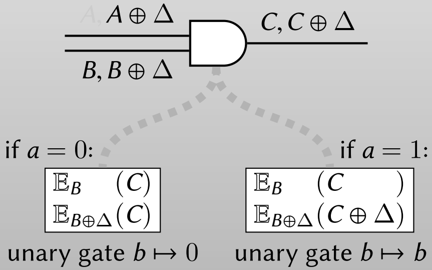

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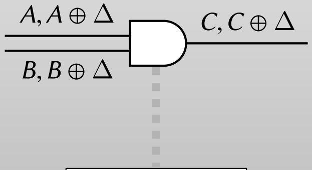

$$\begin{array}{l} \mathbb{E}_B(C) \\ \mathbb{E}_{B\oplus\Delta}(C \oplus a\Delta) \end{array}$$

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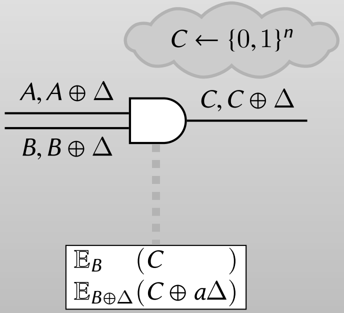

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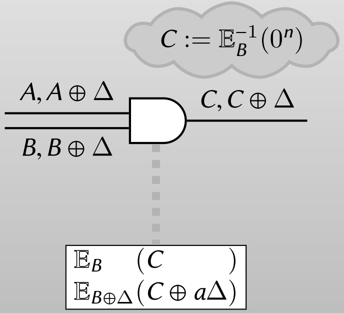

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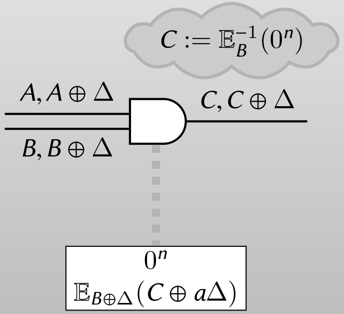

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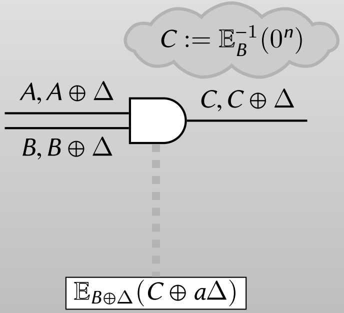

Fine print: permute ciphertexts with permute-and-point.

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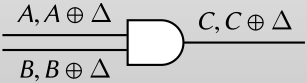

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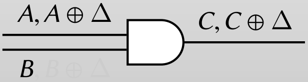

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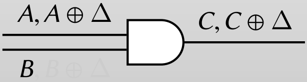

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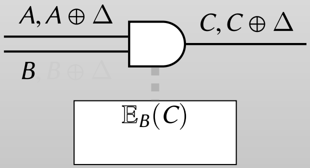

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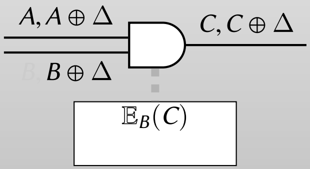

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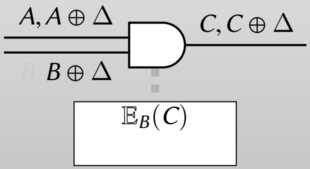

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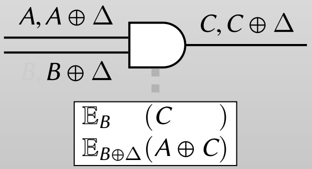

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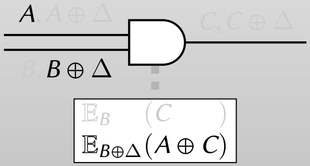

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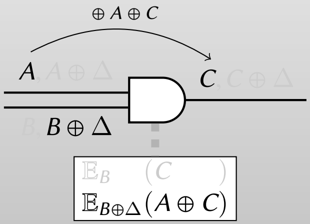

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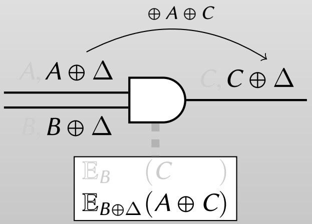

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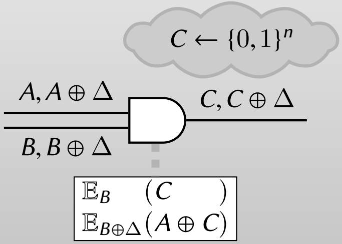

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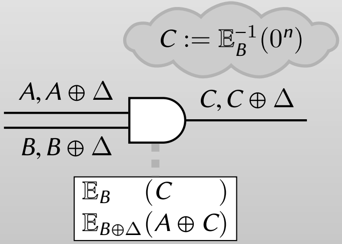

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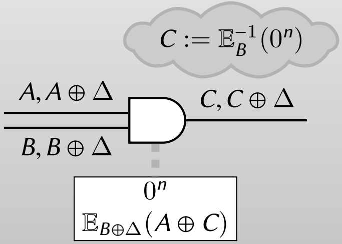

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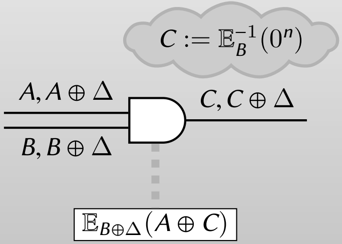

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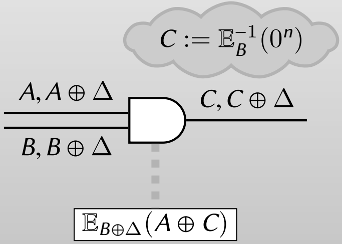

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Fine print: no need for permute-and-point here

Two halves make a whole!

$$a \wedge b$$

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$$a \wedge b = (a \oplus r \oplus r) \wedge b$$

- Garbler chooses random bit r

Two halves make a whole!

$$\begin{aligned} a \wedge b &= (a \oplus r \oplus r) \wedge b \\ &= [(a \oplus r) \wedge b] \oplus [r \wedge b] \end{aligned}$$

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- Garbler chooses random bit r
  - r = color bit of FALSE wire label A
- Arrange for evaluator to learn $a \oplus r$ in the clear
  - $a \oplus r$ = color bit of wire label evaluator gets (A or $A \oplus \Delta$)
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Half gates [ZahurRosulekEvans15]	**0**	**2**	**0**	**4**	**0**	**2**

Open Question

Can we do better than half-gates?

NO

[ZahurRosulekEvans15]

Can't garble an AND gate with < 2 ciphertexts

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. . . using "standard techniques" (details to follow)

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... but the construction doesn't compose with itself or Free-XOR

Open Question

Can we do better than half-gates?

in any useful way?

NO

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Lower bound in more detail

Theorem [ZahurRosulekEvans15]

A garbled AND gate requires 2 ciphertexts using "standard techniques."

Lower bound in more detail

Theorem [ZahurRosulekEvans15]

A garbled AND gate requires 2 ciphertexts using "standard techniques."

Standard techniques: *point-permute + calls to random oracle + everything else linear.*

Important: only the constructions, not adversary, must be linear!

Linear (gate) garbling: details

$\$_{\mathbb{F}}$

Garbler:

- samples field elements

Linear (gate) garbling: details

Garbler:

- samples field elements
- calls random oracle

Linear (gate) garbling: details

$\$_{\mathbb{F}}$

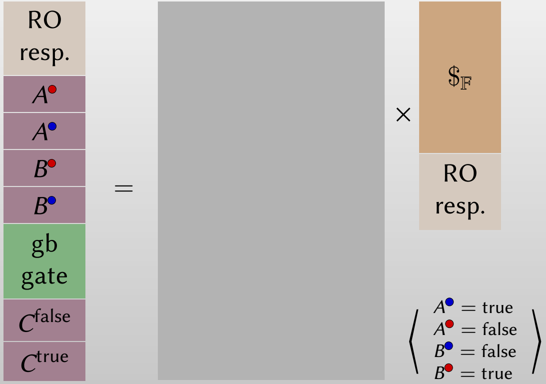
RO resp.

$$\left\langle \begin{array}{l} A^{\color{blue}\bullet} = \text{true} \\ A^{\color{red}\bullet} = \text{false} \\ B^{\color{blue}\bullet} = \text{false} \\ B^{\color{red}\bullet} = \text{true} \end{array} \right\rangle$$

Garbler:

- samples field elements
- calls random oracle
- picks secret "color mapping"

Linear (gate) garbling: details



Garbler:

- samples field elements
- calls random oracle
- picks secret “color mapping”
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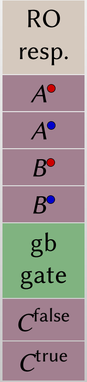
Linear (gate) garbling: details



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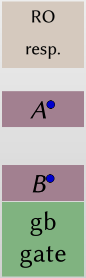

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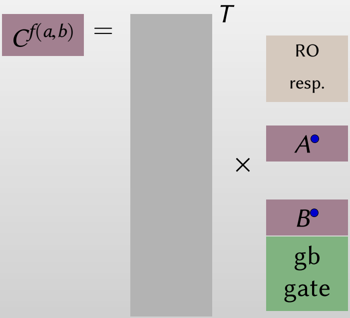

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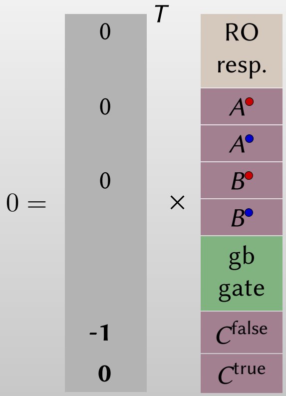

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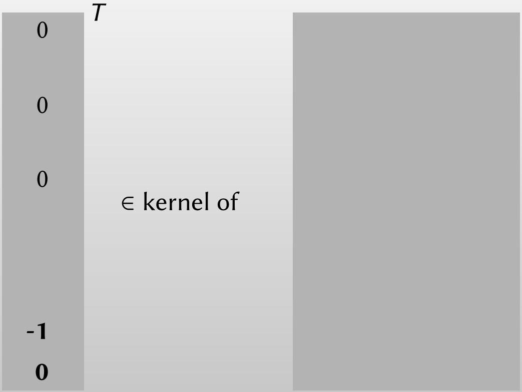

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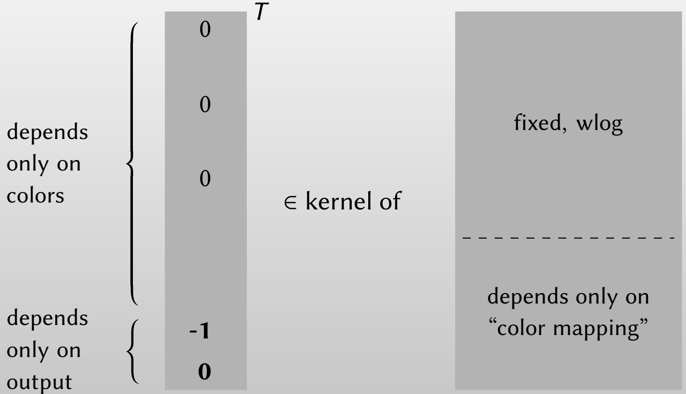

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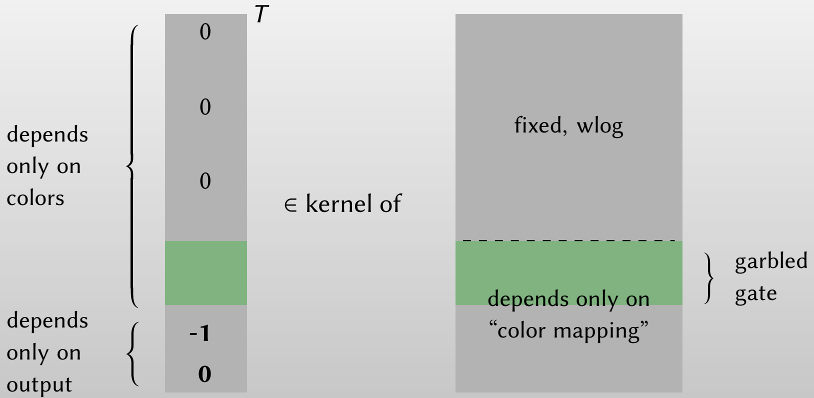

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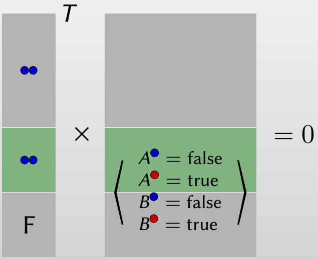

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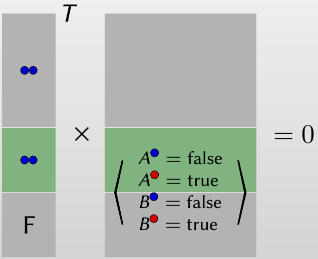

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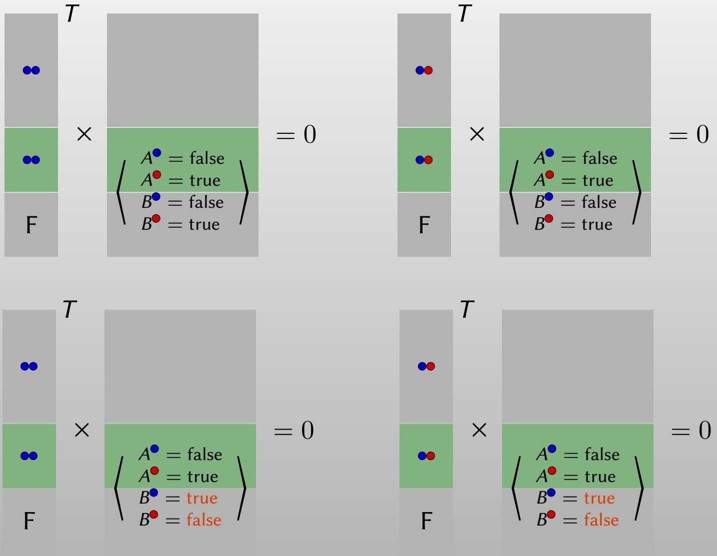

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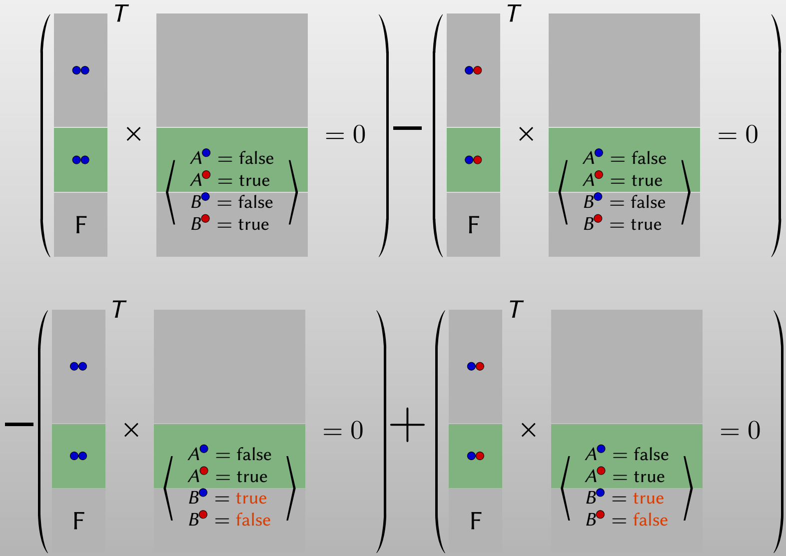

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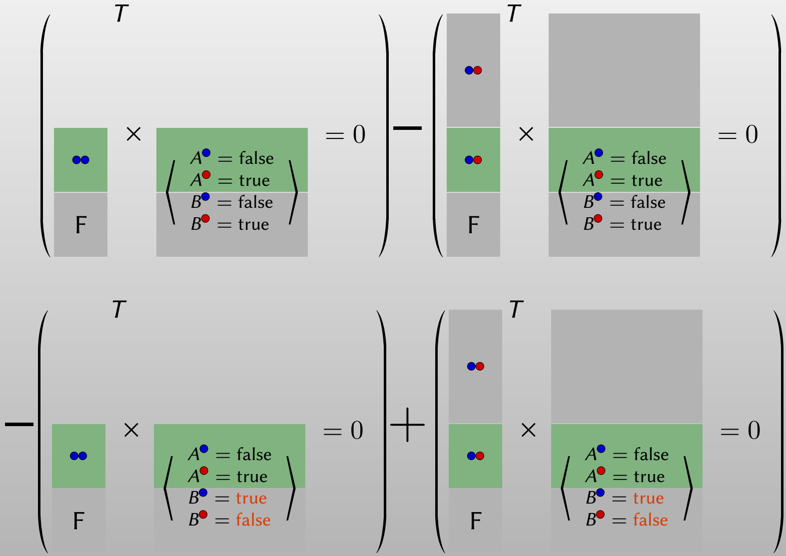

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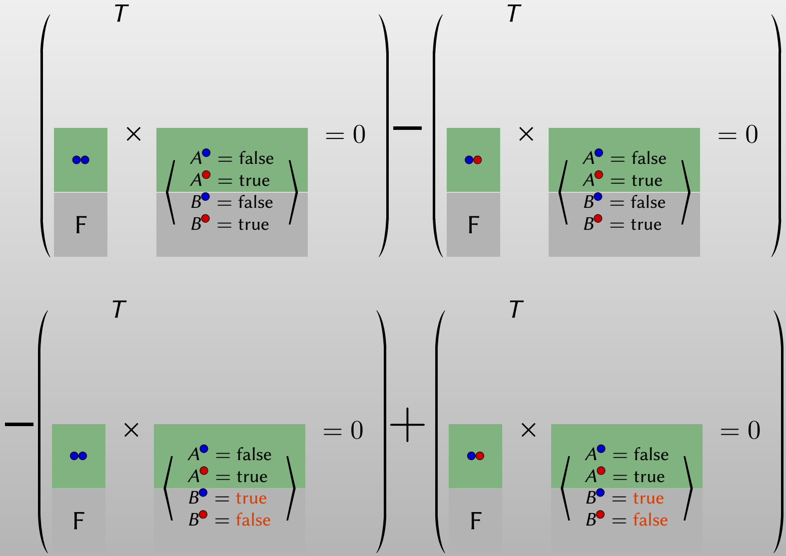

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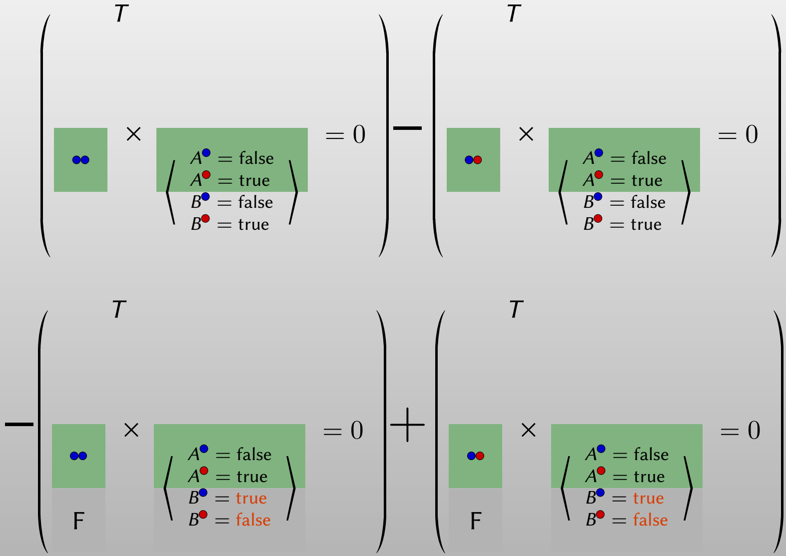

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$\Rightarrow$ $\dim(\text{rowspace}(M - M')) \geq 1$

$\Rightarrow$ M, M' have at least 2 rows

$\Rightarrow$ **garbled gate has at least 2λ bits**

Limitations of model

Limitation:
point-and-permute is sole source of non-linearity

Opportunity:
smaller GC by using alternatives to point-and-permute?
[BallMalkinRosulek16,KempkaKikuchiSuzuki16]

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model doesn't allow nested calls to random oracle	maybe nesting leads to smaller GC? e.g.: $H(H(A) \oplus B)$
linear!	maybe non-linear (but still practical) techniques lead to smaller GC? e.g., compute $GF(2^\lambda)$-inverse of a wire label

How to circumvent lower bound

[KempkaKikuchiSuzuki16]: indirection between color bits & non-linearity

- Based on color bits, evaluator decrypts appropriate **1-bit ciphertext**
- 1-bit payload determines **choice of linear combination**

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Neither construction is **self-composable**:

- Input wire labels must have special form: $(A, A+\Delta), (B, B+\Delta)$
- Garbled gate produces output labels that don't have special form

Summary

	size ($\times\lambda$)		garble cost		eval cost	
	XOR	AND	XOR	AND	XOR	AND
Classical [Yao86,GMW87]	8	8	4	4	2.5	2.5
P&P [BeaverMicaliRogaway90]	4	4	4	4	1	1
GRR3 [NaorPinkasSumner99]	3	3	4	4	1	1
Free XOR [KolesnikovSchneider08]	0	3	0	4	0	1
GRR2 [PinkasSchneiderSmartWilliams09]	2	2	2	2	1	1
Half gates [ZahurRosulekEvans15]	0	2	0	4	0	2

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Your next great idea?	0	1				

Can we do better than half-gates in any useful way?

Roadmap

1 **Standard garbled circuits:** core concepts & constructions

- Yao's construction, security definitions, optimized constructions (row reduction, free XOR, half-gates)

2 **New directions** beyond boolean circuits

- Garbled arithmetic circuits & RAM programs

Beyond Boolean Circuits

What about all the interesting things that are clunky to write as a boolean circuit?

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What about all the interesting things that are clunky to write as a boolean circuit?

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- New generalizations of garbled circuit constructions
- Improved garbling for arithmetic computations
- Improved garbling for high-fan-in boolean computations

Generalized Free XOR

Free XOR:

Wire carries a *truth value* from $\{0,1\}$

Wire labels are bit strings $\{0,1\}^\lambda$.

Global wire-label-offset $\Delta \in \{0,1\}^\lambda$

FALSE wire label is A
TRUE wire label is $A \oplus \Delta$

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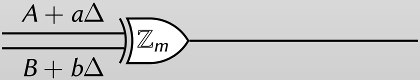

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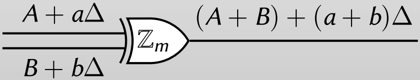

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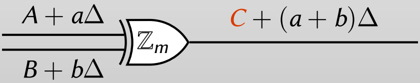

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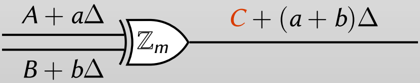

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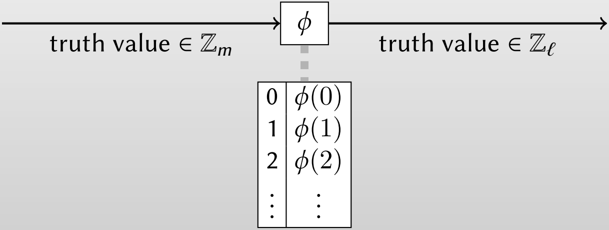
- Free multiplication by public constant c, if $\gcd(c, m) = 1$

Garbling unary gates



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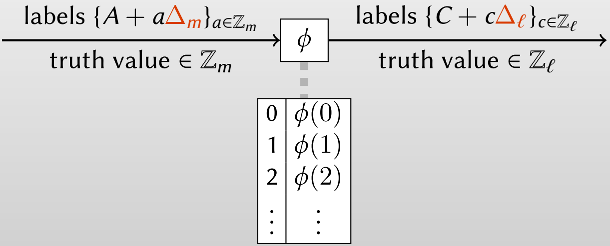

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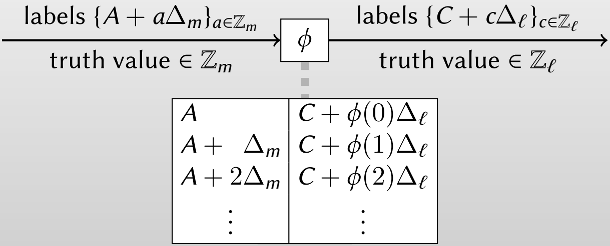

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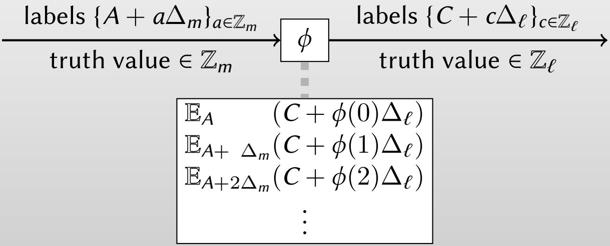

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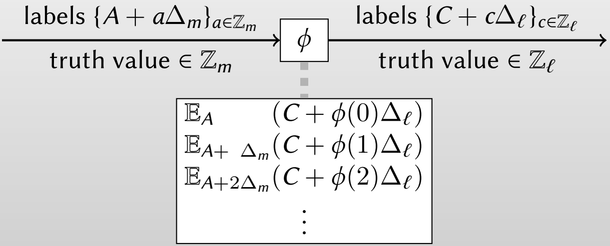

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- $m - 1$ using standard row reduction technique

Generalized garbling tools

We can efficiently garble any computation/circuit where:

- Each wire has a preferred modulus $\mathbb{Z}_m$
  - $\Rightarrow$ Wire-label-offset Δ_m global to all $\mathbb{Z}_m$-wires
- Addition gates: all wires touching gate have same modulus
  - $\Rightarrow$ Garbling cost: **free**
- Mult-by-constant gates: input/output wires have same modulus
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Better basis for many computations than traditional boolean circuits!

Arithmetic computations

Example Scenario

Securely compute linear optimization problem on 32-bit values.

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	cost (# ciphertexts)
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Using generalized garbling techniques:

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- Multiplication mod m costs $O(m)$ ciphertexts!

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Arithmetic computations

$$\text{instead of } \mathbb{Z}_{4294967296}$$

$$\downarrow$$

$$\text{use } \mathbb{Z}_{6469693230}$$

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$$\text{use } \mathbb{Z}_{6469693230} = \mathbb{Z}_{2 \cdot 3 \cdot 5 \cdot 7 \cdots 29}$$

Arithmetic computations

CRT residue number system!

- Generalized garbling scheme supports many moduli in same circuit
- Represent 32-bit integer x as $x \% 2,\ x \% 3,\ x \% 5, \ldots,\ x \% 29$
- Do all arithmetic in each residue (each with small modulus)

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works well for arithmetic on $\mathbb{Z}$, unless you like working mod 6469693230

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Example Scenario

Securely compute boolean circuit with **high-fan-in threshold gates.**

- fan-in-100: AND, OR, majority, threshold, etc.

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- fan-in-100: AND, OR, majority, threshold, etc.

"Standard approach"

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- Garble with half-gates (AND costs 2, XOR costs 0)

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Securely compute boolean circuit with **high-fan-in threshold gates.**

- fan-in-100: AND, OR, majority, threshold, etc.

"Standard approach"

- Express threshold gates in terms of fan-in-2 gates
- Garble with half-gates (AND costs 2, XOR costs 0)

	cost (# ciphertexts)
AND/OR	198
majority	948

High fan-in computations

Idea: AND is unary function of a sum

$$\text{AND}(x_1, \ldots, x_{100}) = [\sum x_i \stackrel{?}{=} 100]$$

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- Represent each bit on a $\mathbb{Z}_{101}$-wire
- Cost to garble sum in $\mathbb{Z}_{101}$ is **free**
- "$v \stackrel{?}{=} 100$" is simple $\mathbb{Z}_{101}$-unary gate $\Rightarrow$ cost = 100

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Same logic for $\text{MAJ}(x_1, \ldots, x_{100}) = [\sum_i x_i \stackrel{?}{>} 50]$

High fan-in computations

instead of $\mathbb{Z}_{101}$

$\downarrow$

use $\mathbb{Z}_{210}$

High fan-in computations

$$\text{instead of } \mathbb{Z}_{101}$$

$$\downarrow$$

$$\text{use } \mathbb{Z}_{210} = \mathbb{Z}_{2\cdot 3\cdot 5\cdot 7}$$

High fan-in computations

Insight: take advantage of multiple moduli

$$\mathsf{AND}(x_1,\ldots,x_{100}) = [\sum x_i \stackrel{?}{=} 100] = [\sum x_i \stackrel{?}{\equiv} 100 \pmod{210}]$$

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- Represent each bit redundantly mod 2, mod 3, mod 5, . . .

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- Represent each bit redundantly mod 2, mod 3, mod 5, ...
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	standard	better	**CRT**
AND/OR	198	100	**21**
majority	948	100	

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Circumventing lower bound

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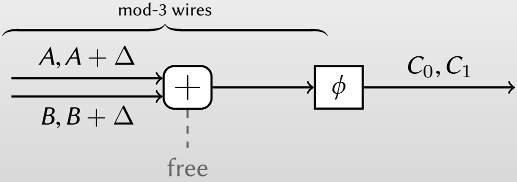
What about case of fan-in 2 AND gate?



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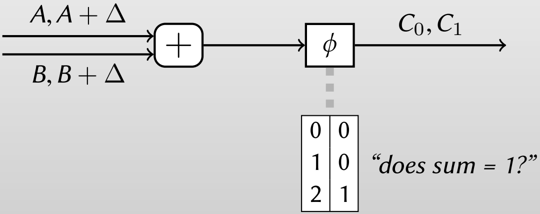

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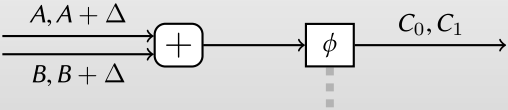

$A + B$	C_0
$A + B + \Delta$	C_0
$A + B + 2\Delta$	C_1

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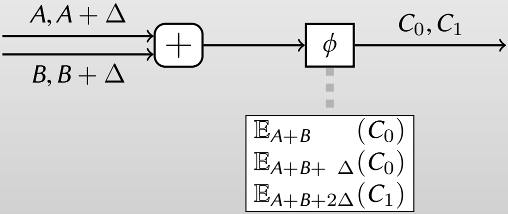

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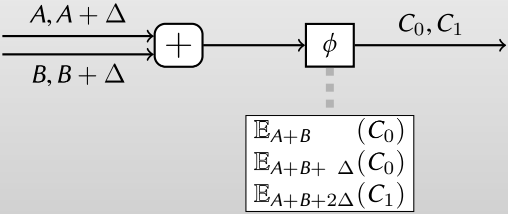

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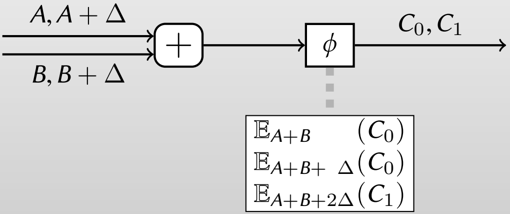

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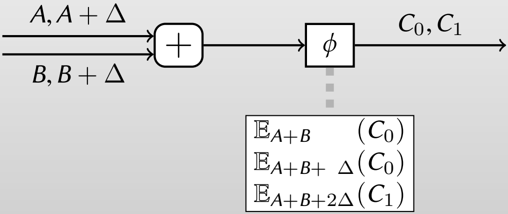
- Stopping there allows **composability**: $C_1 = C_0 + \Delta$
- Instead, further choose C_1 so that remaining 2 ciphertexts are equal
  - $\Rightarrow$ don't need to send both [PinkasSchneiderSmartWilliams09,GueronLindellNofPinkas15]

Circumventing lower bound

What about case of fan-in 2 AND gate? Can garble with 1 ciphertext!



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Challenges:

State of the art:

"If values are represented in CRT form then garbled operations are cheap."

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But doesn't it cost something to get values into CRT form??

Dealing with CRT

Claim:

It's **not hard** to convert into CRT representation $\mathbb{Z}_{p_1} \times \mathbb{Z}_{p_2} \times \cdots \times \mathbb{Z}_{p_k}$

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From binary $b_n b_{n-1} \cdots b_1 b_0$:

- For all i, j, use unary gate $b_i \mapsto b_i \pmod{p_j}$ (1 ciphertext each)
- For all j, add to obtain $\sum_i b_i 2^i \pmod{p_j}$ (**free**)
- Total cost = (# primes) × (# bits) (e.g., 320 ciphertexts for 32 bits)

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At the input level (e.g., OTs in Yao): (similar to [Gilboa99,KellerOrsiniScholl16])

- Outside of the circuit, convert plaintext input into CRT form
- Convert $\mathbb{Z}_{p_j}$-residue to binary, and transfer it using $\lceil \log p_j \rceil$ OTs
- Total cost: $\sum_j \log p_j$ OTs (e.g., 37 OTs for 32-bit values)

Open Problems

Improve the cost of any of these:

- **Comparing** two CRT-encoded values
- Converting CRT representation to binary
- Integer division
- Modular reduction different than the CRT composite modulus (e.g., garbled RSA)

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Comparing CRT values

CRT view of $\mathbb{Z}_{2\cdot 3\cdot 5\cdot 7}$:

0 0 0 0	0
1 1 1 1	1
2 2 2 0	2
3 3 0 1	3
4 4 1 0	4
5 0 2 1	5
6 1 0 0	6
0 2 1 1	7
$\vdots$	$\vdots$
1 4 2 1	29
2 0 0 0	30
$\vdots$	$\vdots$

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Theorem

CRT representation sucks for comparisons!

Comparing CRT values

CRT view of $\mathbb{Z}_{2\cdot 3\cdot 5\cdot 7}$:

$$\begin{array}{c|l} 0\ 0\ 0\ 0 & 0 \\ 1\ 1\ 1\ 1 & 1 \\ 2\ 2\ 2\ 0 & 2 \\ 3\ 3\ 0\ 1 & 3 \\ 4\ 4\ 1\ 0 & 4 \\ 5\ 0\ 2\ 1 & 5 \\ 6\ 1\ 0\ 0 & 6 \\ 0\ 2\ 1\ 1 & 7 \\ \vdots & \vdots \\ 1\ 4\ 2\ 1 & 29 \\ 2\ 0\ 0\ 0 & 30 \\ \vdots & \vdots \end{array}$$

$$\begin{array}{r|l} 0 & 0 \\ 1 & 1 \\ 1\ 0 & 2 \\ 1\ 1 & 3 \\ 2\ 0 & 4 \\ 2\ 1 & 5 \\ 1\ 0\ 0 & 6 \\ 1\ 0\ 1 & 7 \\ \vdots & \vdots \\ 4\ 2\ 1 & 29 \\ 1\ 0\ 0\ 0 & 30 \\ \vdots & \vdots \end{array}$$

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Primorial Mixed Radix (PMR)

0	0
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Approach for comparisons

CRT values given

↓

Convert both CRT values to PMR

↓

Compare PMR (simple L→R scan)

Approach for comparisons

CRT values given

$\downarrow$

Convert both CRT values to PMR

PMR representation of x:

$$\ldots, \quad \left\lfloor \frac{x}{2 \cdot 3 \cdot 5} \right\rfloor \% \, 7, \quad \left\lfloor \frac{x}{2 \cdot 3} \right\rfloor \% \, 5, \quad \left\lfloor \frac{x}{2} \right\rfloor \% \, 3, \quad \lfloor x \rfloor \% \, 2$$

$\downarrow$

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CRT values given

$\downarrow$

Convert both CRT values to PMR

Simple building block:

$$(x\%p,\ \ x\%q) \mapsto \left\lfloor \frac{x}{p} \right\rfloor \%q$$

allows you to compute PMR representation of x:

$$\ldots,\ \ \left\lfloor \frac{x}{2\cdot 3\cdot 5} \right\rfloor \%\, 7,\ \ \left\lfloor \frac{x}{2\cdot 3} \right\rfloor \%\, 5,\ \ \left\lfloor \frac{x}{2} \right\rfloor \%\, 3,\ \ \lfloor x \rfloor \%\, 2$$

$\downarrow$

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$(x\%p,\ x\%q) \mapsto \lfloor x/p \rfloor \% q$

x	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$x \% 3$	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
$x \% 5$	0	1	2	3	4	0	1	2	3	4	0	1	2	3	4

$\lfloor x/3 \rfloor \% 5$	0	0	0	1	1	1	2	2	2	3	3	3	4	4	4

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$x\%3 - x\%5$	0	0	0	-3	-3	2	-1	-1	-1	-4	1	1	-2	-2	-2

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$(x\%3 - x\%5)\%7$	0	0	0	4	4	2	6	6	6	3	1	1	5	5	5
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    - "Project" $x\%3$ and $x\%5$ to $\mathbb{Z}_7$ wires
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   - Apply unary projection:

$$0 \mapsto 0 \quad 2 \mapsto 1 \quad 4 \mapsto 1 \quad 6 \mapsto 2$$
$$1 \mapsto 3 \quad 3 \mapsto 3 \quad 5 \mapsto 4$$

Approach for comparisons

1. General $\boxed{(x\%p,\ x\%q) \mapsto \lfloor x/p \rfloor \%q}$ gadget costs $\sim 2p + 2q$ ciphertexts
2. PMR conversion requires this gadget between *all pairs* of primes
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Operations on 32-bit integers:

	boolean	CRT
addition	62	0
multiplication by public constant	758	0
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squaring, cubing, etc	1864	119

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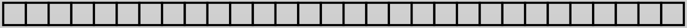
Beyond circuits altogether



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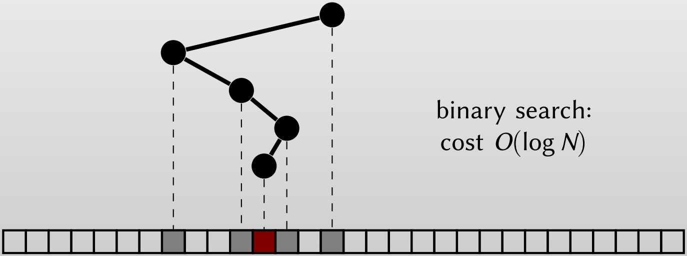

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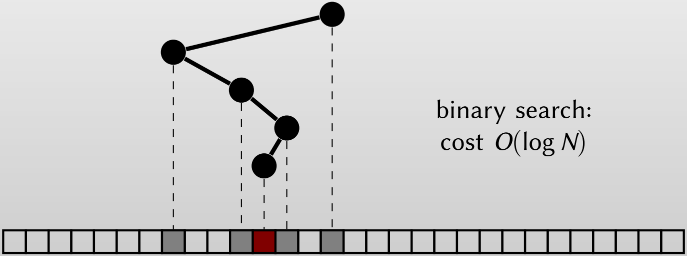

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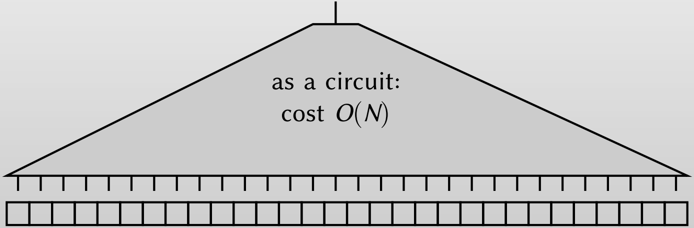

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RAM programs

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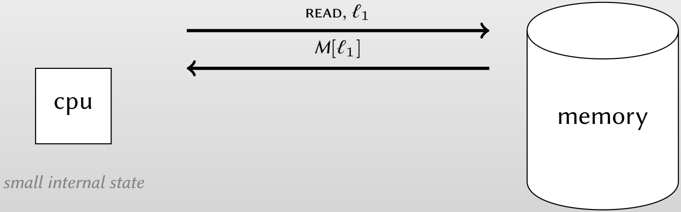

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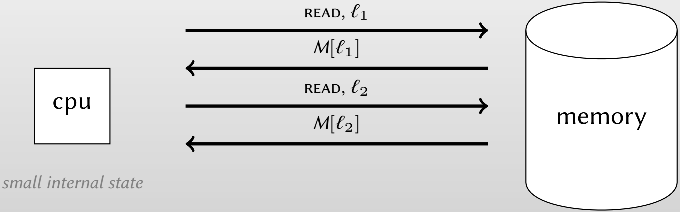

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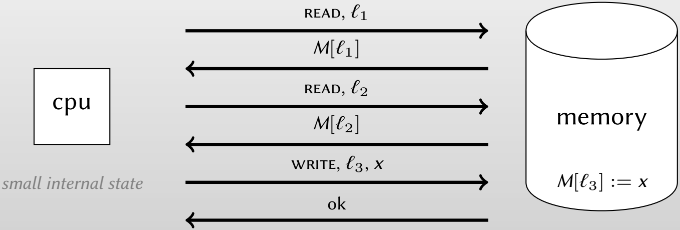

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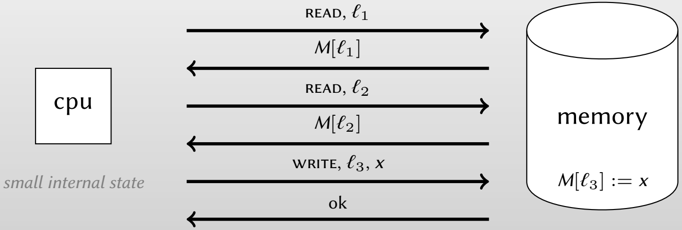
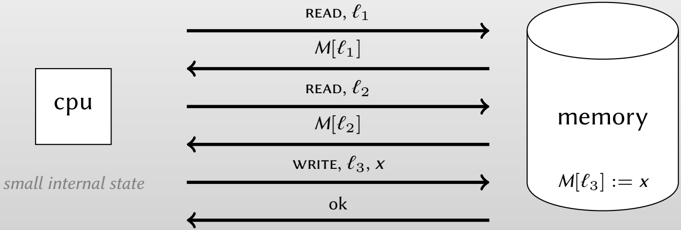


How to garble a RAM computation?

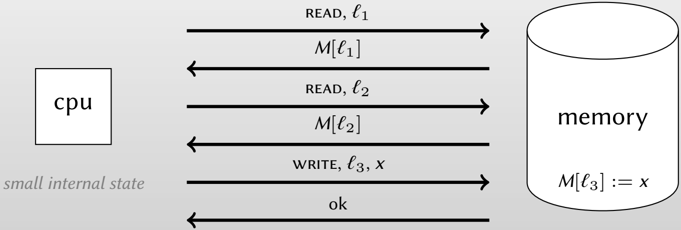
RAM programs



How to garble a RAM computation with cost

$\sim |mem| + |cpu| \cdot$ [# mem accesses] ?

RAM programs



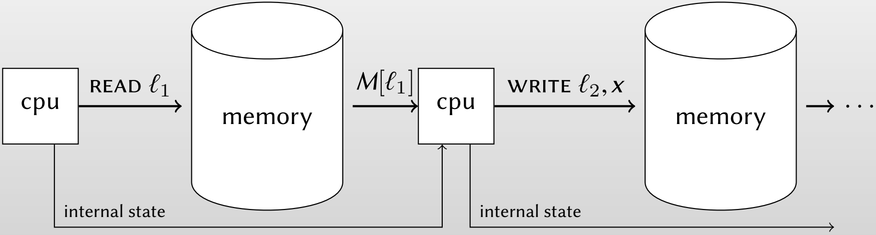
How to garble a RAM computation with cost

$\sim |mem| + |cpu| \cdot$ [# mem accesses] ?

Example: t binary searches

- Naïve cost: $\sim N \cdot t$
- Desired cost: $\sim N + t \cdot \log N$

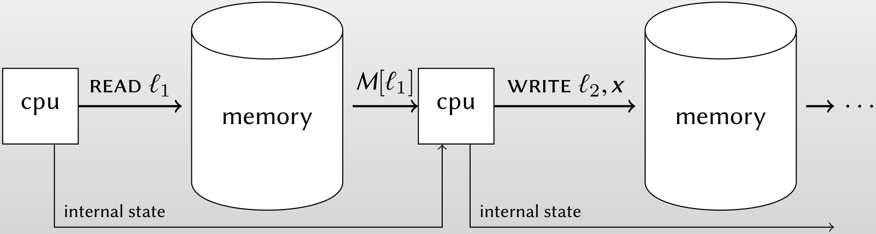
Challenges for Garbled RAM



Garbled circuits are single-use!

$\Rightarrow$ garble *t* separate copies of CPU circuit

Challenges for Garbled RAM



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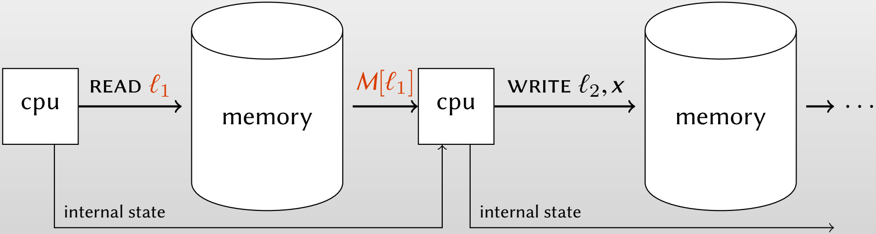
⇒ garble t separate copies of CPU circuit

Memory accesses can depend on private data!

⇒ Compile to **oblivious RAM** (ORAM) [GoldreichOstrovsky96]

Challenges for Garbled RAM



Garbled circuits are single-use!

⇒ garble t separate copies of CPU circuit

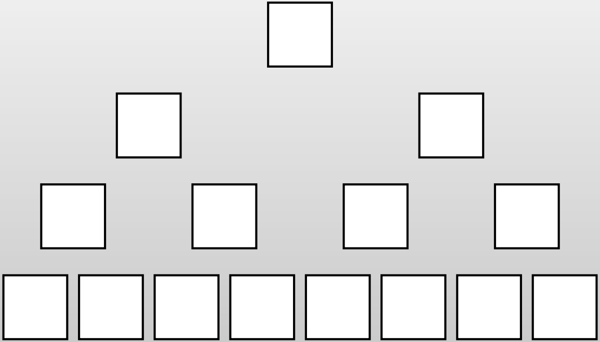
Memory accesses can depend on private data!

⇒ Compile to **oblivious RAM** (ORAM) [GoldreichOstrovsky96]

Memory accesses determined **only at runtime!**

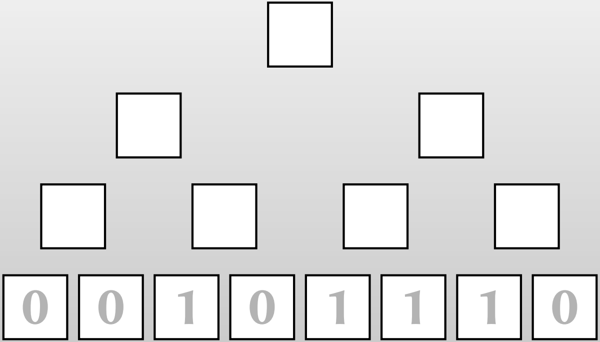
?? How do we get **wire labels** encoding $M[\ell_1]$ when ℓ_1 determined at run-time?

Garbled Memory [GargLuOstrovsky15]



- Binary tree of little **garbled circuits**

Garbled Memory [GargLuOstrovsky15]



- Binary tree of little **garbled circuits**
- Leaf circuits have 1 bit of RAM memory hard-coded

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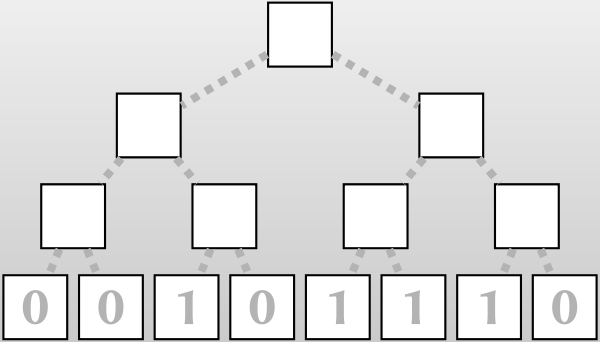
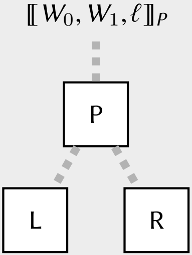


- Binary tree of little **garbled circuits**
- Leaf circuits have 1 bit of RAM memory hard-coded
- Internal circuits have **input wire labels** of children hard-coded (can pass secret information to a child)

Garbled Memory [GargLuOstrovsky15]

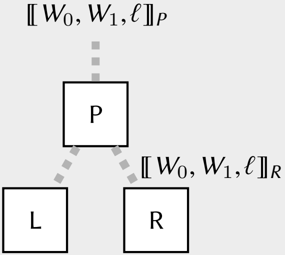
Internal node circuits:



Given (garbled input) W_0, W_1, ℓ

Garbled Memory [GargLuOstrovsky15]

Internal node circuits:

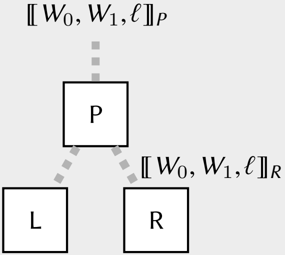


Given (garbled input) W_0, W_1, ℓ

Translate to child's garbled encoding, based on appropriate bit of ℓ

Garbled Memory [GargLuOstrovsky15]

Internal node circuits:



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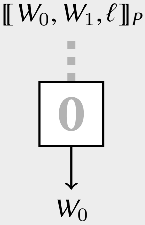
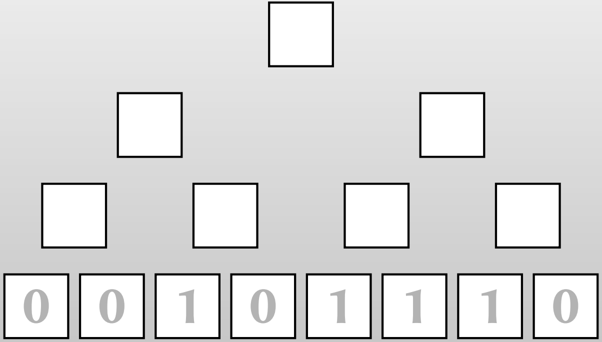
Leaf node circuits:



Given (garbled input) W_0, W_1, ℓ

Output W_0 or W_1 **in the clear**, based on hard-coded bit

Garbled Memory [GargLuOstrovsky15]



- This collection of circuits hard-codes $M[1 \ldots N]$

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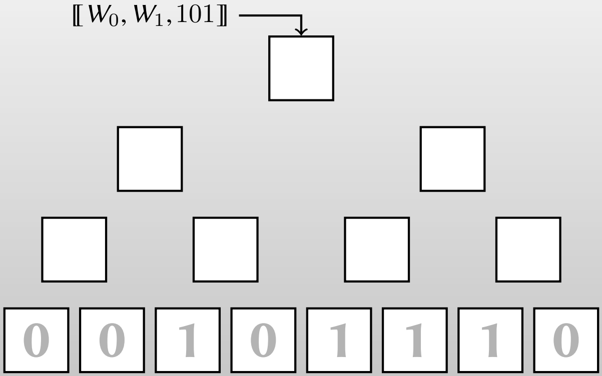

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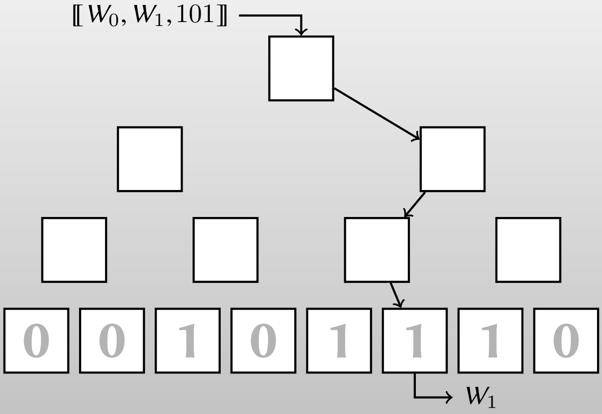
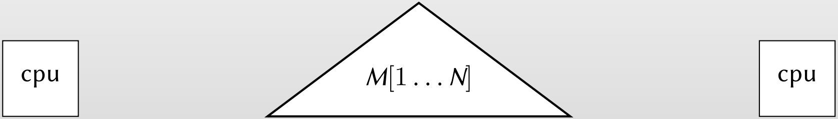


- This collection of circuits hard-codes $M[1 \ldots N]$
- Give it (garbled) $[\![W_0, W_1, \ell]\!] \Rightarrow$ it will give you $W_{M[\ell]}$ (in the clear)
- *(evaluator must know ℓ to evaluate correct subcircuits)*

Garbled RAM main idea



- Garble two copies of the RAM CPU circuit

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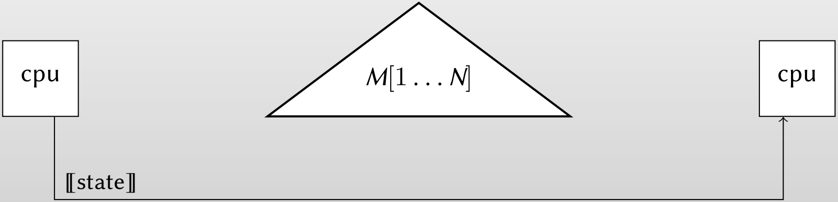

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- Use same wire labels for outgoing state / incoming state ("same wire")

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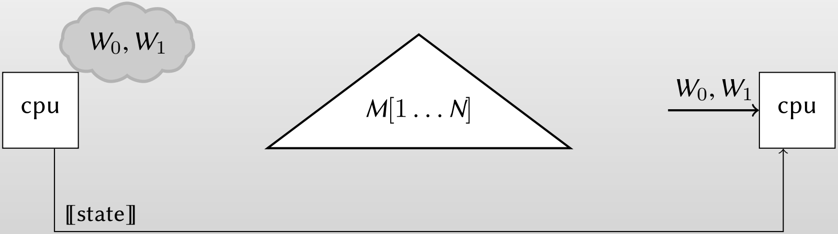

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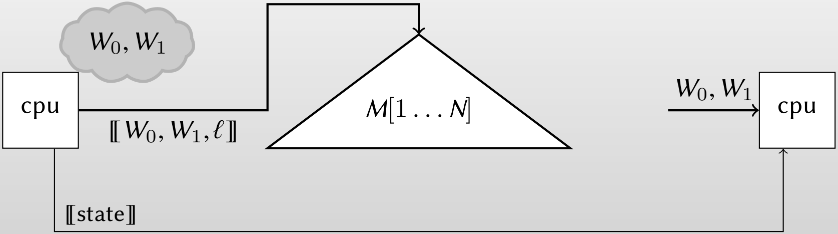

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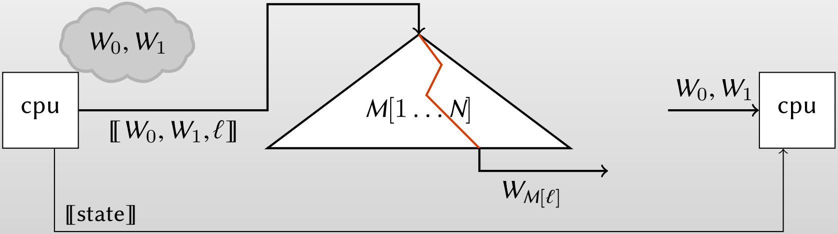

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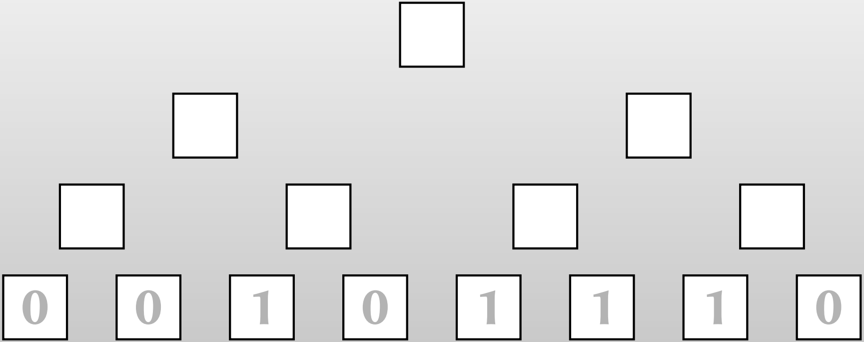
- Use same wire labels for outgoing state / incoming state ("same wire")
- First circuit has input labels of second circuit hard-coded
- On $(\textsc{read}, \ell)$ operation, first circuit:
  - outputs ℓ in clear
  - passes **garbled** W_0, W_1, ℓ to garbled memory
- Garbled memory outputs correct wire label $W_{M[\ell]}$ in the clear

Garbled Memory Fine Print



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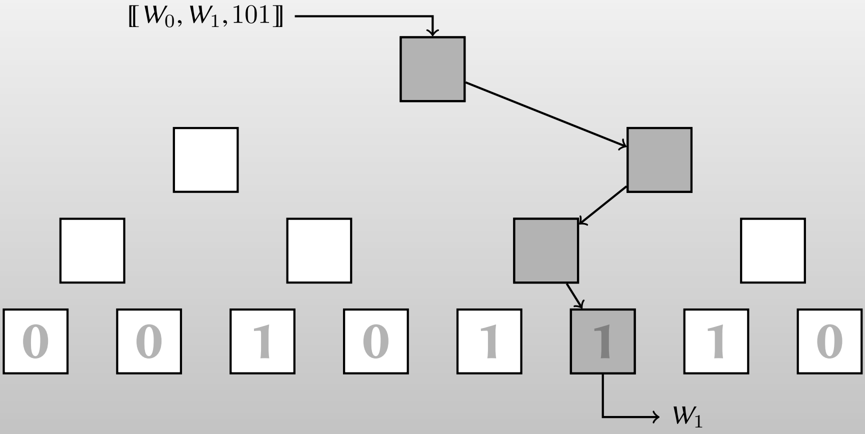

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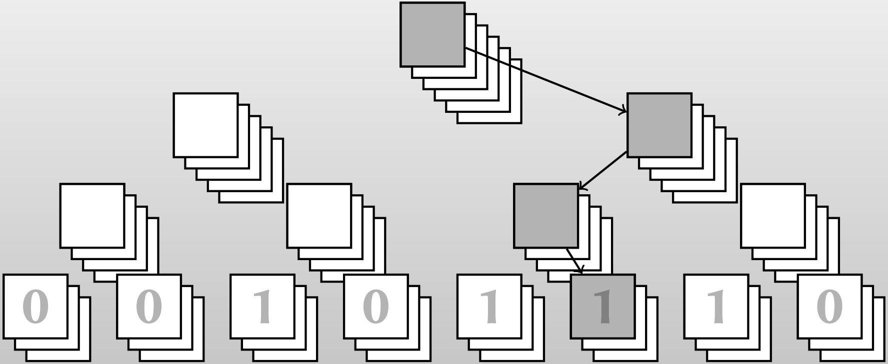

- Each little garbled circuit is **single-use!**
- Solution: each node contains **queue** of circuits
  - Chernoff bound determines # of circuits in each queue
  - Circuits pass hard-coded information to successor in queue

Summary / Open Problems

Garbling beyond boolean circuits

New techniques for garbled **arithmetic circuits**:

- Comparing two CRT-encoded values?
- Converting CRT representation to binary?
- Integer division?
- Modular arithmetic (different than CRT primorial modulus)?

New techniques for garbled **RAM programs**:

- How do these constructions perform in real world?
- How to reduce “slack” introduced by Chernoff bound?

the end.

any questions?