1. Figure 1 shows NMOS and PMOS devices with drains, source, and gate ports annotated. Determine the mode of operation (saturation, linear, or cutoff) and drain current $I_D$ for each of the biasing configurations given below. Use the following transistor data: NMOS: $k'_n = 115 \mu A/V^2$, $V_{T0} = 0.43 V$, $\lambda = 0.06 V^{-1}$, PMOS: $k'_p = 30 \mu A/V^2$, $V_{T0} = -0.4 V$, $\lambda = -0.1 V^{-1}$. Assume $(W/L) = 1$.
   a. NMOS: $V_{GS} = 2.5 V$, $V_{DS} = 2.5 V$. PMOS: $V_{GS} = -0.5 V$, $V_{DS} = -1.25 V$.
   b. NMOS: $V_{GS} = 3.3 V$, $V_{DS} = 2.2 V$. PMOS: $V_{GS} = -2.5 V$, $V_{DS} = -1.8 V$.
   c. NMOS: $V_{GS} = 0.6 V$, $V_{DS} = 0.1 V$. PMOS: $V_{GS} = -2.5 V$, $V_{DS} = -0.7 V$.

2. For the circuit in Figure 2, $V_s = 3.3 V$. Assume $A_0 = 12 \mu m^2$, $\phi_0 = 0.65 V$, and $m = 0.5$. $N_A = 2.5 E16$ and $N_D = 5 E15$.
   a. Find $I_D$ and $V_D$.
   b. Is the diode forward- or reverse-biased?
   c. Find the depletion region width, $W_J$, of the diode.
   d. Use the parallel-plate model to find the junction capacitance, $C_J$.
   e. Set $V_s = 1.5 V$. Again using the parallel-plate model, explain qualitatively why $C_J$ increases.

3. Given the data in Table 1 for a short channel NMOS transistor with $V_{DSAT} = 0.6 V$ and $k' = 100 \mu A/V^2$, calculate $V_{T0}$, $\gamma$, $\lambda$, $2|\phi_f|$, and $W/L$. 

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**Figure 1** PMOS and NMOS Devices

**Figure 2** Series Diode Circuit
4. An NMOS device is plugged into the test configuration shown below in Figure 3. The input $V_{in} = 2$V. The current source draws a constant current of 50 µA. R is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: $k' = 110 \times 10^{-6}$ V/A², $V_T = 0.4$, and $V_{DSAT} = 0.6$V. The transistor has a $W/L = 2.5 \mu/0.25 \mu$. For simplicity body effect and channel length modulation can be neglected. i.e $\lambda = 0$, $\gamma = 0$.
   a. When $R = 10k\Omega$ find the operation region, $V_D$ and $V_S$.
   b. When $R = 30k\Omega$ again determine the operation region $V_D$, $V_S$
   c. For the case of $R = 10k\Omega$, would $V_S$ increase or decrease if $\lambda \neq 0$. Explain qualitatively

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Figure 3 Test Configuration of NMOS Device
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5. A state-of-the-art, synthesizable, embedded microprocessor consumes 0.4mW/MHz when fabricated using a 0.18 µm process. With typical standard cells (gates), the area of the processor is 0.7 mm². Assuming a 100 MHz clock frequency, and 1.8 V power supply. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc.
   a. Using fixed voltage scaling and constant frequency, what will the area, power consumption, and power density of the same processor be, if scaled to 0.12 µm technology, assuming the same clock frequency?
   b. If the supply voltage in the scaled 0.12 µm part is reduced to 1.5 V what will the power consumption and power density be?
   c. How fast could the scaled processor in Part (b) be clocked? What would the power and power density be at this new clock frequency?
   d. Power density is important for cooling the chip and packaging. What would the supply voltage have to be to maintain the same power density as the original processor?

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**Table 1**

<table>
<thead>
<tr>
<th></th>
<th>$V_{GS}$</th>
<th>$V_{DS}$</th>
<th>$V_{BS}$</th>
<th>$I_D$ (µA)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>2.5</td>
<td>1.8</td>
<td>0</td>
<td>1812</td>
</tr>
<tr>
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<td>1.8</td>
<td>0</td>
<td>1297</td>
</tr>
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<td>2</td>
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</tr>
<tr>
<td>4</td>
<td>2</td>
<td>1.8</td>
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<td>1146</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
<td>1.8</td>
<td>-2</td>
<td>1039</td>
</tr>
</tbody>
</table>
6. The superscalar, superpipelined, out-of-order executing, highly parallel, fully x86 compatible JMRII microprocessor was fabricated in a 0.25 μm technology and was able to operate at 100 MHz, consuming 10 watts using a 2.5 V power supply.
   a. Using fixed voltage scaling, what will the speed and power consumption of the same processor be if scaled to 0.1 μm technology?
   b. If the supply voltage on the 0.1 μm part were scaled to 1.0 V, what will the power consumption and speed be?
   c. What supply should be used to fix the power consumption at 10 watts? At what speed would the processor operate?

7. Consider a CMOS process with the following capacitive parameters for the NMOS transistor: $C_{GSO}$, $C_{GSO}$, $C_{DSO}$, $C_{DJ}$, $m_j$, $C_{jsw}$, $m_{jsw}$, and PB, with the lateral diffusion equal to $L_D$. The MOS transistor M1 is characterized by the following parameters: $W$, $L$, $AD$, $PD$, $AS$, $PS$.

![Figure 4 Circuit to measure total input capacitance](image)

   a. Consider the configuration of Figure 4. $V_{DD}$ is equal to $V_T$ (the threshold voltage of the transistor) Assume that the initial value of $V_g$ equals 0. A current source with value $I_{in}$ is applied at time 0. Assuming that all the capacitance at the gate node can be lumped into a single, grounded, linear capacitance $C_T$, derive an expression for the time it will take for $V_g$ to reach 2 $V_T$
   b. The obvious question is now how to compute $C_T$. Among, $C_{db}$, $C_{sb}$, $C_{gs}$, $C_{gd}$, $C_{gb}$ which of these parasitic capacitances of the MOS transistor contribute to $C_T$. For those that contribute to $C_T$ write down the expression that determines the value of the contribution. Use only the parameters given above. If the transistor goes through different operation regions and this impacts the value of the capacitor, determine the expression of the contribution for each region (and indicate the region).
   c. Consider now the case depicted in Figure 5. Assume that $V_d$ is initially at 0 and we want to charge it up to 2 $V_T$. Again among, $C_{db}$, $C_{sb}$, $C_{gs}$, $C_{gd}$, $C_{gb}$ which device capacitances contribute to the total drain capacitance? Once again, make sure you differentiate between different operation regions.
Figure 5 Circuit to measure total drain capacitance