1. (a) NMOS: $V_{DS} > V_{GS} - V_T \Rightarrow$ saturation.

   $$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) = 283.3 \mu A$$

   PMOS: $|V_{DS}| > |V_{GS} - V_T| \Rightarrow$ saturation.

   $$I_D = \frac{1}{2} k_p' \frac{W}{L} (|V_{GS} - V_T|^2 (1 + \lambda |V_{DS}|) = 0.17 \mu A$$

   (b) NMOS: $V_{DS} < V_{GS} - V_T \Rightarrow$ linear.

   $$I_D = \frac{k_n'}{L} \{(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\} = 447.8 \mu A$$

   PMOS: $|V_{DS}| > |V_{GS} - V_T| \Rightarrow$ linear.

   $$I_D = \frac{k_p'}{L} \{(|V_{GS}| - |V_T|)|V_{DS}| - \frac{V_{DS}^2}{2}\} = 64.8 \mu A$$

   (c) NMOS: $V_{DS} < V_{GS} - V_T \Rightarrow$ linear.

   $$I_D = \frac{k_n'}{L} \{(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\} = 1.38 \mu A$$

   PMOS: $|V_{DS}| > |V_{GS} - V_T| \Rightarrow$ linear.

   $$I_D = \frac{k_p'}{L} \{(|V_{GS}| - |V_T|)|V_{DS}| - \frac{V_{DS}^2}{2}\} = 36.75 \mu A$$

2. (a) $I_D = 0 A$, $V_D = -3.3 V$

   (b) Reverse biased

   (c) $W_j = \sqrt{\left(\frac{2\epsilon_{Si} N_A + N_D}{q \frac{N_A N_D}{N_A N_D}}\right) (\phi_0 - V_D)} = 1.108 \mu m$

   $\epsilon_{Si} = 11.7 \times \epsilon_0 = 11.7 \times 8.854 \times 10^{-12} F/m = 1.036 \times 10^{-10} F/m$

   $q = 1.6 \times 10^{-19} C$

   (d) $C_j = \frac{\epsilon_{Si} A_D}{W_j} = 1.122 f F$
(e) Lower reverse-biased voltage leads to reduced width of depletion region, \( W_j \). Effectively as plates of capacitor are brought closer together, capacitance \( C_j \) increases.

3. \( V_{DS} > V_{DSAT} \implies \) velocity saturation.
Assuming for all 5 cases that \( V_{min} = V_{DSAT} = 0.6V \),

In cases 1-3,
\( V_{BS} = 0 \implies V_T = V_{T0} \).
Using \( I_D = k' \frac{W}{L} \{(V_{GS} - V_T)V_{min} - \frac{V_{min}^2}{2}\}(1 + \lambda V_{DS}) \)
\( W \frac{L}{L} = 15, V_{T0} = 0.44V, \lambda = 0.08V^{-1} \)

In cases 4-5,
Substituting previously found values and using
\( V_T = V_{T0} + \gamma (\sqrt{|-2\Phi_F + V_{SB}|} - (\sqrt{|-2\Phi_F|}) \\
|2\Phi_F| = 0.6V, \gamma = 0.3V^{1/2} \)

4. (a) \( V_D = V_{DD} - I_D R_D = 2V \)
For saturation, \( V_{DS} > V_{GS} - V_T \implies V_D > V_G - V_T \)
\( \therefore \) NMOS is in saturation region.
\[
I_D = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_T)^2 = 50 \mu A \\
V_S = 1.3V
\]

(b) \( V_D = V_{DD} - I_D R_D = 1V \)
For saturation, \( V_{DS} > V_{GS} - V_T \implies V_D > V_G - V_T \)
\( \therefore \) NMOS is in linear region.
\[
I_D = k' \frac{W}{L} \{(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\} = 50 \mu A \\
V_S = 0.93V
\]

(c) Based on equation \( I_D = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_T)^2(1 + \lambda V_{DS}), \lambda \neq 0 \) means \( I_D \) has to increase. However, since current source fixes \( I_D \) to 50 \( \mu A \), \( V_{GS} \) needs to decrease by increasing \( V_S \). So \( V_S \) would increase.

5. (a) For short-channel, fixed-voltage scaling:
\[
S = \frac{0.18 \mu}{0.12 \mu} = 1.5
\]
\[ A' = \frac{A}{S^2} = 0.311 \text{mm}^2 \]
\[ P' = \frac{P}{S^2} = 0.4 \text{mW/MHz} \times 100 \text{MHz} = 40 \text{mW} \]
\[ \left( \frac{P}{A} \right)' = 128.62 \text{mW/mm}^2 \]

(b) General scaling: \( U = \frac{1.8}{1.5} = 1.2 \)
\[ P' = \frac{P}{U^2} = 27.78 \text{mW} \]
\[ \left( \frac{P}{A} \right)' = 89.32 \text{mW/mm}^2 \]

(c) \( f' = f \times S = 150 \text{MHz} \)  
Assuming dynamic power dominates,
\[ P_{150} = P_{100} \times S = 41.67 \text{mW} \]
\[ \left( \frac{P_{150}}{A} \right)' = 133.99 \text{mW/mm}^2 \]

(d) Since power density scales by \( \frac{S^2}{U^2} \):
\[ \left( \frac{P_{150}}{A} \right)' = \left( \frac{P_{100}}{A} \right) \times \frac{S^2}{U^2} \]
\[ U^2 = S^3 \]
\[ U = 1.837 \]
\[ U = \frac{1.8}{V'} \]
\[ V' \approx 1V \]

6. (a) Assuming long-channel, fixed-voltage scaling:
\( S = 2.5 \)
\[ f' = f \times S^2 = 625 \text{MHz} \]
\[ P' = P \times S = 25 \text{W} \]

(b) Full-scaling (since \( U = S = 2.5 \)):
\[ f' = f \times S = 250 \text{MHz} \]
\[ P' = \frac{P}{S^2} = 1.6 \text{W} \]

(c) To keep power constant:
\[ \frac{S}{U^3} = 1 \Rightarrow U = 1.36 \]
\[ V' = \frac{V}{U} = 1.84V \]
\[ f' = f \times \frac{S^2}{U} \approx 460\,MHz \]

7. (a) Device is off while \( V_G < V_T \).

For \( V_G = 0 \rightarrow V_T \): \( C_T = C_T(1) \)
\( V_G = V_T \rightarrow 2V_T \): \( C_T = C_T(2) \)

\[ t_1 = C_T(1) \frac{V_T}{I_{in}} \]
\[ t_2 = C_T(2) \frac{2V_T - V_T}{I_{in}} \]
\[ \therefore t = t_1 + t_2 = [C_T(1) + C_T(2)] \frac{V_T}{I_{in}} \]

(b) \( C_{sb}, C_{db} \) do not contribute to gate capacitance.

While device is off, \( V_G < V_T, C_{gb} \) contributes to \( C_T \).
During \( V_T < V_G < 2V_T \), \( C_{gb} \) falls to zero.

\[ 0 < V_G < V_T \implies C_T = C_T(1) = C_{ox}WL + W(C_{GD0} + C_{GS0}) \, V_T < \]
\[ V_G < 2V_T \implies C_T = C_T(2) = \frac{2}{3} C_{ox}WL + W(C_{GD0} + C_{GS0}) \]

(c) Device is always off. \( C_{gs}, C_{gb}, C_{sb} \) do not have connection to drain node.
Overlap of \( C_{gd} \) and varying \( C_{db} \) make up \( C_T \).

\[ C_T = WC_{GD0} + K_{eq}C_{j0} + K_{eqsw}C_{jsw0} \]
\[ C_{j0} = C_{j}AD \]
\[ C_{jsw0} = C_{jsw}PD \]
\[ C_T = WC_{GD0} + K_{eq}C_{j}AD + K_{eqsw}C_{jsw}PD \]
where,

\[ K_{eq} = \frac{-P_{B}^{m_j}}{2V_T(1 - m_j)} \left[ (P_B - 2V_T)^{(1-m_j)} - (P_B)^{(1-m_j)} \right] \]
\[ K_{eqsw} = \frac{-P_{B}^{m_{jsw}}}{2V_T(1 - m_{jsw})} \left[ (P_B - 2V_T)^{(1-m_{jsw})} - (P_B)^{(1-m_{jsw})} \right] \]