Class Grading

- Homework (5) ------ 10%
- Lab ------ 20%
- Midterm 1 ------ 20%
- Midterm 2 ------ 20%
- Final Project ------ 30%

Textbooks:

Digital Integrated Circuits, A Design Perspective, Jan M Rabaey
History of Digital Design (Mechanical Era)

- **Charles Babbage - Difference Engine (1832)**
  - Made for decimal number system
  - 25,000 mechanical parts.
  - 1700 pounds (~500,000 USD in 2018 money)

- **Analytical Engine (1834)**
  - Can perform addition, subtraction, multiplication and division.
  - Two-Cycle sequence, store and mill(execute).
  - Even had pipelining
Electrical Solution

- **ENIAC** (*Electronic Numerical Integrator and Computer*), 1943
  - Military Computer, Used in Manhattan Project
  - 18,000 vacuum tubes
  - 80 feet long, 8.5 feet high
- **UNIVAC** (*Universal Automatic Computer*), 1951
  - Commercial variant
- Huge Power requirements.
- Cumbersome, lot of parts
- Literally, lots of bugs
  - Term coined by Grace Hooper for systems
Transistor era

- Transistor invented in 1947 in Bell Labs by John Bardeen[1]
- First IC by Jack Kilby at Texas Instruments in 1958
  - Jack Kilby was awarded Nobel Prize for this contribution
- 1960, First commercial logic gate.
- 1962, TTL(transistor transistor logic).
- I2L, (integrated Injection Logic)

MOSFET era

- Idea was around since 1925, had gate stability problem.
- Took off in 1970s
- Intel, 4004 1972
- Intel, 8080 1974
- Fast forward to today
Moore’s law in Microprocessors

Transistors on Lead Microprocessors double every 2 years

2X growth in 1.96 years!
Die Size Growth

~7% growth per year
~2X growth in 10 years

Die size grows by 14% to satisfy Moore’s Law

Courtesy, Intel
Power will be a major problem

Power delivery and dissipation will be prohibitive

Courtesy, Intel
Lead Microprocessors power continues to increase

Courtesy, Intel
Power will be a major problem

Power delivery and dissipation will be prohibitive

Courtesy, Intel
Challenges in Digital Design

∞ DSM

“Microscopic Problems”
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

Everything Looks a Little Different

∞ 1/DSM

“Macroscopic Issues”
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

...and There’s a Lot of Them!
Productivity Trends

Complexity outpaces design productivity

Source: Sematech

Courtesy, ITRS Roadmap
Technology Scaling

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction
Design Abstraction Levels

- System
- Module
- Gate
- Circuit
- Device
Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function
Cost of Integrated Circuits

- **NRE (non-recurrent engineering) costs**
  - design time and effort, mask generation
  - one-time cost factor

- **Recurrent costs**
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area
Increasing NRE Cost

“The club of people who can afford an extreme sub-micron ASIC or COTS design is getting pretty exclusive.”

Ron Wilson, EE Times (May 2000)

70nm ASICs will have $4M NRE
Die Cost

Single die

Wafer

Going up to 12” (30cm)
Cost per transistor
Yield

\[ Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\% \]

\[
\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}
\]

\[
\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}
\]
Defects

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

$\alpha$ is approximately 3

$$\text{die cost} = f (\text{die area})^4$$
## Examples

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Def./cm²</th>
<th>Area mm²</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486 DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>Power PC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super Sparc</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
Reliability—Noise in Digital Integrated Circuits

Inductive coupling  Capacitive coupling  Power and ground noise
DC Operation - Voltage Transfer Characteristic

VOH = f(VOL)
VOL = f(VOH)
VM = f(VM)

Switching Threshold
Nominal Voltage Levels
Mapping between analog and digital signals

- "1": $V_{OH}$, $V_{IH}$
- Undefined Region
- "0": $V_{IL}$, $V_{OL}$

Graph:
- $V_{out}$ vs $V_{in}$
- Slope = -1
- $V_{IH}$ and $V_{IL}$
Definition of Noise Margins

"1"  
$V_{OH}$  
$NM_H$  
$V_{IH}$  
Noise margin high

"0"  
$V_{OL}$  
$NM_L$  
$V_{IL}$  
Noise margin low

Gate Output  
Gate Input

Undefined Region
Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources
Key Reliability Properties

- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;
Regenerative Property

Regenerative

Non-Regenerative
Regenerative Property

A chain of inverters

Simulated response
Fan-in and Fan-out

Fan-out $N$

Fan-in $M$
Ideal Gate

\[ V_{out} \]

\[ V_{in} \]

\[ g = \infty \]

\[ R_i = \infty \]
\[ R_o = 0 \]
\[ \text{Fanout} = \infty \]
\[ \text{NM}_{H} = \text{NM}_{L} = V_{DD}/2 \]
An Old-time Inverter
Delay Definitions

\[ V_{in} \]

\[ t \]

\[ V_{out} \]

\[ t_f \]

\[ t_{pHL} \]

\[ t_{pLH} \]

\[ 10\% \]

\[ 50\% \]

\[ 90\% \]
Ring Oscillator
A First-Order RC Network

\[ v_{out}(t) = \left( 1 - e^{-t/\tau} \right) V \]

\[ t_p = \ln(2) \quad \tau = 0.69 \text{ RC} \]

Important model – matches delay of inverter
Power Dissipation

Instantaneous power:
\[ p(t) = v(t)i(t) = V_{\text{supply}}i(t) \]

Peak power:
\[ P_{\text{peak}} = V_{\text{supply}}i_{\text{peak}} \]

Average power:
\[ P_{\text{ave}} = \frac{1}{T} \int_{t}^{t+T} p(t)\,dt = \frac{V_{\text{supply}}}{T} \int_{t}^{t+T} i_{\text{supply}}(t)\,dt \]
Energy and Energy-Delay

**Power-Delay Product (PDP)** =

\[ E = \text{Energy per operation} = P_{av} \times t_p \]

**Energy-Delay Product (EDP)** =

\[ \text{quality metric of gate} = E \times t_p \]
A First-Order RC Network

\[
E_{0 \rightarrow 1} = \int_{0}^{T} P(t) dt = V_{dd} \int_{0}^{T} i_{\text{supply}}(t) dt = V_{dd} \int_{0}^{T} C_L dV_{\text{out}} = C_L \cdot V_{dd}^2
\]

\[
E_{\text{cap}} = \int_{0}^{T} P_{\text{cap}}(t) dt = \int_{0}^{T} V_{\text{out}} i_{\text{cap}}(t) dt = V_{dd} \int_{0}^{T} C_L V_{\text{out}}^2 dV_{\text{out}} = \frac{1}{2} C_L \cdot V_{dd}^2
\]