Alternative Register Styles
Pulse Registers

- Create a short pulse around rising or falling edge of the clock
- This is done to avoid race condition
Pulse Registers

Advantages

● Reduced clock load
● Small number of transistors

Disadvantages

● Increased verification complexity
Pulse Registers (Contd.)

Flow-through positive edge-triggered register
Sense-Amplifier-Based Registers

Accept small signal inputs and amplify the to rail-to-rail swing
Sense-Amplifier-Based Registers

$L_3$ is isolated so charge accumulates until $L_1/L_3$ change state, causing $L_2$ to change state as well. As a result the flip-flop outputs change.

The leakage current attempts to charge $L_1/L_3$ but the DC path through the shorting transistor allows it to leak away to ground.
Pipelining: An Approach to Optimize Sequential Circuits
Pipelining

(a) Reference circuit

<table>
<thead>
<tr>
<th>Clock Period</th>
<th>Adder</th>
<th>Absolute Value</th>
<th>Logarithm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$a_1 + b_1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>$a_2 + b_2$</td>
<td>$</td>
<td>a_1 + b_1</td>
</tr>
<tr>
<td>3</td>
<td>$a_3 + b_3$</td>
<td>$</td>
<td>a_2 + b_2</td>
</tr>
<tr>
<td>4</td>
<td>$a_4 + b_4$</td>
<td>$</td>
<td>a_3 + b_3</td>
</tr>
<tr>
<td>5</td>
<td>$a_5 + b_5$</td>
<td>$</td>
<td>a_4 + b_4</td>
</tr>
</tbody>
</table>

(b) Pipelined version

$$T_{\text{min.pipe}} = t_{c-q} + \max(t_{p_d,\text{add}}, t_{p_d,\text{abs}}, t_{p_d,\text{log}})$$
Latch versus Register-Based Pipeline
Pipelined datapath using $C^2$MOS latches
Pipelined datapath using $C^2$MOS latches (Contd.)
NORA-CMOS (Cont'd.)

(a) CLK-module

(b) $\overline{CLK}$-module

<table>
<thead>
<tr>
<th>CLK block</th>
<th>Logic</th>
<th>Latch</th>
</tr>
</thead>
<tbody>
<tr>
<td>$CLK = 0$</td>
<td>Precharge</td>
<td>Hold</td>
</tr>
<tr>
<td>$CLK = 1$</td>
<td>Evaluate</td>
<td>Evaluate</td>
</tr>
</tbody>
</table>
Nonbistable Sequential Circuits
The Schmitt Trigger
CMOS Implementation of Schmitt Trigger
Monostable Sequential Circuits
Astable Circuit
Perspective
Choosing a Clocking Strategy

(a) delay cell

(b) two stage VCO

(c) simulated waveforms of 2-stage VCO
Summary

- Bistable Circuits
- Latch
- Register
- Dynamic memory
- Pulse based registers
- Choice of clocking styles
- Schmitt Trigger
- Monostable Circuits
- Astable Circuits
Implementation Strategies for Digital ICs
Introduction

A growing gap between design complexity and design productivity
Generic Digital Processor
Generic Digital Processor

- The datapath
- The Control Module
- The memory module
- The interconnect
System-on-a-Chip
Impact of Implementation Choices

- **None**: 100-1000 MOPS/mW
- **Somewhat flexible**: 10-100 MOPS/mW
- **Fully flexible**: 1-10 MOPS/mW
- **Domain-specific processor (e.g., DSP)**: 0.1-1 MOPS/mW
Implementation Strategies

Digital Circuit Implementation Approaches

- Custom
  - Cell-based
    - Standard Cells
    - Compiled Cells
  - Array-based
    - Macro Cells
    - Pre-diffused (Gate Arrays)
    - Pre-wired (FPGA's)
- Semicustom