Transmission Gate Logic

(a) Circuit

(b) Symbolic representation

A = \( V_{DD} \)

B (initially at 0)

C = \( V_{DD} \)

\( \bar{C} = 0 \)

(a) charging node B

A = 0

B (initially at \( V_{DD} \))

C = \( V_{DD} \)

\( \bar{C} = 0 \)

(a) discharging node B
Example (Multiplexer)

\[ \bar{F} = (A \cdot S + B \cdot \bar{S}) \]
Example (XOR)
Performance of Pass-Transistor-Gate Logic
Performance of Pass-Transistor-Gate Logic

\[ R_n = \frac{V_{DD} - V_{out}}{I_N} = \frac{V_{DD} - V_{out}}{k_n \left( \frac{W}{L} \right)_N \left( (V_{DD} - V_{out} - V_{Tn})V_{DSAT} - \frac{V_{DSAT}^2}{2} \right)} \]

\[ \approx \frac{V_{DD} - V_{out}}{k_n \left( V_{DD} - V_{out} - V_{Tn} \right)V_{DSAT}} \]

\[ R_p = \frac{V_{DD} - V_{out}}{I_P} = \frac{V_{DD} - V_{out}}{k_p \cdot \left( -V_{DD} - V_{Tp} \right)(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2}} \]

\[ \approx \frac{1}{k_p \left( V_{DD} - |V_{Tp}| \right)} \]
Performance of Pass-Transistor-Gate Logic

(a) A chain of transmission gates

\[ t_p(V_n) = 0.69 \sum_{k=0}^{n} CR_{eq} k = 0.69 CR_{eq} \frac{n(n+1)}{2} \]
Example

- No. of gates - 16
- Average resistance - 8 kΩ each
- Average capacitance - 3.5fF each

\[ t_p = 0.69 \cdot CR_{eq} \frac{n(n+1)}{2} = 0.69 \cdot (3.6fF)(8K\Omega)\left(\frac{16(16+1)}{2}\right) \approx 2.7\,ns \]
How to deal with propagation delay

Add m number of buffers,

\[ t_p = 0.69 \left( \frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right) + \left( \frac{n}{m} - 1 \right) t_{buf} \]

\[ = 0.69 \left[ CR_{eq} \frac{n(m+1)}{2} \right] + \left( \frac{n}{m} - 1 \right) t_{buf} \]

Optimum number of m

\[ m_{opt} = 1.7 \sqrt{\frac{t_{pbuf}}{CR_{eq}}} \]
Dynamic CMOS Design

- Precharge
- Evaluation
Features of Dynamic CMOS Design

- Logic implemented by NMOS pull-down network
- N+2 transistors used
- Non-ratioed
- Consumes only dynamic power
- Faster switching speed
  - Reduced logical effort due to reduced load capacitance
  - No short circuit
Speed and Power Dissipation of Dynamic Logic

- Increased speed and reduced implementation area
- Have to keep pre-charge in mind
- Advantage from power perspective
  - Lower physical capacitance due to reduced number of gates
  - Can have one logical transition per cycle (No Glitch)
  - No short-circuits
- Disadvantages
  - What about power consumed by clock?
  - Still higher number of transistor than minimum required for logic
  - Leakage current
  - Higher switching activity due to periodic precharge

\[
\alpha_0 \rightarrow 1 = p_0 \\
\alpha_0 \rightarrow 1 = \frac{N_0}{2^N}
\]
Signal Integrity Issues in Dynamic Design
Charge Leakage

(a) Leakage sources

(b) Effect on waveforms
Charge Leakage (contd.)

(a)

(b)
Charge Sharing

1. $\Delta V_{out} < V_{Tn} - \text{In this case, the final value of } V_X \text{ equals } V_{DD} - V_{Tn}(V_X). \text{ Charge conservation yields}$

$$C_L V_{DD} = C_L V_{out}(t) + C_a [V_{DD} - V_{Tn}(V_X)]$$

or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = \frac{C_a}{C_r} [V_{DD} - V_{Tn}(V_X)]$$

2. $\Delta V_{out} > V_{Tn} - V_{out} \text{ and } V_X \text{ reach the same value:}$

$$\Delta V_{out} = -V_{DD} \left( \frac{C_a}{C_a + C_L} \right)$$

$$\frac{C_a}{C_L} = \frac{V_{Tn}}{V_{DD} - V_{Tn}}$$
Charge Sharing (Contd.)
Capacitive Coupling

- High output impedance makes the circuit very sensitive to crosstalk effects.
- backgate(output-to-input)
- Input of static NAND gate coupled to output of Dynamic NAND Gate
Clock Feedthrough

Figure 6.62 E
the effect of \( ba \)

due to clock feedthrough

Out\(_1\) (does not discharge to gnd)
Cascading Dynamic Gates
Cascading Dynamic Gates

(a)

(b)
Domino Logic
Domino Logic (Contd.)

- Only non-inverting logic can be implemented.
- Very high speeds can be achieved.
Dealing with Non Inverting Property of Domino Logic

(a) before logic transformation

(b) after logic transformation
Dual-rail domino

Figure 6.68 Simple dual rail
Optimizing of Domino Logic Gates
Multiple-output domino

\[ O_1 = A \cdot B(C+D) \]
\[ O_2 = B(C+D) = B \cdot O_3 \]
\[ O_3 = C+D \]
Compound domino
np-CMOS
Which one to choose?

- Primary requirement
  - Ease of design
  - Robustness
  - Area
  - Speed
  - Power dissipation
Static CMOS

Advantages

- Robust
- High degree of automation and trouble free

Disadvantages

- Requires more area
- Not good performance in case of large fan-in
Pseudo NMOS

Advantages

● Simple
● Fast

Disadvantages

● Reduced noise margin
● Static power dissipation
Pass-Transistor Logic

Advantage

- Good for multiplexers and adders

Disadvantage

- Low input impedance
Dynamic Logic

Advantages

- Easy to implement fast and complex gates

Disadvantages

- Parasitic Effects
- Need periodic Refresh
Designing Logic for reduced Supply Voltages

(a) $V_{DD}/V_T$ for fixed performance

(b) Leakage as a function of $V_T$

\[ I_{leakage} = I_S 10^{\frac{V_{GS} - V_{TH}}{S} \left(1 - 10^{-\frac{nV_{DS}}{S}}\right)} \]
Designing Logic for reduced Supply Voltages

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>$V_X$</th>
<th>$I_{SUB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$V_{th} \ln (1+n)$</td>
<td>$I^N_{SUB}$ ($V_{GS} = V_{BS} = -V_X$)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>$I^N_{SUB}$ ($V_{GS} = V_{BS} = 0$)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$V_{dd} - V_T$</td>
<td>$I^N_{SUB}$ ($V_{GS} = V_{BS} = 0$)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$2I^P_{SUB}$ ($V_{SG} = V_{SB} = 0$)</td>
</tr>
</tbody>
</table>