Introduction
Timing Metric for sequential Circuits

- Setup time ($t_{su}$)
- Hold time ($t_{hold}$)
- Worst case propagation delay ($t_{c-q}$)
Timing Metric for sequential Circuits

Minimum clock period $T$ required for proper operation,

$$T \geq t_{c-q} + t_{plogic} + t_{su}$$

Condition for hold time,

$$t_{cdregister} + t_{cdlogic} \geq t_{hold}$$

$t_{cdregister}$ is minimum propagation delay of the register
Memory Classification
Foreground vs Background Memory

**Foreground memory:**

Memory is built into logic. (e.g. registers)

**Background Memory:**

Higher area densities through efficient use of array structures and by trading off performance and robustness for size.
Static versus Dynamic Memory

Static Memory:
- Preserve state as long as power is on.
- Built by using positive feedback or regeneration

Dynamic Memory:
- Based on charge storage
- Needs to be refreshed periodically
Latches versus Registers

Latches:
- Level-sensitive circuit
- Transparent mode
- Hold mode

Registers:
- Edge-triggered circuit
Static Latches and Registers
The Bistability Principle
Metastable vs Stable Operation points
Changing the state of bistable circuit

- Cutting the feedback loop
  \[ Q = \text{Clk}_n.Q + \text{Clk}.\text{In} \]

- Overpowering the feedback loop

  Feedback can be overpowered using trigger signal
Multiplexer-Based Latches

(a) Schematic diagram

(b) Non-overlapping clocks
Master-Slave Edge-Triggered Register
Master-Slave Edge-Triggered Register (Contd.)
Master-Slave Edge-Triggered Register (Contd.)
Non-Ideal Clock Signals
Non-Ideal Clock Signals (Contd.)

(a) Schematic diagram

(b) Two-phase non-overlapping clocks
Low Voltage Static Latches
Static SR Flip-Flop
Dynamic Latches and Registers
Dynamic Transmission-Gate Edge-Triggered Registers
Dynamic Transmission-Gate Edge-Triggered Registers

Advantages:

- Requires less transistors
- Setup time is just delay of transmission gates

Disadvantages:

- Periodic refresh
- Losses due to charge leakage, diode leakage and subthreshold current
- Clock overlap

\[ t_{\text{overlap}0-0} < t_{T1} + t_{I1} + t_{T2} \]
\[ t_{\text{hold}} > t_{\text{overlap}1-1} \]
$C^2MOS$- A Clock-Skew Insensitive Approach
C²MOS- A Clock-Skew Insensitive Approach

(a) (0-0) overlap

(b) (1-1) overlap
C²MOS- Transient Response
Dual-Edge Registers
True Single-Phase Clocked Register (TSPCR)

Positive Latch

Negative Latch
True Single-Phase Clocked Register (TSPCR) (Cont)

(a) Including logic into the latch
(b) AND latch
True Single-Phase Clocked Register (TSPCR) (Cont)

(a) Positive Latch

(b) Negative Latch
True Single-Phase Clocked Register (TSPCR) (Cont)
Alternative Register Styles
Pulse Registers

(a) register

(b) glitch generation

(c) glitch clock
Pulse Registers (Contd.)
Sense-Amplifier-Based Registers
Sense-Amplifier-Based Registers

$L_3$ is isolated so charge accumulates until $L_1/L_3$ change state, causing $L_2$ to change state as well. As a result the flip-flop outputs change.

The leakage current attempts to charge $L_1/L_3$ but the DC path through the shorting transistor allows it to leak away to ground.
Pipelining: An Approach to Optimize Sequential Circuits
Pipelining

(a) Reference circuit

<table>
<thead>
<tr>
<th>Clock Period</th>
<th>Adder</th>
<th>Absolute Value</th>
<th>Logarithm</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>$a_1 + b_1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>$a_2 + b_2$</td>
<td>$</td>
<td>a_1 + b_1</td>
</tr>
<tr>
<td>3</td>
<td>$a_3 + b_3$</td>
<td>$</td>
<td>a_2 + b_2</td>
</tr>
<tr>
<td>4</td>
<td>$a_4 + b_4$</td>
<td>$</td>
<td>a_3 + b_3</td>
</tr>
<tr>
<td>5</td>
<td>$a_5 + b_5$</td>
<td>$</td>
<td>a_4 + b_4</td>
</tr>
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(b) Pipelined version

\[
T_{\min,\text{pipe}} = t_{c-q} + \max(t_{p_d,\text{add}}, t_{p_d,\text{abs}}, t_{p_d,\text{log}})
\]
Latch versus Register-Based Pipeline
Latch versus Register-Based Pipeline (Contd.)
NORA-CMOS
NORA-CMOS (Contd.)

(a) CLK-module

(b) CLK-module

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<th>Logie</th>
<th>Latch</th>
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<td>CLK = 0</td>
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Nonbistable Sequential Circuits
The Schmitt Trigger

- $v_{in}$
  - $V_{M+}$
  - $V_{M-}$
- $t_0$ to $t$
- $v_{out}$
  - $t_0 + t_p$ to $t$
CMOS Implementation of Schmitt Trigger
Monostable Sequential Circuits
Astable Circuit
Perspective
Choosing a Clocking Strategy

(a) delay cell

(b) two stage VCO

(c) simulated waveforms of 2-stage VCO